ECE-124 Lab-4 Submission form – Spring 2015

Registered Lab Session			Demo TA	Report TA	Total Mark /20
☐ AM-Tue [203] ☐ PM-Tue [206]	☐ AM-Wed [201] ☐ PM-Wed [204]	☐ AM-Thu [202] ☐ PM-Thu [205]			

I am submitting this report for grading. I certify that this report, including any code, descriptions, flowcharts as part of the submission were written by me and has received no prior academic credit at this university or any institution. The penalty for plagiarism or submission without signature(s) will be grade of zero.

Name	UW User ID *NOT Student Number* (Please PRINT)	Signature	Effort Division
Partner A:			/100
Partner B:			/100

Lab Demo

Binary 1Hz, Modulus 1Hz and 10Hz clock dividers work?	+2	
1 Hz clock generated from the 10 Hz clock?	+1	
Traffic light works?	+3	
Discussion (VHDL Code, design techniques, combinational versus sequential processes, etc.)	+4	

Lab Report

Implementation procedure, decisions, debugging techniques and State view	+2	
Fully commented readable VHDL printout (double side printout is okay)	+2	
Functional simulation waveforms	+4	
Worst Case Speed Parameters (if applicable): Tsu _____ ns (setup time) Th _____ ns (hold time) Tco _____ ns (clock to output time) Tpd _____ ns (propagation delay time)	+1	
Circuit size in compilation report … Total logic elements: _____ /33216	+1	
Delay in report submission (10% deduction per day) number-of-days: _____	-1	

Comments
