A Compact Low Voltage CMOS Four-Quadrant Analog Multiplier

N. Kiatwarin*, W. Ngamkham** and W. Kiranon*

* Department of Telecommunication Engineering, Faculty of Engineering,
King Mongkut's Institute of Technology Ladkrabang, THAILAND
Tel: (662) 9883655 Ext. 239, Email: narumol@mut.ac.th

**Department of Control and Instrumentation Engineering
Mahanakorn University of Technology
51 Chuem Samphan Rd. Nong-Chok Bangkok 10530, THAILAND
Tel: (662) 9883655 Ext. 239, Email: wanaya@mut.ac.th

***Abstract*-In this paper, a compact low-voltage CMOS four-quadrant analog multiplier is proposed. The proposed circuit is obtained by rearranging circuit topology of a recently reported multiplier which is unpractical since the circuit topology itself needs an ideal voltage reference to form a multiplication function. By doing so, the ideal voltage reference is no longer required leading to achieve a new multiplier circuit with real compactness. Simulated results using PSPICE for 0.35µm CMOS process show that main performances of the proposed multiplier, including linearity, bandwidth and power consumption, are successfully improved.**

I. INTRODUCTION

Analog multipliers are found in many applications such as modulator, frequency doublers, absolute value circuit, and etc. These applications are required to operate in low voltage environment for improving their power efficiency and incorporating with mixed signal systems to be used in portable applications [1]. A number of circuit techniques for realizing a CMOS analog multiplier had been collected and systematically evaluated by G. Han and E. Sanchez-Sinencio [2].

According to [2], there are several means to realize a four quadrant analog multiplier and it is also suggested by [3] that using saturated MOSFET in strong inversion is more practical than any other means. Recently, based on a square-law relation of saturated MOSFET, various compact multiplier architectures which are constituted by a circuit cell called a "flipped voltage follower: FVF" [4], have been chronologically proposed in [5]-[8]. Most of them feature wide input range, high operating frequency and low power consumption which are resulted from excellent manipulations of the square-law function in high compactness structures.

Focusing on the latest version in [8], which is seemed to be the most compact circuit, it is found that the overall multiplier circuit can not be called compact since it requires an extra voltage reference connected between the resistive loads. To generate the extra voltage reference, more power consumption and circuit complexity are unavoidable.

In this paper, we propose a new multiplier circuit which is based on a similar technique to [8] but an arrangement of the circuit in transistor level is improved such that the extra voltage reference becomes redundant and can be eliminated. We then obtain a four quadrant analog multiplier with real compact structure. Therefore, some circuit performances of the proposed multiplier are successfully improved. In order to validate the circuit performances, the proposed multiplier has been simulated in PSPICE by using model parameter for 0.35 micron CMOS process. The results show that bandwidth, linearity and power consumption of the proposed circuit are better than those of the circuit in [8].

The remaining of this paper is organized in the following sections, a basic concept for realizing the analog multiplier is introduced in Section II. Next, a modification of square rooting circuit used to form an analog multiplier is described in Section III. The proposed multiplier circuit is illustrated in Section IV. In addition, simulated results of the proposed multiplier and conclusion are presented in Section V and VI, respectively.

II. BASIC CONCEPT

Realizing a proposed analog multiplier and the multiplier in [8] is based on a similar approach showing in Fig. 1. It comprises a pair of common source amplifier (M1 and M2), which acts as input transistors to provide output currents in term of squaring functions of input voltages (V_1 and V_2), and two identical voltage controlled square root blocks which operate as non-linear cancellation paths. Injecting the output currents of the input transistors into the square root blocks, a differential output current of the overall circuit will become a multiplication function of two input signals V_{12} and V_{34}. More detail of mathematical analysis using square-law relation of saturated MOSFET in strong inversion will be shown in the paragraph below.

Assuming the MOSFET M1 and M2 are biased in active region and neglecting channel length modulation effect, the current I_A and I_B can be respectively found as

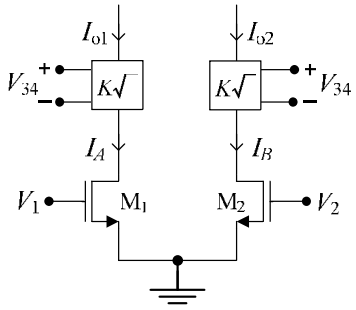

Figure 1. Basic concept for realizing a four quadrant analog multiplier.

$$I_A = \beta_n (V_1 - V_{tn})^2 \tag{1}$$

and

$$I_B = \beta_n (V_2 - V_{tn})^2, \tag{2}$$

where $\beta_n = 0.5\mu_n C_{ox}(W/L)$ is a transconductance parameter of each MOSFET and V_{tn} is the threshold voltage of NMOS transistor.

From (1) and (2), the relationship between the current I_A and I_B and the differential input voltage $V_{12} = V_1 - V_2$ can be given by

$$\sqrt{I_A} - \sqrt{I_B} = V_{12}\sqrt{\beta_n} \tag{3}$$

The drain currents I_A and I_B are fed into the square root blocks controlled by V_{34}, results in

$$I_{out} = I_{o1} - I_{o2} = KV_{34}\left(\sqrt{I_A} - \sqrt{I_B}\right) \tag{4}$$

where K is the gain of the square root blocks.

Substituting (3) into (4), yields

$$I_{out} = K\sqrt{\beta_n} V_{12} V_{34} \tag{5}$$

It can be seen that an output current appeared in (5) is in form of a multiplication function between two input signals V_{12} and V_{34}.

Based on this approach, both linear transconductor [9] and four-quadrant analog multiplier [10] have been proposed. Unfortunately, the early works in [9] and [10] require more than 3V for supply voltage which is not sufficiently low for modern analog design. Subsequently, a new square rooting circuit operated under 1.5V single supply was proposed in [11] which can be applied as a compact four quadrant analog multiplier as well [8]. However, the multiplier in [8] is not practical since it requires an ideal voltage reference to create the multiplication function.

In the next section, the improved square root circuit which is more suitable for realizing an analog multiplier will be described.

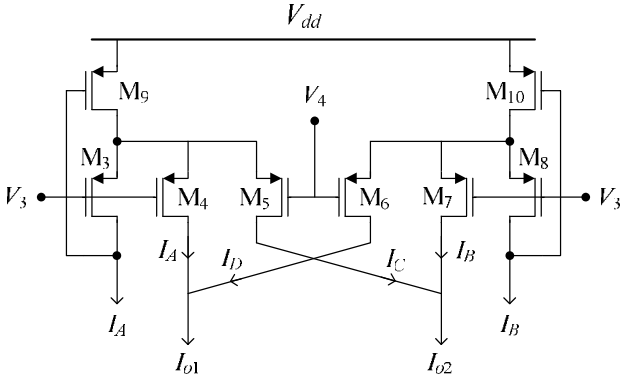

Figure 2. The proposed square rooting circuit.

III. SQUARE ROOTING CIRCUIT

A proposed square rooting circuit which is improved from [11] is shown in Fig.2. Using square-law relation of saturated MOSFET in strong inversion and setting M3-M8 to be identical, the currents I_C and I_D are found to be

$$I_C = \beta_p \left(V_{34} + \sqrt{\frac{I_A}{\beta_p}} \right)^2 \tag{6}$$

and

$$I_D = \beta_p \left(V_{34} + \sqrt{\frac{I_B}{\beta_p}} \right)^2, \tag{7}$$

where $\beta_p = 0.5\mu_p C_{ox}(W/L)$ is a transconductance parameter of each PMOS transistor and $V_{34} = V_3 - V_4$ is a differential control voltage.

Considering (6) and (7) in conjunction with the fact that $I_A + I_D = I_{o1}$ and $I_B + I_C = I_{o2}$ leading to

$$I_{o1} = \beta_p V_{34}^2 + 2V_{34}\sqrt{\beta_p}\sqrt{I_A} + I_A + I_B \tag{8}$$

and

$$I_{o2} = \beta_p V_{34}^2 + 2V_{34}\sqrt{\beta_p}\sqrt{I_B} + I_A + I_B \tag{9}$$

Subtracting (8) and (9), results in

$$I_{out} = I_{o1} - I_{o2} = 2V_{34}\sqrt{\beta_p}\left(\sqrt{I_A} - \sqrt{I_B}\right) \tag{10}$$

It is obvious that the output current of the improved square root circuit is a function of a square root of I_A and I_B and its gain can be adjusted by the voltage V_{34} and transconductance parameter β_p.

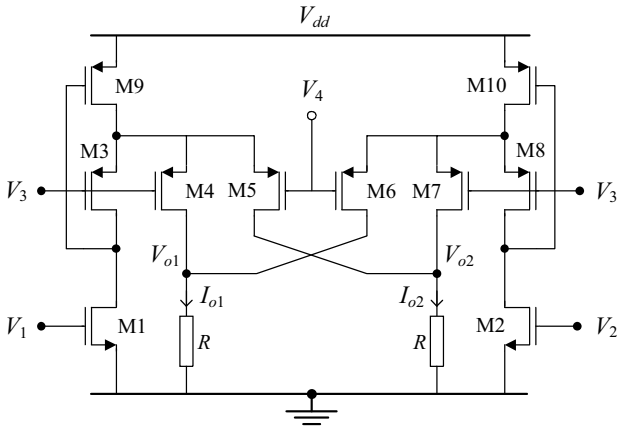

Figure 3. The proposed four quadrant analog multiplier circuit.

IV. Proposed Multiplier Circuit

Fig.3 shows the proposed multiplier circuit which is constituted by substituting the square rooting circuit in Fig. 2 into the square root blocks of Fig.1. Focusing on the differential output voltage we have found that

$$V_{out} = V_{o1} - V_{o2} = R\left(I_{o1} - I_{o2}\right), \tag{11}$$

Substituting (10) into (11), differential output voltage can be found as

$$V_{out} = 2RV_{34}\sqrt{\beta_p}\left(\sqrt{I_A} - \sqrt{I_B}\right) \tag{12}$$

Finally, substituting (3) into (12) yields

$$V_{out} = 2R\sqrt{\beta_n\beta_p}V_{12}V_{34} \tag{13}$$

Now, we have an output offset-free four quadrant analog multiplier and its gain can be adjusted by the load resistor R and the dimensions of each MOSFET.

V. Simulation Results

The multiplier circuit in Fig. 3 was designed and simulated by using PSPICE for 0.35 micron CMOS process parameter with main parameters $V_{tn} \cong 0.51$ and $V_{tp} \cong -0.66$. The input voltage V_{12} and V_{34} are set to be balance with common mode voltages of $V_{C1} = 1$V and $V_{C2} = 0.2$V, respectively and supply voltage V_{DD} is set at 1.8V. Transistor dimensions are listed in Table 1. Trying to avoid channel length modulation and short channel effects, the channel lengths of all transistors are set to be two times longer than 0.35 micron. The load resistors R are chosen to be 2.5 kΩ. At the quiescent point, power consumption of the proposed multiplier is 165 μW.

Fig. 4 shows simulated DC transfer characteristics of the proposed multiplier, when V_{12} was swept continuously from -0.4V to 0.4V while V_{34} was varied from -0.4V to 0.4V with 0.1V step size. It can be observed that the linear range of V_{12} is approximately ±0.4V.

Transient response of the multiplier operated as amplitude modulator is shown in Fig. 5. A 0.4V, 25 kHz sinusoidal carrier signal V_{12} shown in Fig. 5(a) was multiplied by a 0.4V, 1 kHz sinusoidal modulating signal V_{34} shown in Fig. 5(b). A resulting waveform is shown in Fig. 5(c).

Frequency response of the multiplier for various gains was set by sweeping V_{34} from 0.1V to 0.4V with 0.1V step size as the same condition of DC sweep and the results show in Fig. 6 demonstrating that bandwidth of the proposed circuit is higher than 110 MHz for all gains.

Circuit linearity is examined by simulated total harmonic distortion (THD), when V_{34} was fixed at 0.4V and applying various amplitudes of 25 kHz sinusoidal V_{12}. The result is displayed in Fig. 7 that less than 0.6% THD is achieved for V_{12} amplitude about 0.4V.

Comparative results of the simulated performances between this work and [8] are shown in table II.

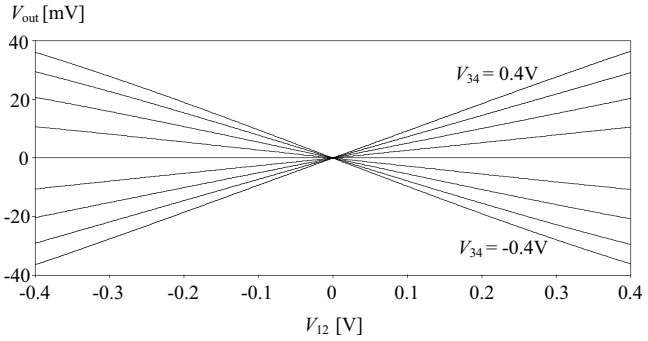

Figure 4. DC transfer characteristics.

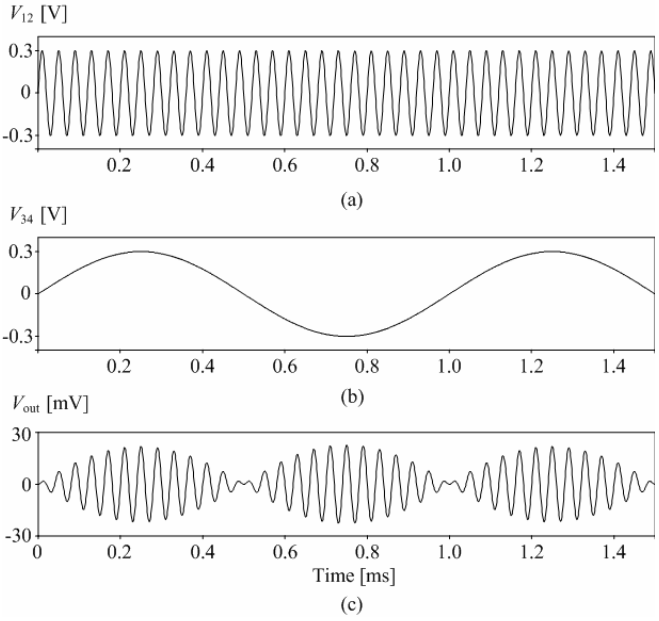

Figure 5. Output waveforms
(a) V_{12} sinusoidal carrier signal (b) V_{34} sinusoidal modulating signal
(c) Output waveform of amplitude modulator

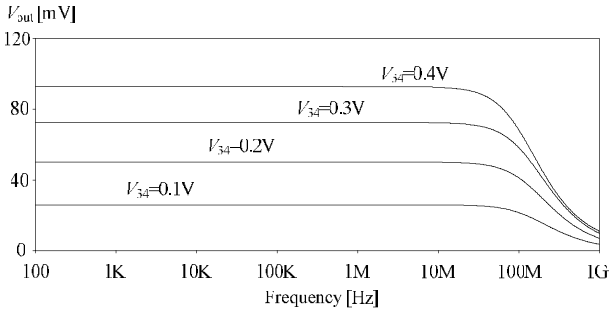

Figure 6. Frequency response.

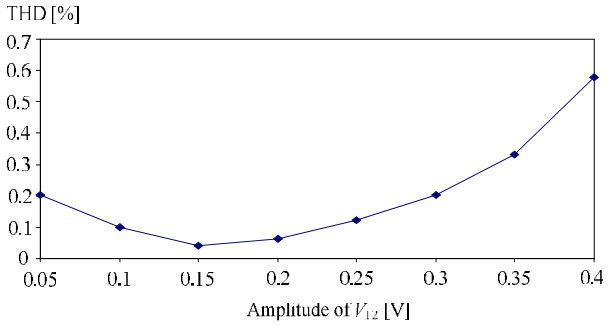

Figure 7. Simulated total harmonic distortion.

TABLE I
TRANSISTOR DIMENSION

Transistor	W [μm]	L [μm]
M1-M2	1	1
M3-M8	3.5	1
M9-M10	40	1

TABLE II
Comparison of simulated characteristics between the proposed multiplier and the multiplier in [8]

Multiplier characteristic	Proposed	Ref. [8]
Power consumption [μW]	165	200
THD [%] *	≅ 0.6	≅ 0.8
-3 dB Bandwidth [MHz]	>110	>10
Total physical area [μm]^2 **	103	672

* V_{34} was fixed at 0.4V and V_{12} is a 25 kHz sinusoidal signal with amplitude of 0.4V
** roughly estimated from transistor dimensions

VI. CONCLUSION

A new square rooting circuit can be used for realizing a CMOS four-quadrant analog multiplier has been presented. The resulting multiplier circuit is improved to be more compact than the previous work. The extra voltage reference is not required for the proposed circuit. As a result, the proposed multiplier provides high bandwidth, high linearity and low static power consumption. Simulation results are given to verify the multiplier circuit performances.

ACKNOWLEDGMENT

The authors would like to thank C. Sawigun for useful suggestion and discussion.

REFERENCES

[1] S. Yan and E. Sanchez-Sinencio, "Low Voltage Analog Circuit Design Techniques: A Tutorial," *IEICE Trans. Analog Integrated Circuits and Systems*, vol. E00-A, no. 2, pp. 1-8, Feb. 2000.

[2] G. Han and E. Sanchez-Sinencio, "CMOS Transconductance Multipliers: A Tutorial," *IEEE Trans. Circuits Syst. II*, vol. 45, no. 12, pp. 1550-1563, Dec. 1998.

[3] B. Maundy and M. Maini, "A Comparison of Three Multiplier Based on the V_{gs}^2 Technique for Low-Voltage Applications," *IEEE Trans. Circuits Syst. I*, vol. 50, no. 7, pp. 937-940, Jul. 2003.

[4] R. G. Cavajal, J. Ramirez-Angulo, A. J. Lopez Matin, A. Torralba, J. A. Gomez Galan, A. Carlosena, and F. M. Chavero, "The flipped voltage follower: a useful cell for low-voltage low-power circuit design," *IEEE Trans. Circuits Syst. I*, 2005, 52,(7), pp. 1276-1291.

[5] J. Ramirez-Angulo, R.G. Carvajal, and J. Martinnez-Heredia, "1.4V supply, wide swing, high-frequency CMOS analogue multiplier with high current efficiency," *Proc IEEE ISCAS*, May 2000, Geneva Switzerland, Vol. V, pp. 553-536.

[6] A. Demosthenous, and M. Panovic, "Low voltage MOS linear transconductor/squarer and four-quadrant multiplier for analog VLSI," *IEEE Trans on Cir. and Syst. I: Regular paper*, vol. 52, no. 9, pp. 1721-1731, 2005.

[7] C. Sawigun, and J. Mahattanakul, "A low voltage CMOS linear transconductor suitable for analog multiplier application," *Proc. IEEE ISCAS'06*, pp. 1543-1546, KOS, Greece, 2006.

[8] C. Sawigun and A. Demosthenous, "Compact low voltage CMOS four quadrant analog multiplier," *Electronics Letters*, vol. 39, no. 25, pp. 1771-1772 , Sep. 2006.

[9] J. Mahattanakul and C. Toumazou, "Independent control of transconductance gain and input linear range in a MOS linear transconductance amplifier," *Electronics Letters*, vol. 32, no. 18, pp. 1629-1630 , Aug. 1996.

[10] A. Hyogo, Y. Fukutomi and K. Sekine, "Low voltage four quadrant analog multiplier using square-root circuit based on CMOS pair," *Proc. of IEEE ISCAS'99*, pp. II 274-277, 1999.

[11] C. Sawigun, N. Kiatwarin and W. Ngamkham, "A low voltage MOS linear transconductor with constant input linear range," *ECTI 2006*, vol. 1, pp. 167-170, Ubon Ratchathani, Thailand, 2006.