CHAPTER ONE

Circuit and System Fundamentals

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1.1.0. INTRODUCTION

The formulation of meaningful analytical procedures and design strategies for even the most advanced of electronic feedback circuits and systems relies on a thorough grasp of basic circuit and system concepts. Aside from abilities to apply and interpret the Kirchhoff voltage and current laws (KVL and KCL) in both the time and frequency domains, at least three issues underpin the mission of acquiring design-oriented analytical proficiency in the electronic circuits arena. The first of these is the theorems attributed to Thévenin and Norton. An ability to apply these theorems to the problems of exploring and understanding the electrical dynamics of electronic networks that couple specified signal sources to an arbitrary linear or nonlinear load is a virtual cornerstone of the electronic networks discipline. For example, Thévenin's and Norton's theorems might be gainfully applied to deduce the desired input/output (I/O) electrical characteristics of a preamplifier designed for insertion between the output terminals of a compact disc player and the input terminals of the power amplifier used to drive the audio speakers of a stereo system.

A second issue embraces transfer functions of linear networks. The capability of deducing the transfer characteristic and casting it into appropriate mathematical form serve a multitude of purposes. Included among these purposes are a delineation of the input to output gain of the network undergoing investigation, the determination of the network input and output impedances, an assessment of the relative stability of the system, and the determination of the time domain response of the subject circuit to specified transient and steady state input excitations. Phasor analyses in the sinusoidal steady state, which is fundamental to a stipulation of the manner in which the system gain and pertinent impedance levels depend on the frequency of the applied input signal, are intimately linked to network transfer functions. Phasors comprise the basis for deducing such electronic circuits and systems performance metrics as bandwidth, impedances, frequency response, and phase response. The bandwidth defines the frequency interval over which the I/O gain is maintained nominally constant. The impedance levels at the input and output terminals of an active network are instrumental in determining whether an amplifier is more suitable for voltage than for current amplification. The frequency response is essentially a mathematical snapshot of the manner in which the network under consideration performs over specified intervals of signal frequency. Finally, the phase response establishes the network delay, which defines the average time required by a system to process and ultimately deliver the desired steady state output response to a specified input signal.

The third issue is the intelligent use of the four types of dependent generators; namely, the voltage controlled current source (VCCS), the voltage controlled voltage source (VCVS), the current controlled current source (CCCS), and the current controlled voltage source (CCVS). Understanding the volt-ampere properties of these mathematical circuit branch elements is a prerequisite to formulating reasonably accurate, design-oriented, linearized circuit models for active devices, such as the metal-oxide-semiconductor field-effect transistor (MOSFET), the bipolar junction transistor (BJT), and the PN junction diode. Moreover, the facility to exploit these properties prudently and creatively is fundamental to the intelligent application of Thévenin's and Norton's theorems and to the efficient deduction of the transfer characteristics of electronic systems.

In an attempt to vector the interested reader on a path toward ultimate electronic circuit design proficiency, the foregoing and a few related other concepts indigenous to basic circuit theory are reviewed and exemplified in this chapter. These reviews and illustrations serve to

introduce the reader to an interesting and even perplexing paradox that underpins the genuinely difficult task (some might even argue art) of creative and innovative electronic circuit and system design. In particular, the fundamental purpose of circuit analysis is not the precise disclosure of either a circuit response or a specific circuit performance metric. Instead, analyses are conducted to gain an insightful understanding of the limitations and attributes of the time and frequency domain electrical dynamics pervasive of a circuit architecture deemed plausible for the design mission. As such, these design-oriented analyses respond to the time-honored adage that nothing should ever be built until that which is to be built is thoroughly understood.

Design-oriented engineering analysis is not a trivial undertaking because design itself is neither trivial nor straightforward. Design is a challenging undertaking because it is not the problem of finding the N solutions to a system of N equations in N unknowns. The most typical design problem is one in which there are more specifications that must be satisfied or more variables that need to be determined than there are independent equations that can be written. Basic algebra teaches that a problem for which the number of unknowns does not match the number of available independent equations has no unique solution. Since poorly structured mathematical problems are implicit to virtually all design environments, unique design solutions rarely prevail. Nevertheless, viable and even creative solutions can be determined. The best of these solutions, in the sense of yielding reliable, manufacturable, and cost effective electronic networks that meet operating specifications, are rarely forged by trial and error strategies. Instead, optimal solutions derive from fundamental phenomenological understanding. The task necessarily preceding such understanding is the conduct of thorough mathematical and computer-based analyses that insightfully highlight both the attributes and the limitations of the circuit and system architectures under consideration. The satisfying understanding that supports the completion of a design project ensues when analytical disclosures can be creatively interpreted and lucidly explained in terms of fundamental physical laws, basic circuit and system theories, and simple mathematical models.

1.2.0. THÉVENIN'S AND NORTON'S THEOREMS

Consider the system in Figure (1.1a), which abstracts two terminals of a generalized linear network coupled to a load branch. Since the subject network is stipulated as a linear entity, its intrinsic branch elements are exclusively linear resistors, linear capacitors, linear inductors, and linear controlled voltage and current sources. Although no sources of energy are presumed embedded in the structure, any number of independent energy sources can be applied. To this end and without loss of generality, two independent inputs –a voltage source, V_s, and a current source, I_s,– are depicted. It should be understood that the presumption of no intrinsic energy sources implies at least one of three possible operational circumstances. In particular, the internal capacitors and inductors may have zero initial voltages and currents, respectively, at the time at which the indicated input sources, V_s, and I_s, are applied. Alternatively, it may be that analytical interest focuses on only the steady state performance of the system. Accordingly, the effects of initial capacitive and inductive energies have dissipated and no longer possess engineering significance. A third possibility is that initial capacitor voltages and inductor currents are treated as additional independently applied input excitations, similar to the signal sources, V_s, and I_s. In the present circumstance, it is tacitly assumed that analytical attention focuses exclusively on steady state electrical characteristics.

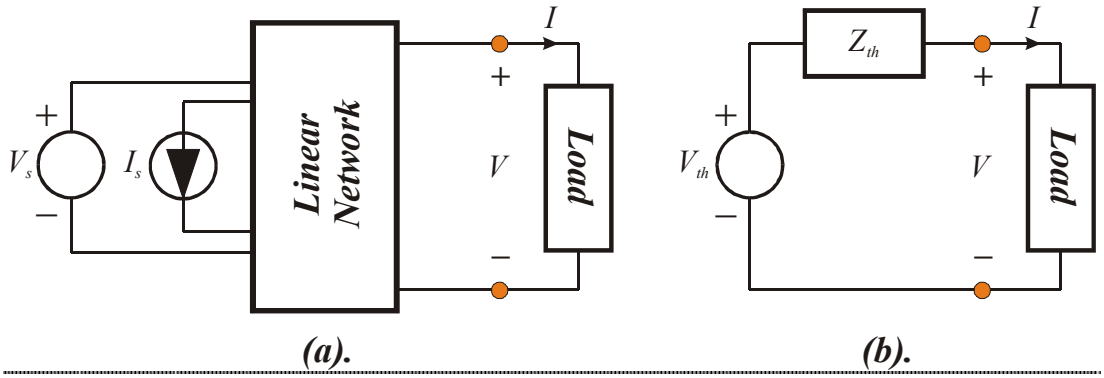


Figure (1.1). **(a).** A Linear Network Driving An Arbitrary Load And Excited By An Independent Voltage Source, V_s, And An Independent Current Source, I_s. **(b).** The System In (a) With The Linear Network Supplanted By Its Thévenin Equivalent Circuit Consisting Of A Voltage Source, V_{th}, Connected In Series With An Impedance Z_{th}.

Thévenin's theorem states that the electrical characteristics at any port (or terminal pair) of a linear electrical network can be modeled by a voltage source in series with an impedance, as suggested by Figure (1.1b). The indicated voltage source, V_{th}, is termed the ***Thévenin voltage*** of the port undergoing scrutiny, while the subject series impedance, Z_{th}, is known as the ***Thévenin impedance*** of said port. If the port at which Thévenin's theorem is applied happens to be the output port of the network where signal responses to applied input excitations are to be delivered, the Thévenin impedance is also known as the network ***output impedance***. When V_{th} and Z_{th} are correctly measured or calculated, the Thévenin equivalent circuit, or Thévenin model, "seen" by the load establishes a load voltage, V, and a load current, I, that are respectively identical to the load voltage and current supported by the original system in Figure (1.1a). It is important to underscore the fact that the foregoing assertions are independent of the nature of the load connected to the network port undergoing a Thévenin investigation. This is to say that the load at hand can be a passive, an active, a linear, or even a nonlinear electrical branch.

An alternative to Thévenin's theorem is Norton's theorem, which stipulates that any port of a linear electrical network can be represented as a current source in shunt with an impedance, as suggested by Figure (1.2). The current source, I_n, is termed the ***Norton current*** of the port undergoing scrutiny. The associated shunt impedance, which can be termed the ***Norton impedance***, is, at risk of deflating Norton's ego, identical to the Thévenin impedance introduced in Figure (1.1b).

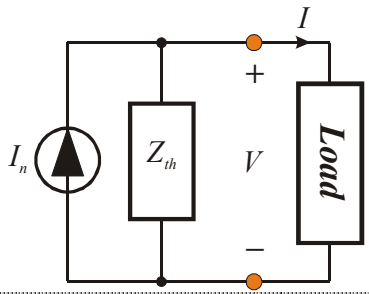


Figure (1.2). The Norton Equivalent Circuit For The System Given In Figure (1.1a). As In The Case Of The Thévenin Model In Figure (1.1b), The Norton Circuit Delivers A Load Voltage, V, And A Load Current, I, That Are Respectively Identical To the Load Voltage And Load Current Observed In The Original System.

The topological simplicity of both the Thévenin and Norton models obscures their actual significance and engineering utility. An initial appreciation of these models can be garnered from the realization that the linear networks they represent can be large, intricate circuits comprised of hundreds thousands of interconnected electrical branch elements. But architectural complexity notwithstanding, only two elements –voltage source and impedance in the case of Thévenin and current source and impedance in the case of Norton– are required for the unique determination of the voltage and corresponding current associated with an appended load. In short, it is likely easier to analyze the model in either Figure (1.1b) or in Figure (1.2) than it is to analyze the entire electrical system abstracted in Figure (1.1a). The downside to this Thévenin or Norton analytical tack is that the replacement of the original system by either of the models shown in Figures (1.1b) or (1.2) leads to an irretrievable loss of branch voltage, branch current, and branch power information within the linear network. In most electronic circuit and system applications, this loss of information is an acceptable consequence of the expediency with which the load voltage, current, and power can be determined in terms of Thévenin or Norton parameters. In a few cases, such loss of information may prove unacceptable. For example, in some design environments, it may be essential to understand how nonzero network element tolerances or other manufacturing uncertainties deleteriously affect the ability of a linear network to establish and sustain required load voltage and current characteristics.

The Thévenin and Norton equivalent circuits are two distinctly different circuit topologies that serve to model any considered linear electrical system. Questions therefore naturally arise as to why two modeling approaches need be advanced when one model appears to suffice. To be sure, either a Thévenin or a Norton representation can be used to model a port of any linear network. Given the widespread analytical comfort levels associated with voltage sources, it is hardly surprising that the Thévenin equivalent circuit enjoys wider popularity than does its Norton counterpart. But in fact, some network ports are more amenable to Thévenin modeling, while others are more appropriate to Norton modeling. In idealized operating circumstances, it is even possible to encounter a network port for which Thévenin parameters can be calculated or measured, but Norton parameters are not deterministic, and vice versa. For example, and as is demonstrated in the following subsection of material, the Norton current is indeterminate for a network port whose Thévenin impedance is zero. In this case, only a Thévenin equivalent circuit can be meaningfully contrived and, as Figure (1.3a) illustrates, the subject network port emulates the volt-ampere characteristics of an ideal voltage source. On the other hand, the Thévenin voltage of a network port having infinitely large Thévenin impedance cannot be determined, which accordingly forces a Norton representation of said port. In this case, the network port at hand behaves as the ideal current source depicted in Figure (1.3b). A general extrapolation of the foregoing two statements is that a network port characterized by a small Thévenin impedance behaves as an approximate ideal voltage source and is therefore prudently modeled by a Thévenin equivalent circuit. On the other hand, a linear network port that emulates idealized current source characteristics by virtue of its large Thévenin impedance is best represented by a Norton equivalent circuit.

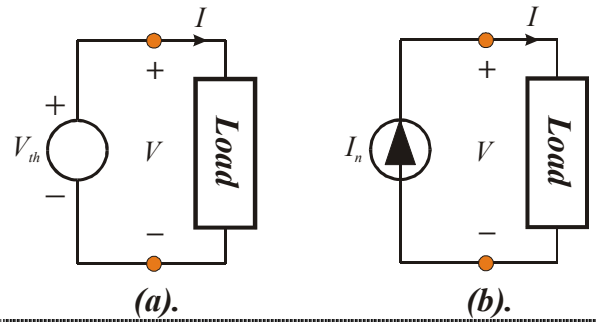


Figure (1.3). **(a).** The Thévenin Equivalent Circuit Of A Loaded Linear Network Port Whose Thévenin Port Impedance Is Zero. The Port In Question Behaves As An Ideal Voltage Source. **(b).** The Norton Equivalent Circuit Of A Loaded Linear Network Port Whose Thévenin Port Impedance Is Infinitely Large. The Port In Question Behaves As An Ideal Current Source.

1.2.1. THÉVENIN AND NORTON PARAMETERS

The experimental determination or analytical evaluation of the Thévenin parameters commences by noting in Figure (1.1b) that the load voltage, V, is

$$V = V_{th} - Z_{th} I \,, \tag{1-1}$$

where I is obviously the current supplied by the network and conducted by the load connecting to, or terminating, the network port undergoing scrutiny. The fact that the Thévenin equivalent circuit is independent of the nature of the load encourages the exploitation of specific loads that facilitate the direct determination of the Thévenin voltage, V_{th}. To this end, if the actual load were to be supplanted by an open circuit, as shown in Figure (1.4a), current I is necessarily reduced to zero, which renders $V \equiv V_{th}$ in (1-1). In other words, the Thévenin voltage of a linear network port is the voltage established at that port when said port is open circuited. This observation explains the common reference to a Thévenin voltage as an ***open circuit voltage***.

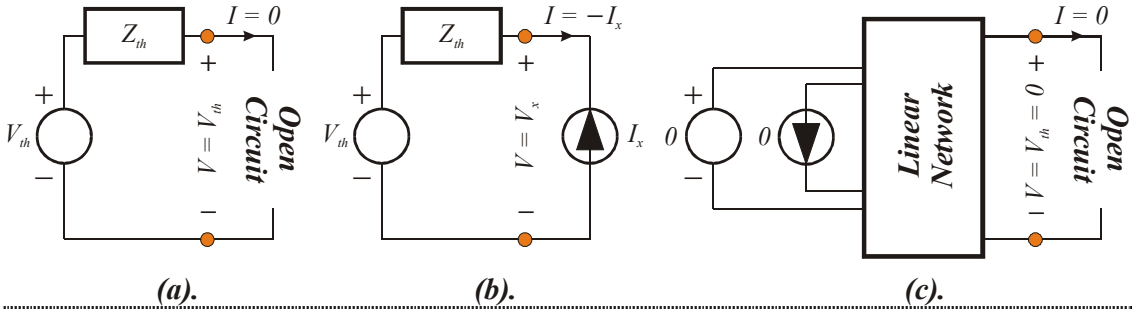


Figure (1.4). **(a).** The Calculation Of The Thévenin Equivalent Voltage At A Port Of A Linear Network. **(b).** The Ohmmeter Method Of Evaluating The Thévenin Equivalent Impedance. **(c).** The Strategy For Realizing Zero Thévenin Equivalent Voltage. Zero Thévenin Voltage Expedites The Ohmmeter Method Of Computing The Thévenin Equivalent Impedance.

Consider now the case in which the original load is replaced by an ideal current source of value I_x, as is depicted in Figure (1.4b). The resultant network current is $I = -I_x$, and if V_x denotes the value of port voltage V corresponding to the applied current load, (1-1) delivers

$$\frac{V_x}{I_x} = Z_{th} + \frac{V_{th}}{I_x}, \tag{1-2}$$

where it is important to note that voltage V_x is in disassociated polarity reference to current I_x. It would be delightful if V_{th} could be constrained to zero under the stipulated load current source constraint. In this event, the ratio of the current source voltage, V_x, -to- the current source current, I_x, is the Thévenin impedance, Z_{th}, in need of evaluation. The strategy for effecting null V_{th} in a physically sound sense derives from classic ***superposition theory***, which applies to all linear networks. In particular, recall from Figure (1.1a) that the network undergoing study is excited by two sources of independent energy; namely, voltage V_s and current I_s. Superposition theory states that any branch voltage or any branch current of any linear electrical system, which certainly embraces a linear network under the condition of a linear load termination that happens to be a constant current source, is the algebraic superposition of the effects of all applied independent sources of voltage and current. It follows that

$$V_{th} = A_{st}V_s + Z_{st}I_s, \tag{1-3}$$

where A_{st} and Z_{st} are understood to be constants (perhaps frequency dependent constants), independent of V_s and I_s. Obviously, V_{th} is zero if the applied signal energies are nulled, as is highlighted in the abstraction of Figure (1.4c). Thus, the Thévenin impedance at a network port can be determined as the ratio of a voltage, V_x, established in response to an applied load current, I_x, -to- I_x, under the special circumstance of all independently applied signal sources set to zero.

The procedure advanced for Thévenin impedance calculation effectively mirrors the operation of an ohmmeter used to measure the resistance between two electrical terminals. It might therefore be termed the ***ohmmeter method*** of impedance computation. At risk of inadvertently depressing the reader, there is no such beast as an ohmmeter. The ohmmeters commonly found in the laboratory are actually electronic systems that perform two functions when its leads are connected to a terminal pair of interest. The first function is the injection of a current (I_x) that is sufficiently small to preclude any significant electrical perturbation of the network undergoing characterization. In strictly linear networks, such as those considered in this discussion, superposition renders the actual value of I_x immaterial. In nonlinear structures, such as transistors or batteries, the value of I_x is so crucial as to render a conventional ohmmeter ineffective for resistance evaluation. The second function performed by the ohmmeter is the monitoring of the resultant voltage (V_x) established at the port to which the current is applied. The reading observed on the ohmmeter is actually this voltage scaled to the applied current (V_x/I_x) and hence, it is the resistance evidenced at the port in question.

The determination of the Norton current, I_n, like the evaluation of the Thévenin voltage, relies on the fundamental fact that the parameters of the Norton equivalent circuit are independent of the load termination. If, therefore, the load appearing in Figure (1.2) is replaced by an electrical short circuit, as indicated in Figure (1.5), it is clear the that resultant current, I, flowing through the short circuited load is identical to I_n. It follows that in general, the Norton current of linear network port is the current supplied by that port to a short-circuited termination. Not surprisingly, the Norton current is often referred to as a ***short circuit current***. And like V_{th}, I_n is the superposition of the effects of the applied input signal energies. With reference to Figure (1.1a),

$$I_n = Y_{sn}V_s + A_{sn}I_s, \tag{1-4}$$

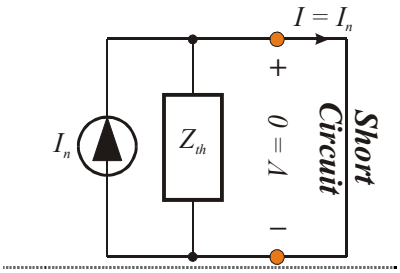


Figure (1.5). Calculation Of The Norton Equivalent Current At A Port Of A Linear Network.

where Y_{sn} and A_{sn} are constants that are independent of applied signal voltage, V_s, and applied signal current, I_s.

1.2.2. ENGINEERING OBSERVATIONS

Three useful and interesting sidebars ensue from the foregoing considerations. The first and most obvious of these is that the Thévenin equivalent circuit of the system in Figure (1.1a) can, by virtue of Figure (1.1b) and (1-3), be drawn in the topological format of Figure (1.6a). In this diagram, parameter A_{st} is a dimensionless parameter that represents the voltage transfer function, or voltage gain, from the port at which V_s is incident -to- the port that is terminated in the considered load. As such, A_{st} might logically be termed the system ***Thévenin voltage gain*** or equivalently, the system ***open circuit voltage gain***. On the other hand, parameter Z_{st} has units of ohms and is the ***Thévenin transimpedance***, or ***open circuit transimpedance***, evidenced between the port at which signal current I_s is applied and the load port. In other words, the transimpedance, like any impedance function, is a voltage -to- current ratio; it is literally the transfer impedance measured from the port of source current application -to- the load voltage response. A second, related observation is that because of (1-4), the Norton equivalent circuit in Figure (1.2) can be delineated as the structure offered in Figure (1.6b). In this case, parameter A_{sn} is dimensionless and symbolizes the ***Norton current gain***, or ***short circuit current gain***, between the applied signal source current, I_s, and the load port at which voltage V is established. On the other hand, Y_{sn}, which has units of mhos, is the ***Norton transadmittance***, or ***short circuit transfer admittance***, from the port at which signal voltage V_s is applied and the load port that conducts current I. Collectively, both of the models in Figure (1.6) underscore the fact that the Thévenin voltage and Norton current at a network port are respectively the superimposed effects of the energy sources applied to the network undergoing examination. They also highlight the various transfer relationships that link the Thévenin load voltage and the Norton load current to input signal energies.

The third observation derives from the explicit requirement that the Thévenin and Norton equivalent circuits applied to a given network port must each produce identical load voltage and current results under actual load termination conditions. In other words, one engineer using the Thévenin model and another using the Norton equivalent circuit must each compute the same load voltage and current responses. This necessity means that the Thévenin voltage, V_{th}, and the Norton current, I_n, are not independent variables. In order to arrive at the relationship between V_{th} and I_n, consider the model in Figure (1.1b) under the special circumstance of a short-circuited load, as depicted in Figure (1.7a). By definition, the resultant load current, I, is the short circuit, or Norton load current, I_n, which is

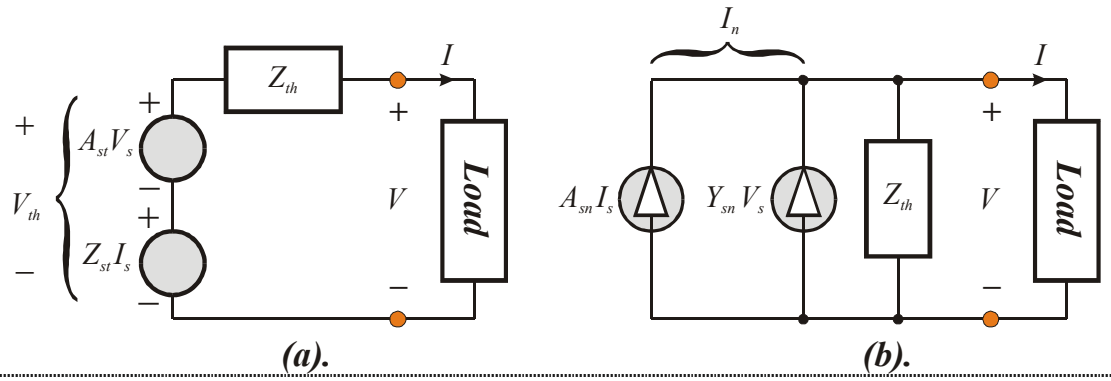


Figure (1.6). **(a).** Alternative Form Of The Thévenin Equivalent Circuit For The Linear Network Of Figure (1.1a). The Thévenin Voltage Is Cast Explicitly In Terms Of The Open Circuit Voltage Gain, A_{st}, And The Open Circuit System Transimpedance, Z_{st}. **(b).** Alternative Form Of The Norton Equivalent Circuit For Figure (1.1a). The Norton Current Is Cast In Terms Of The Short Circuit System Current Gain, A_{sn}, And The Short Circuit System Transadmittance, Y_{sn}.

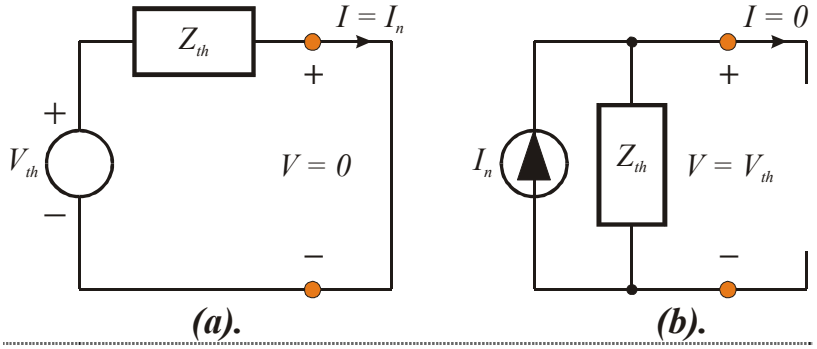


Figure (1.7). **(a).** The Thévenin Equivalent Circuit Of A Linear Network Port Terminated In A Short Circuited Load. **(b).** The Norton Equivalent Circuit Of A Linear Network Port That Is Open Circuited.

$$I \equiv I_n = \frac{V_{th}}{Z_{th}}. \tag{1-5}$$

This elegantly simple result shows that the Norton current at a port of a linear electrical network is nothing more than the ratio of the Thévenin voltage -to- the Thévenin impedance at said port. The application of the Norton model in Figure (1.2) to the special case of an open circuited load shown in Figure (1.7b) delivers a consistent result. Specifically, the open circuit load voltage V, which is now identical to the Thévenin voltage, V_{th}, "seen" by the load, is

$$V_{th} = Z_{th}I_n\,, \tag{1-6}$$

for which an understanding with respect to (1-5) assuredly instills pride in your high school algebra teachers.

EXAMPLE #1.1:

The circuit appearing in Figure (1.8) is the linearized model of a bipolar junction transistor (BJT) voltage buffer, which is otherwise known as an emitter follower. The applied signal source is represented as a Thévenin equivalent circuit consisting of the series interconnection of a signal voltage, V_s, and a signal source

resistance, R_s. The output signal voltage is V_o, which is taken as the voltage developed across a load capacitance of value C_l. Determine expressions for the Thévenin voltage, V_{th}, seen by the capacitive load, the Thévenin resistance, R_{th}, facing this load, and the transfer function, $A_v(s) = V_o(s)/V_s(s)$. As a demonstration of the utility of the Thévenin analytical approach to evaluating the performance of an electronic network, examine the voltage transfer function from the perspective of determining the *3-dB* bandwidth, ω_b, and plotting the frequency response of the amplifier. Numerically evaluate the Thévenin voltage gain, A_{st}, the Thévenin resistance, and the *3-dB* bandwidth for transistor parameters of r_b = *200 Ω*, r_π = *2 KΩ*, r_o = *50 KΩ*, and β = *120 amps/amp*. Additionally, take R_s = *300 Ω*, R_l = *3 KΩ*, and C_l = *10 pF*.

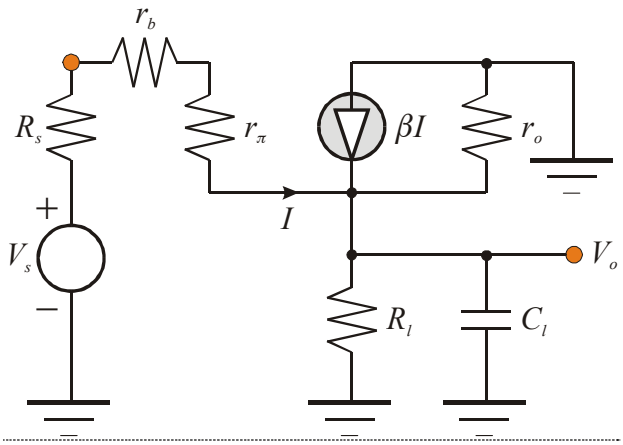


Figure (1.8). Linearized Model Of A Bipolar Junction Transistor Emitter Follower.

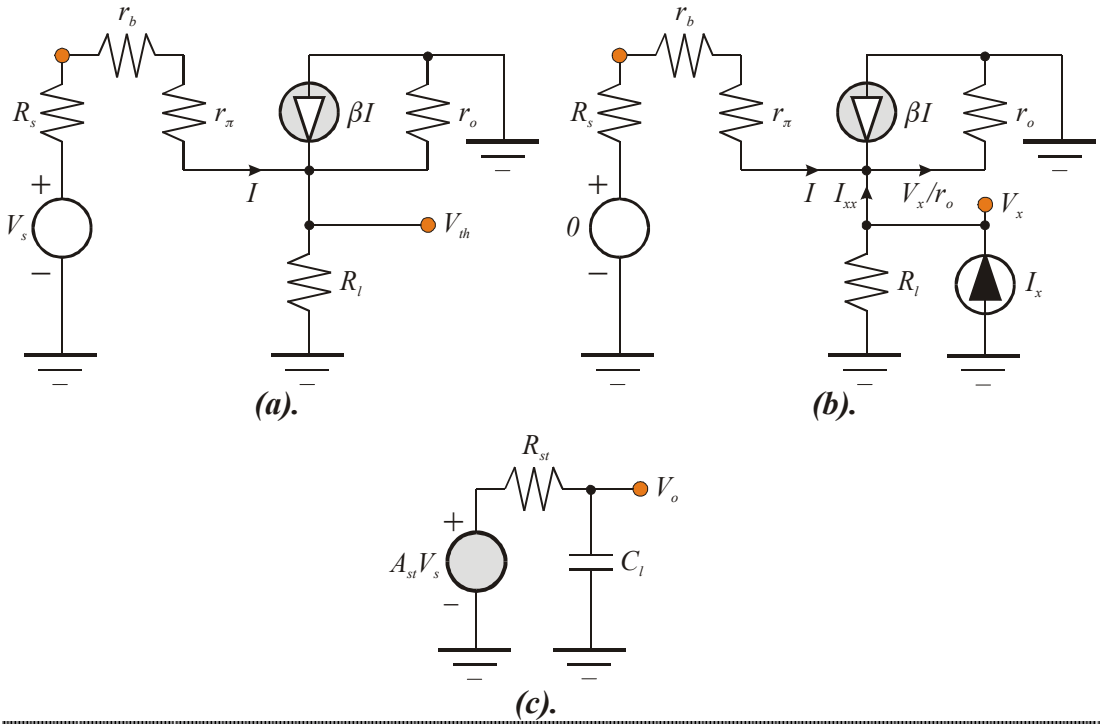


Figure (1.9). **(a).** Equivalent Circuit Used To Evaluate The Thévenin Voltage Seen By The Capacitance, C_l, In Figure (1.8). **(b).** Equivalent Circuit Used To Evaluate The Thévenin Resistance Seen By The Capacitance, C_l, In Figure (1.8). **(c).** Thévenin Equivalent Circuit Pertinent To The Output Port Of The Amplifier In Figure (1.8).

SOLUTION #1.1:

(1). Figure (1.9a) is the circuit diagram appropriate to the computation of the Thévenin voltage, V_{th}, established at the capacitive load port. Note in this diagram that the capacitive load branch has been removed; that is, the load has been open circuited. The resultant branch currents have been identified in this circuit diagram to appease Kirchhoff. Observe that the current, I, which controls the dependent current source, βI, is expressible as

$$I = \frac{V_s - V_{th}}{R_s + r_b + r_\pi} . \tag{E1-1}$$

A conventional nodal analysis then yields

$$\frac{V_{th}}{R_l} + \frac{V_{th}}{r_o} - (\beta + 1) I = \frac{V_{th}}{R_l} + \frac{V_{th}}{r_o} - \frac{(\beta + 1)(V_s - V_{th})}{R_s + r_b + r_\pi} = 0 , \tag{E1-2}$$

from which the Thévenin voltage computes to be

$$\boxed{V_{th} = \left[\frac{(\beta + 1)(r_o \| R_l)}{R_s + r_b + r_\pi + (\beta + 1)(r_o \| R_l)} \right] V_s .} \tag{E1-3}$$

As a check on the propriety of (E1-3), note that $\beta = 0$ in Figure (1.9a) eliminates the current controlled current source, βI. Since resistance r_o is clearly in parallel with resistance R_l, it is hardly surprising that (E1-3) reduces to the simple voltage divider expression,

$$V_{th} = \left[\frac{(r_o \| R_l)}{R_s + r_b + r_\pi + (r_o \| R_l)} \right] V_s . \tag{E1-4}$$

(2). The circuit diagram used to determine the Thévenin resistance, R_{th}, seen by the load capacitance, C_l, in Figure (1.8) is provided in Figure (1.9b), where the independent signal voltage, V_s, applied to the original circuit has been nulled. It is evident that the "ohmmeter" current, I_x, relates to the "ohmmeter voltage," V_x, in accordance with

$$I_x = \frac{V_x}{R_l} + I_{xx} = \frac{V_x}{R_l} + \frac{V_x}{r_o} - (\beta + 1) I , \tag{E1-5}$$

where current I is now

$$I = - \frac{V_x}{R_s + r_b + r_\pi} . \tag{E1-6}$$

Upon combining these two relationships, the pertinent Thévenin resistance is found to be

$$\boxed{R_{th} = \frac{V_x}{I_x} = (R_l \| r_o) \left\| \left(\frac{r_\pi + r_b + R_s}{\beta + 1} \right) \right. .} \tag{E1-7}$$

For $\beta = 0$, this solution collapses to the expected result of a parallel combination of three effective circuit resistances; namely, the load resistance, R_l, the transistor model resistance, r_o, and the net resistance comprised of the series interconnection of resistances r_π, r_b, and R_s.

(3). From the solution for the Thévenin voltage in Step (1) above, the Thévenin voltage gain, A_{st}, is

$$A_{st} = \frac{V_{th}}{V_s} = \frac{(\beta + 1)(r_o \| R_l)}{R_s + r_b + r_\pi + (\beta + 1)(r_o \| R_l)} . \tag{E1-8}$$

The resultant model for the evaluation of the overall voltage gain of the emitter follower is shown in Figure (1.9c). This simple model readily produces an overall gain expression of

$$\boxed{A_v(s) = \frac{V_o(s)}{V_s(s)} = \frac{A_{st}\left(1/sC_l\right)}{R_{th} + 1/sC_l} = \frac{A_{st}}{1 + sR_{th}C_l}.} \qquad \text{(E1-9)}$$

It is appropriate to interject that the product, $R_{th}C_l$, is the ***time constant*** attributed to the capacitance, C_l. In general, it can be stated that the time constant associated with a capacitor in a linear network is the product of said capacitance and the Thévenin resistance faced by the subject capacitor.

(4). In the laboratory, the amplifier at hand might very well be characterized under steady state sinusoidal operating conditions. With sinusoidal excitation, the steady state response derives from replacing the Laplace operator, s, in the preceding result by the imaginary frequency variable, $j\omega$. Thus,

$$A_v(j\omega) = \frac{V_o(j\omega)}{V_s(j\omega)} = \frac{A_{st}\left(1/j\omega C_l\right)}{R_{th} + 1/j\omega C_l} = \frac{A_{st}}{1 + j\omega R_{th}C_l}, \qquad \text{(E1-10)}$$

for which the magnitude of gain is

$$\left|A_v(j\omega)\right| = \left|\frac{V_o(j\omega)}{V_s(j\omega)}\right| = \left|\frac{A_{st}}{1 + j\omega R_{th}C_l}\right| = \frac{\left|A_{st}\right|}{\sqrt{1 + \left(\omega R_{th}C_l\right)^2}}. \qquad \text{(E1-11)}$$

Note that for very small radial signal frequencies, ω, the voltage transfer function is approximately constant, independent of frequency. On the other hand, large ω incurs a reduced magnitude of transfer function and thus, a degraded gain. Indeed, infinitely large ω results in zero gain magnitude. Such a transfer function characteristic is indicative of a ***lowpass network***; that is, a network capable of passing with minimal gain reduction, or with minimal attenuation, low signal frequencies from its input -to- its output port, but incapable of processing very large frequencies without substantial attenuation. Of course, the reason for this lowpass characteristic is rendered transparent by the original circuit in Figure (1.8). In particular, there is only one energy storage element –capacitor C_l– in the subject network. At very low signal frequencies, this capacitor emulates an open circuited branch, thereby collapsing the network at hand to a purely resistive, so called ***memoryless***, circuit. In a memoryless configuration, no branch element has an impedance that varies with signal frequency and accordingly, the gain of such a circuit is a constant, independent of signal frequency. At higher frequencies, the impedance of capacitor C_l decreases and in the limit of infinitely large frequency, the impedance of C_l approaches zero ohms. Since C_l is incident with the output port of the circuit, the magnitude of the output voltage, $V_o(j\omega)$, and thus the gain, $V_o(j\omega)/V_s(j\omega)$, decreases progressively toward zero for large signal frequencies.

(5). The gain expression deduced in the preceding computational step indicates that the zero frequency gain, say $A_v(0)$, is actually the Thévenin voltage gain, A_{st}. In the most general of circuit analyses, A_{st} is not identically equal to the zero frequency gain. It happens here that $A_{st} \equiv A_v(0)$ only because the load, which is removed from the otherwise memoryless network in the course of delineating the Thévenin gain, happens to be a capacitor. Thus, removal of the load in this example is tantamount to a consideration of zero signal frequency effects since a capacitive impedance at zero frequency is infinitely large.

In a lowpass circuit, the *3-dB* frequency, ω_b, is the frequency at which the gain magnitude is a factor of the square root of two smaller than the magnitude of the zero frequency gain; that is,

$$\left|A_v(j\omega_b)\right| \triangleq \frac{\left|A_v(0)\right|}{\sqrt{2}} = \frac{\left|A_v(0)\right|}{\left|1 + j\omega_b R_{th} C_l\right|} . \tag{E1-12}$$

Evidently,

$$\boxed{\omega_b = \frac{1}{R_{th} C_l} ,} \tag{E1-13}$$

which is little more than the inverse time constant associated with the lone capacitive element, C_l, in the original network.

A factor of *root two* gain degradation is equivalent to a gain magnitude deterioration of *three decibels* because of the definition of a decibel. In particular, the decibel value of any positive or a negative number, X, is $20\log_{10}|X|$. If X is root two, its decibel (or *dB*) value is very close to *3*. It follows that

$$\begin{aligned} A_v(j\omega_b) \text{ in db} &= 20\log_{10}\left|A_v(j\omega_b)\right| = 20\log_{10}\left|A_v(0)\right| - 20\log_{10}\sqrt{2} \\ &\approx 20\log_{10}\left|A_v(0)\right| - 3\,dB ; \end{aligned}$$

that is, the decibel value of gain is reduced from its decibel value of zero frequency gain by an amount equal to *3 dB*. Hence, the signal frequency effecting a root two gain magnitude reduction is termed the *3-dB* frequency.

(6). The gain relationships in Step (4) can now be written in the forms

$$A_v(j\omega) = \frac{V_o(j\omega)}{V_s(j\omega)} = \frac{A_{st}}{1 + j\omega/\omega_b} , \tag{E1-14}$$

and

$$\left|A_v(j\omega)\right| = \left|\frac{V_o(j\omega)}{V_s(j\omega)}\right| = \frac{\left|A_{st}\right|}{\sqrt{1+\left(\omega/\omega_b\right)^2}} . \tag{E1-15}$$

The frequency response of an amplifier is simply the plot of its gain magnitude as a function of signal frequency. For the amplifier undergoing consideration herewith, this plot appears in Figure (1.10), where the gain scale is in units of decibels and is normalized to the zero frequency gain, A_{st}. The frequency scale is normalized to the *3-dB* bandwidth, ω_b.

The frequency response effectively pictures the ability of an amplifier to process applied input signals of varying frequencies. For example, the lowpass amplifier at hand is capable of providing an essentially constant I/O transmission over relatively low frequencies, but it is incapable of sustaining this transmission at high frequencies. To this end, the *3-dB* frequency is a measure of amplifier effectiveness over frequency. To the extent that "essentially constant gain" can be viewed as a gain magnitude that is within *three decibels* of its maximum (in this case, the low frequency) gain, the *3-dB* bandwidth, ω_b, can be interpreted as the maximum frequency over which relatively constant gain is sustained. In this example, the maximum gain is actually less than one, which logically brings into question the utility of the considered amplifier. Despite this less than unity maximum gain, the buffer enjoys widespread popularity in electronic circuits and systems. More information about buffering applications is provided subsequently.

(7). For the stipulated numerical values of all device and circuit parameters, the Thévenin gain, the Thévenin voltage gain, Thévenin resistance, and *3-dB* bandwidth are

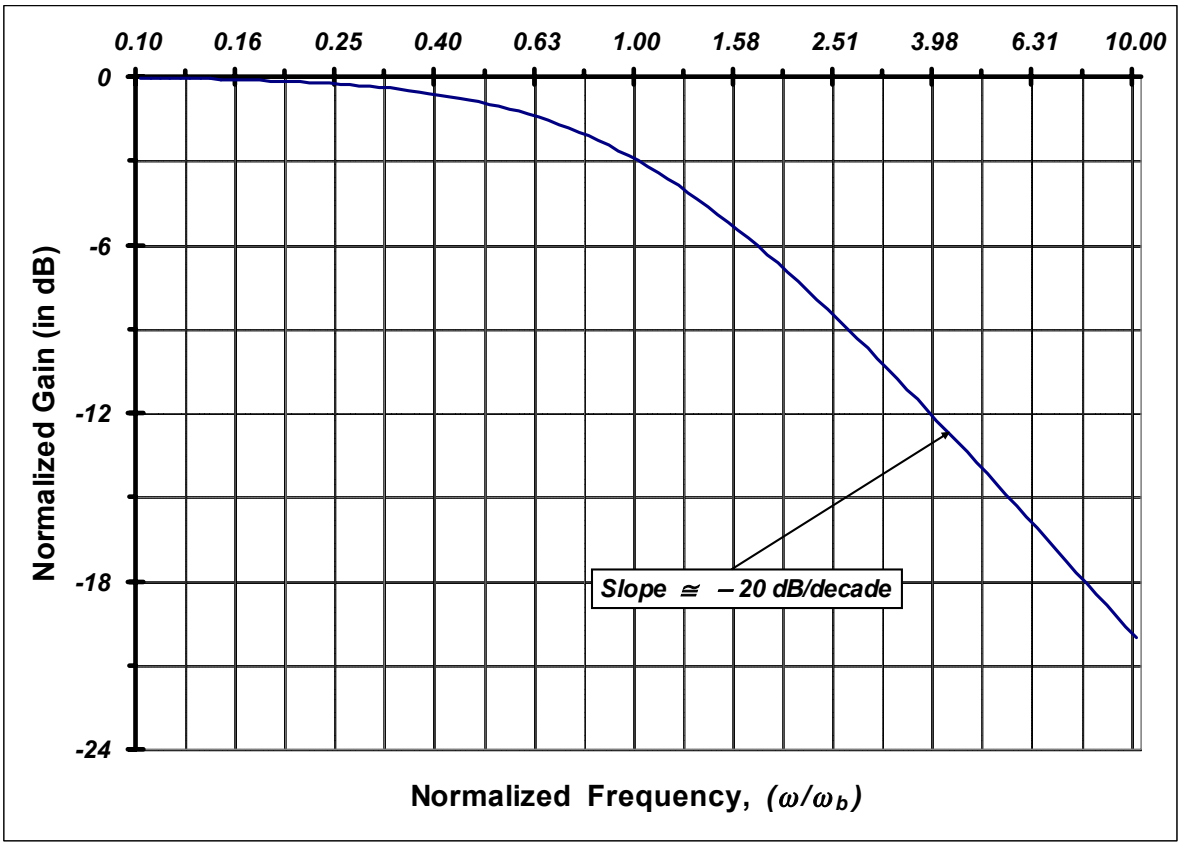


Figure (1.10). Frequency Response Of The Amplifier Studied In Example (1.1). The Gain Scale Is Normalized To The Zero Frequency Value, A_{st}, Of Amplifier Gain.

$$\begin{aligned} A_{st} &= 0.993 = -0.063\ dB \\ R_{th} &= 20.51\ \Omega \\ \omega_b &= 2\pi(775.9\,MHz)\ . \end{aligned}$$

In short, the buffer considered herewith establishes, within *3-dB* error, almost unity voltage gain *(0 dB)* over a frequency passband extending from *0 Hz* -to- slightly under *776 MHz*, while providing a Thévenin resistance at its output port of slightly more than *20 Ω*. Because the Thévenin resistance is indeed computed at the output port of the amplifier, this resistance metric is referred to as simply the amplifier ***output resistance***.

COMMENTS: The commentaries accompanying the preceding computational steps can be supplemented by the overarching observation of the profound simplicity of the Thévenin equivalent circuit. In particular, the original circuit in Figure (1.8) contains eight *(8)* branch elements, while its Thévenin model in Figure (1.9c) contains only three *(3)* elements. This simplicity fosters design-oriented insights that are not rendered immediately transparent by the original configuration. For example, to the extent that the design objective is the realization of a buffer characterized by near unity low frequency gain and very low output resistance, the results highlighted by the Thévenin model suggest that large transistor β is essential. Note that the output resistance clearly satisfies

$$R_{th} < \frac{r_\pi + r_b + R_s}{\beta + 1},$$

which further dramatizes the importance of large β. Even the ability to achieve large *3-dB* bandwidth is seen to be strongly dependent on transistor β, since

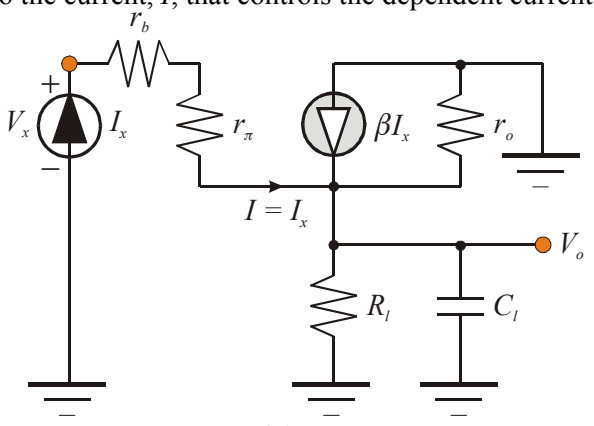
$$\omega_b = \frac{1}{R_{th}C_l} \approx \frac{\beta + 1}{(R_s + r_b + r_\pi)C_l}.$$

EXAMPLE #1.2:

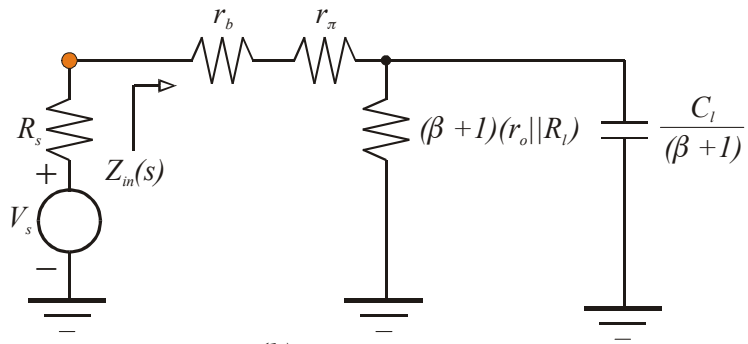
Reconsider the circuit in Figure (1.8) from the perspective of evaluating the Thévenin equivalent circuit presented to the signal source by the input port of the amplifier. Using the parameter values provided in the preceding example, evaluate the Thévenin input impedance at zero frequency, infinitely large signal frequency, and the previously computed *3-dB* frequency of the amplifier.

SOLUTION #1.2:

(1). Because the circuit capacitor in Figure (1.8) is presumed to have zero initial charge and because no other energy sources appear within the network to the right of the signal source, the Thévenin equivalent circuit at the amplifier input port is comprised exclusively of an impedance, say $Z_{in}(s)$. The pertinent model for computing this impedance appears in Figure (1.11a) and reflects the fact that the "ohmmeter" current, I_x, is identical to the current, I, that controls the dependent current source, βI.



(a).



(b).

Figure (1.11). (a). Circuit Model Used To Compute The Thévenin Impedance Presented To The Signal Source By The Input Port Of The Amplifier. **(b).** Topological Depiction Of The Thévenin Input Impedance Determined For The Equivalent Circuit In (a).

(2). Since the branch elements, R_l, r_o, and C_l are connected in parallel with one another and since the net current flowing through this shunt interconnection *is* $(\beta + 1)I = (\beta + 1)I_x$,

$$V_x = \left(r_b + r_\pi\right) I_x + \frac{\left(\beta + 1\right)\left(r_o \| R_l\right) I_x}{1 + s\left(r_o \| R_l\right) C_l}, \tag{E2-1}$$

whence

$$\boxed{Z_{in}(s) = \frac{V_x}{I_x} = r_b + r_\pi + \frac{\left(\beta + 1\right)\left(r_o \| R_l\right)}{1 + s\left(r_o \| R_l\right) C_l}.} \tag{E2-2}$$

This result can be rewritten in the form

$$Z_{in}(s) = r_b + r_\pi + \frac{\left(\beta + 1\right)\left(r_o \| R_l\right)}{1 + s\left[\left(\beta + 1\right)\left(r_o \| R_l\right)\right]\left[\frac{C_l}{\left(\beta + 1\right)}\right]}, \tag{E2-3}$$

which suggests representing the input amplifier port by the model offered in Figure (1.11b).

Because the Thévenin impedance found above pertains to the input port of the considered amplifier, it is often referred to as the ***Thévenin input impedance*** or, in abridged fashion, the ***input impedance*** of the amplifier. Note that this input impedance is computed with the capacitive load in tack; that is, the capacitive load is not removed from the circuit, as it is in the Thévenin voltage determination. In the jargon of circuit theory, the resultant input impedance, with the actual load connected, is sometimes called the ***driving point input impedance***, as opposed to the open circuit input impedance, which would be $Z_{in}(s)$ under the condition of load removal.

(3). At zero signal frequency, the load capacitance behaves as an open circuit. More correctly, the admittance, sC_l, of the load capacitance at zero frequency is zero. From either the foregoing analytical disclosures or the representation in Figure (1.11b),

$$\boxed{Z_{in}(0) = r_b + r_\pi + \left(\beta + 1\right)\left(r_o \| R_l\right) = 344.7\ K\Omega.}$$

(4). At infinitely large signal frequency, the load capacitance behaves as an short circuit. In particular, the impedance, $1/sC_l$, of the load capacitance is zero at infinitely large signal frequency. From either the foregoing analytical disclosures or the representation in Figure (1.11b),

$$\boxed{Z_{in}(\infty) = r_b + r_\pi = 2.20\ K\Omega.}$$

(5). At the *3-dB* bandwidth, ω_b, of the buffer, the driving point input impedance is

$$Z_{in}(j\omega_b) = r_b + r_\pi + \frac{\left(\beta + 1\right)\left(r_o \| R_l\right)}{1 + j\omega_b\left(r_o \| R_l\right) C_l}. \tag{E2-4}$$

From the preceding example, $\omega_b = 2\pi(775.9\ MHz)$ and accordingly,

$$\boxed{Z_{in}(j\omega_b) = 2{,}200 + \frac{342.5(10^3)}{1 + j138.0} \approx \left(2{,}200 - j2{,}482\right)\Omega.}$$

Since the imaginary part of this impedance function is negative, the input impedance at the *3-dB* bandwidth of the amplifier is noted to be capacitive.

COMMENTS: The use of Thévenin's theorem has served to highlight several important properties of a voltage buffer. The first of these properties, which derives from Example (1.1), is that the low frequency voltage transmission factor, or gain, is less than unity, but indeed, close to one. A second property is a low frequency input impedance that is significantly larger than the low frequency Thévenin output impedance. In particular, the I/O impedance transformation ratio is, from the present and preceding example, $344.7\ K\Omega/20.51\ \Omega = 16.8(10^3)$. As is illustrated shortly, this dramatic ratio boasts utility in practical electronic systems. Third, the capacitive nature of the input impedance renders a significant reduction of this impedance over signal frequency. In this example, the difference between the low frequency and very high frequency input impedances is $344.7\ K\Omega/2.20\ K\Omega$, which is better than *156*.

1.3.0. DEPENDENT SOURCES AND AMPLIFIER CONCEPTS

The Thévenin and Norton theorems and concepts addressed in the preceding section of material lay a foundation on which to build a fundamental understanding of general amplifiers and their respective properties. This understanding sets the stage for both open loop and closed loop electronic system design strategies by transforming the abstractness of dependent energy sources into topological tools that support design objectives. To this end, it is both instructive and interesting to be aware of the fact that there exist only four fundamental types of linear amplifiers and that these four amplifier configurations respectively emulate the four controlled sources that are an implicit part of basic circuit theory literature.

The most popular amplifying unit is the ***voltage amplifier***, whose practical implementation delivers volt-ampere characteristics that emulate those of an ideal voltage controlled voltage source. The ubiquitous operational amplifier is an excellent example of a voltage amplifier. The second most common amplifier is the ***transadmittance amplifier***, which is often referred to in the literature as simply a ***transconductor***. The transconductor, which emulates the electrical characteristics of a voltage controlled current source, delivers an output port current that is directly proportional to applied input port voltage. It is the foundation of many broadband low-pass and tuned radio frequency (RF) amplifiers. It also enjoys utility as the gain cell implicit to wideband and ultra linear active resistance-capacitance (RC) filters. The ***transimpedance amplifier***, or ***transresistor***, is the dual of the transconductor. It converts an applied input current to an output voltage response and as such, its electrical dynamics approximate the ideal current controlled voltage source. Like the transconductor, the transresistor is often the core active element of broadband networks. It is often synthesized by appending appropriate feedback to a basic voltage amplifier. An operational amplifier operated with resistive feedback between its input and phase-inverted output ports is among the most common of transresistors. Finally, the volt-ampere characteristics of a ***current amplifier*** emulate the electrical properties of an ideal current controlled current source. The current amplifier is rarely used as stand-alone circuit architecture. Instead, its impedance transformation attributes encourage its utilization in conjunction with transconductors to arrive at compensated circuits whose bandwidths are, under certain conditions, substantively larger than the bandwidth capabilities of transconductors operated without current amplifier compensation.

1.3.1. VOLTAGE AMPLIFIER

The circuit schematic symbol of a voltage amplifier is diagrammed in Figure (1.12a). Like all simple linear amplifiers, it is a ***two port*** structure. Its input port, to which signal is applied to establish the differential input port voltage, V, which is ultimately amplified, is comprised of the two terminals labeled *"+"* and *"–."* The *"+"* terminal is called the ***non-inverting input terminal***, while the *"–"* terminal is termed the ***inverting node***. The output port on the right of the circuit schematic symbol supports the Thévenin, or open circuit, voltage response, V_{th}, to applied input excitation. In the most general case, the open circuit, or Thévenin, response, V_{th}, is extracted differentially between the two terminals that comprise the amplifier output port. If one of the two output port terminals is incident with the amplifier ground terminal, V_{th} is referred to as a ***single ended output voltage***. If, as is diagrammed in the subject figure, neither of the two output port terminals is grounded, V_{th} is called a ***differential output voltage***. Similarly, note that voltage V might be termed a ***differential input voltage*** because neither of the two input port terminals across which this voltage is established is indicated as common to the amplifier ground.

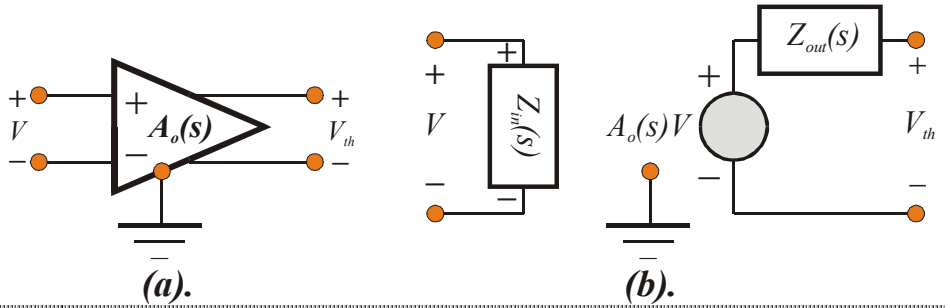


Figure (1.12). (a). Circuit Schematic Symbol Of A Voltage Amplifier. The Amplifier Is Depicted In Its Non-Inverting Mode, Since The Controlling Input Voltage, V, Is Applied Differentially From The Non-Inverting Input Terminal -To- The Inverting Input Terminal. **(b).** Circuit Model Of The Amplifier In (a). Parameter $Z_{in}(s)$ Is The Driving Point Input Impedance. To First Order, This Impedance Is Independent Of The Load Termination. Parameter $Z_{out}(s)$ Is The Driving Point Output Impedance Of The Amplifier. The Parameter, $A_o(s)$, Is The Thévenin Voltage Gain Of The Amplifier And Is Measured As The Ratio Of The Differential Open Circuit Output Voltage, V_{th}, -To- The Differential Input Port Voltage, V.

The indicated gain, $A_o(s)$, is a frequency dependent transfer function. For $V > 0$, which indicates that the non-inverting input terminal lies at a signal potential that is larger than the potential established at its inverting counterpart, the Thévenin output voltage is $A_o(s)V$, thereby implying no phase inversion between the input and output ports. In other words, if V rises with time, the Thévenin output voltage is an amplified version of voltage V that likewise increases with time. On the other hand, for $V < 0$, which suggests that V is applied from the *"–"* input terminal -to- the *"+"* input terminal, as opposed to the polarity indicated in Figure (1.12a), the open circuit output voltage is $-A_o(s)V$, and *180* degree I/O phase inversion is evident.

From Thévenin's theorem, a viable equivalent circuit for the voltage amplifier abstracted in Figure (1.12a) is the model offered in Figure (1.12b). The input port model, which consists of a simple input impedance branch, $Z_{in}(s)$, reflects the presumption that no energy sources appear either within the active amplifier block or at the output port of the amplifier. Strictly speaking, $Z_{in}(s)$ is a driving point input impedance; that is, it is an impedance that is dependent on the load that terminates the amplifier output port. However, in this initial foray

into the world of linear amplifiers, $Z_{in}(s)$ is presumed independent of the output port load. This presumption means that $Z_{in}(s)$ is unchanged whether the output port is terminated in a specific load or open circuited, as it is during the process of computing the Thévenin output port voltage. As the student will ultimately learn, this independence of the Thévenin input impedance on load termination is closely approximated if there is insignificant internal feedback implicit to the active amplifier cell. In turn, negligible internal feedback is generally a reasonable presumption at all but very high signal frequencies.

In the output port representation, $Z_{out}(s)$ is the usual Thévenin equivalent impedance seen looking into the output terminal. This impedance is, in fact, the driving point output impedance in that it is determined under the condition of the input port terminated in the internal impedance of the applied signal source. Like the nominal independence of $Z_{in}(s)$ on load termination, $Z_{out}(s)$ is also nominally independent of source impedance if negligible internal feedback prevails within the amplifier itself. The dependent voltage, $A_o(s)V$, is the Thévenin voltage established at the output port, while $A_o(s)$ is the Thévenin voltage gain measured from the differential amplifier input port, where voltage V prevails, -to- the open circuited differential output port where the Thévenin voltage, V_{th}, is established.

In an actual linear application of the voltage amplifier, a signal voltage source having a Thévenin internal impedance of $Z_s(s)$ activates the input port, while a load impedance, $Z_l(s)$, terminates the output port, as is depicted in Figure (1.13a). Recalling the amplifier model hypothesized in Figure (1.12b), the system model pertinent to Figure (1.13a) is the topology appearing in Figure (1.13b). By inspection, the overall system voltage gain, say $A_v(s)$, is

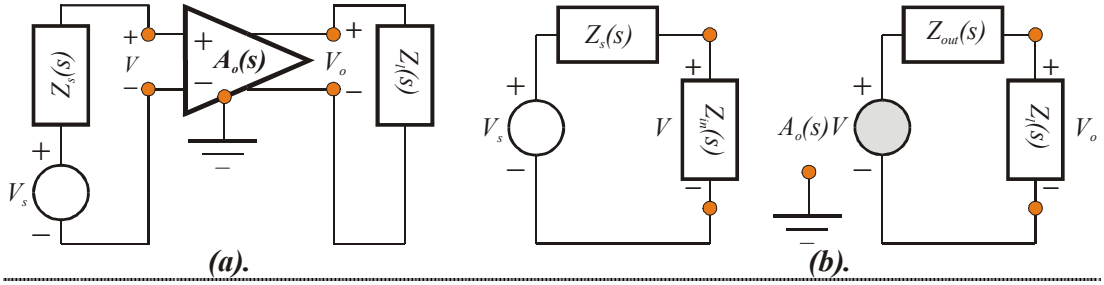


Figure (1.13). (a). System Schematic Depiction Of A Voltage Amplifier Terminated In A Load Impedance And Driven At Its Input Port By A Voltage Source. **(b).** Equivalent Circuit Of The System In (a). The Input Voltage, V, And The Output Response, V_o, Are Taken Herewith As Differential Circuit Branch Voltages. However, And Depending On The Actual System Architecture, Either V Or V_o, Or Both, Can Be Single Ended Variables. If Both V And V_o Are Extracted As Single Ended Node Voltages, The System In (a) Is Said To Maintain A Common Ground Between Its Input And Output Ports.

$$A_v(s) = \frac{V_o}{V_s} = \frac{V_o}{V} \times \frac{V}{V_s} = A_o(s)\left[\frac{Z_l(s)}{Z_l(s)+Z_{out}(s)}\right]\left[\frac{Z_{in}(s)}{Z_{in}(s)+Z_s(s)}\right], \qquad (1\text{-}7)$$

which shows that the overall voltage gain, compared to the Thévenin voltage gain, $A_o(s)$, is degraded by a factor equal to the product of input port and output port voltage dividers. The gain, $A_o(s)$, is the gain afforded by the amplifying device and is therefore the maximum possible gain achievable in a linear system in which this device is embedded. Accordingly, (1-7) underscores the fact that a linear system degrades the available device gain by the combined effects of nonzero amplifier driving point output impedance and finite amplifier driving point input imped-

ance. This observation begets a stipulation of the electrical characteristics indigenous to an ***ideal voltage amplifier***.

(1). *The driving point input impedance, $Z_{in}(s)$, is infinitely large for all signal frequencies and for all load terminations.* Note that the infinitely large input impedance property implies that zero current is drawn from the signal source by the amplifier input port. As a result, no voltage drop appears across the internal signal source impedance, thereby maximizing the transfer of applied Thévenin source voltage to the amplifier input port.

(2). *The driving point output impedance, $Z_{out}(s)$, is zero for all signal frequencies and for all signal source impedances.* This characteristic allows an output port voltage to be developed across any load impedance, inclusive (in principle only) of even a short-circuited load. More importantly, the voltage developed across the load termination is the Thévenin output port voltage, which is the maximum possible voltage that can be generated across the terminating load impedance.

(3). *In an ideal voltage amplifier, $A_o(s)$ is a constant, A_o, independent of signal frequency*. Properties #1 and #2 allow for a system gain that is identically equal to the voltage gain afforded by the amplifying device. Pragmatically, this gain, $A_o(s)$, is generally a suitably large, constant, real number, say A_o, at low frequencies. At high frequencies in the steady state, it attenuates at a minimum rate of *20 dB/decade* because of unavoidable intrinsic energy storage parasitics. Observe that the idealized constant gain stipulation implies the unrealistic device capability of amplifying signals whose frequencies embody a range extending from "DC" -to- daylight.

Figure (1.14) summarizes the electrical properties of an ideal voltage amplifier.

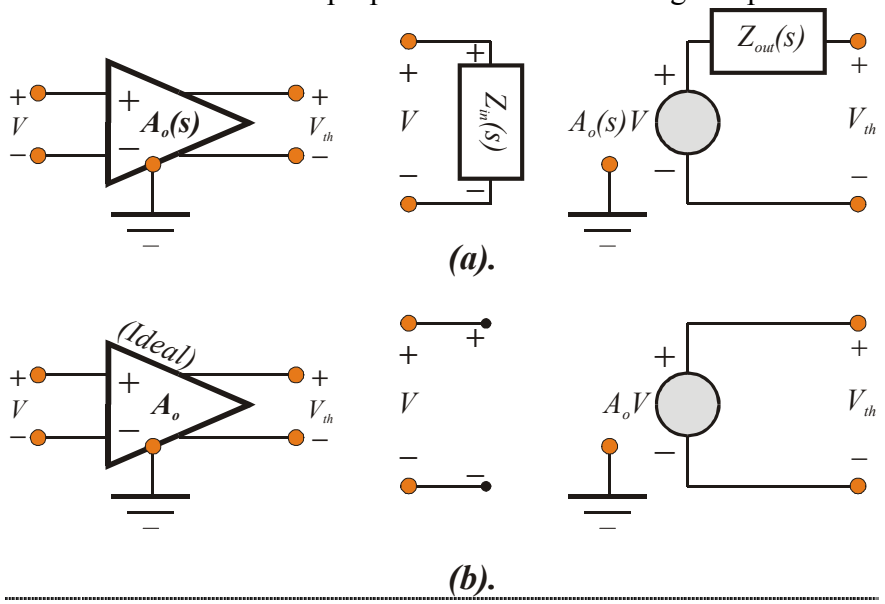


Figure (1.14). (a). System Schematic Diagram And Circuit Level Model Of A Voltage Amplifier. **(b).** System Schematic Diagram And Circuit Level Model Of An Ideal Voltage Amplifier. The Gain Parameter, A_o, Is A Constant, Independent Of The Frequencies Of Applied Input Signals.

Voltage amplifiers are often operated with differential input and single ended output ports. With reference to Figure (1.12a), the pertinent circuit schematic symbol is the structure shown in Figure (1.15a), and the applicable equivalent circuit appears in Figure (1.15b). In the interest of schematic simplicity, the diagram in Figure (1.15a) is generally cast in the form of Figure (1.15c), where it is understood that the output port voltage, V_{th}, is now referred to system

ground. The diagrams in Figures (1.13) and (1.14) remain applicable for single ended outputs, with the proviso that the system ground is now incident with the negative terminal of the output voltage response, V_o.

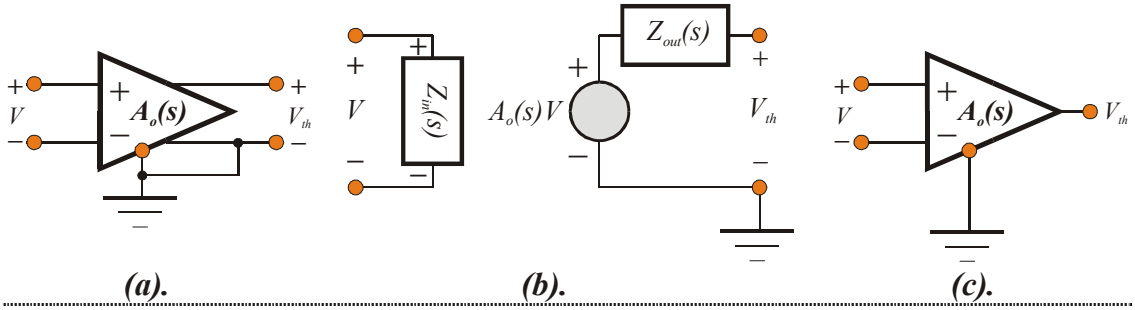


Figure (1.15). (a). Schematic Portrayal Of A Voltage Amplifier With Single Ended Output. **(b).** Equivalent Circuit Of The Single Ended Configuration Abstracted In (a). **(c).** Simplified Schematic Symbol Of A Voltage Amplifier With Single Ended Output. In This Depiction, The Open Circuit Output Voltage, V_{th}, Is Presumed Measured With Respect To The System Ground.

1.3.2. TRANSCONDUCTOR

The circuit schematic symbol of a transadmittance amplifier, or transconductor, appears in Figure (1.16a). Yet another name for this amplifier is ***operational transconductor amplifier***, which is commonly abbreviated as ***"OTA."*** The differential input port voltage, V, which is established as a result of applied input signal, is a positive number when it is measured from the non-inverting input terminal *(+)* -to- the inverting terminal *(–)*. This input port voltage is converted by the transconductor into a short circuit, or Norton, output current, I_n. The subject Norton current is proportional to V with a proportionality constant, $G_m(s)$, whose dimension is mhos; that is, $I_n = G_m(s)V$. Note that the positive algebraic sense of I_n is a current flowing into the positive output terminal and flowing out of the negative output terminal of the transconductor when $V > 0$. The Thévenin and Norton concepts introduced earlier render the architecture of Figure (1.16b) a plausible two port model of the linear transconductor.

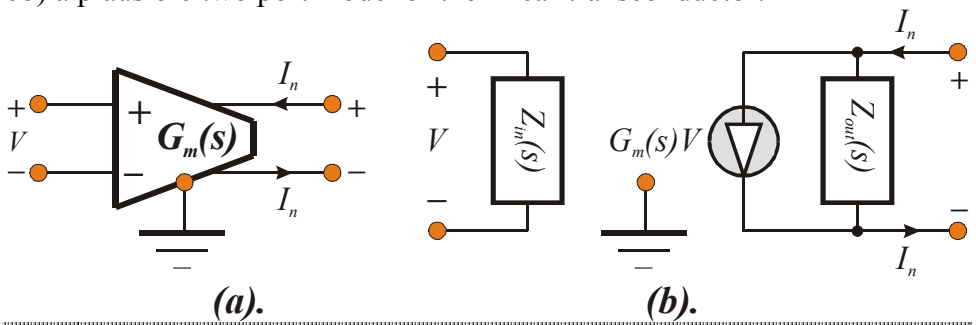


Figure (1.16). (a). Circuit Schematic Symbol Of A Transconductance Amplifier. **(b).** Circuit Model Of The Amplifier In (a). Parameter $Z_{in}(s)$ Is The Driving Point Input Impedance, While $Z_{out}(s)$ Is The Driving Point Output Impedance Of The Amplifier. The Parameter, $G_m(s)$, Is The Norton Transadmittance Of The Transconductor.

Figure (1.17a) offers a linear system application of the transconductor introduced in Figure (1.16), while Figure (1.17b) depicts its corresponding circuit model. As usual, $Z_s(s)$ represents the source impedance of the applied voltage signal, and $Z_l(s)$ is the load impedance incident with the transconductor output port. By inspection, the I/O transadmittance, say $Y_f(s)$, is

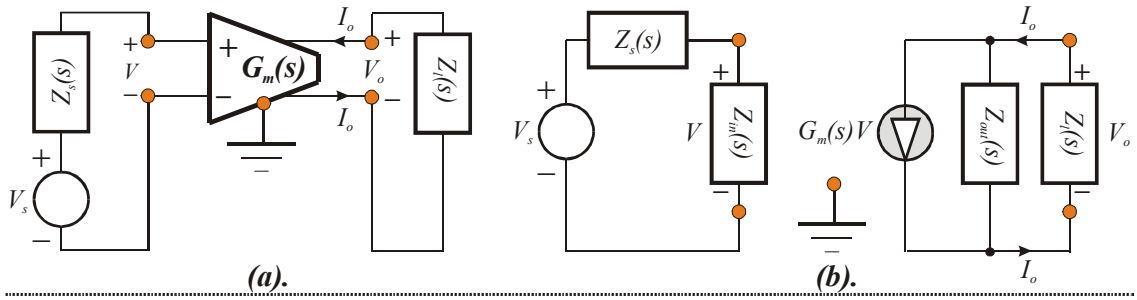


Figure (1.17). (a). System Schematic Diagram Of A Transadmittance Amplifier Terminated In A Load Impedance And Driven At Its Input Port By A Voltage Source. **(b).** Equivalent Circuit Of The System In (a).

$$Y_f(s) = \frac{I_o}{V_s} = \frac{I_o}{V} \times \frac{V}{V_s} = G_m(s)\left[\frac{Z_{out}(s)}{Z_{out}(s)+Z_l(s)}\right]\left[\frac{Z_{in}(s)}{Z_{in}(s)+Z_s(s)}\right]. \qquad (1\text{-}8)$$

Analogous to the voltage gain expression in (1-7), this transadmittance function is the product of a maximum transfer function (in this case, a transadmittance function) and two dividers. The first of the two dividers on the right hand side of this relationship, which is a current divider for the system output port in Figure (1.17b), approaches unity as the output impedance, $Z_{out}(s)$, tends toward an open circuit. The second divider is an input port voltage divider, which approaches unity as the driving point input impedance, $Z_{in}(s)$, emulates the impedance of an open circuit. These observations lead forthwith to the electrical definitions implicit to an ***ideal transadmittance amplifier***.

(1). *The driving point input impedance, $Z_{in}(s)$, is infinitely large for all signal frequencies and for all load terminations.* Infinitely large input impedance implies that zero current is drawn from the signal source by the amplifier input port. As a result, no voltage drop appears across the internal signal source impedance, thereby maximizing the transfer of applied Thévenin signal voltage to the amplifier input port.

(2). *The driving point output impedance, $Z_{out}(s)$, is infinitely large for all signal frequencies and for all signal source impedances.* This characteristic allows for an output current that is identical to the Norton output current and is therefore independent of load impedance.

(3). *In an ideal transconductor or transadmittance amplifier, $G_m(s)$ is a constant, independent of signal frequency*. Properties #1 and #2 allow for a system transadmittance that is identically equal to the transadmittance afforded by the amplifying device. Pragmatically, this forward transfer relationship is generally a suitably large, constant, real number, say g_m, at low frequencies. At high frequencies in the steady state, the effective forward transconductance attenuates owing to the unavoidable presence of internal energy storage parasitics.

Figure (1.18) reviews the foregoing electrical properties. Observe that the circuit model of an ideal transadmittance amplifier is identical to the schematic abstraction of a voltage controlled current source.

1.3.3. TRANSRESISTOR

Figure (1.19a) shows the circuit schematic symbol of a transimpedance amplifier, or more simply, a transresistor. This type of amplifier operates on applied input current, I, to generate an output port Thévenin voltage, $R_m(s)I$, that is proportional to current I. For a driving point input impedance of $Z_{in}(s)$ and a driving point output impedance of $Z_{out}(s)$, the electrical model is the topology offered in Figure (1.19b).

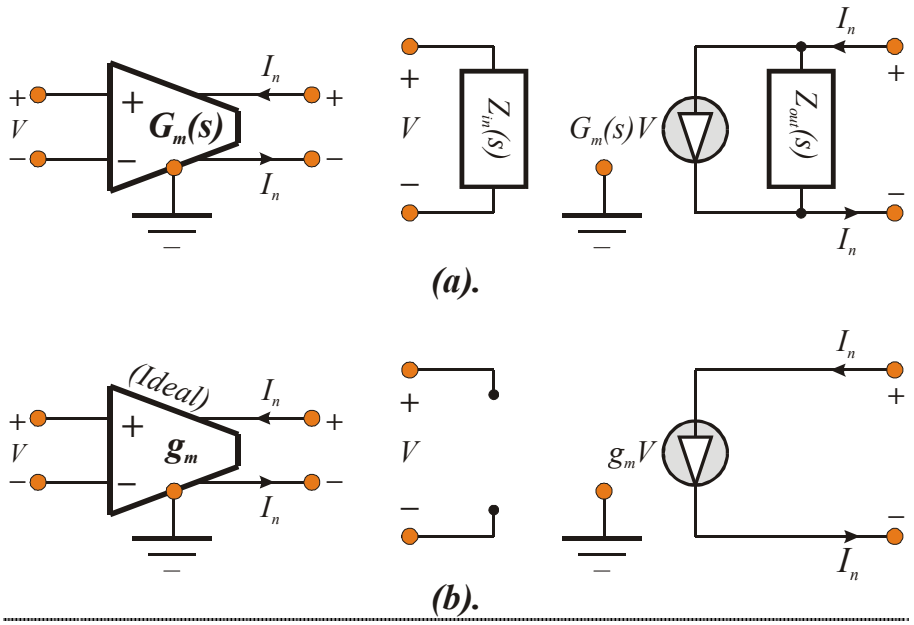


Figure (1.18). (a). System Schematic Diagram And Circuit Level Model Of A Transadmittance Amplifier, Or Transconductor. **(b).** System Schematic Diagram And Circuit Level Model Of An Ideal Transconductor. The Transconductance Parameter, g_m, Is A Constant, Independent Of Frequency.

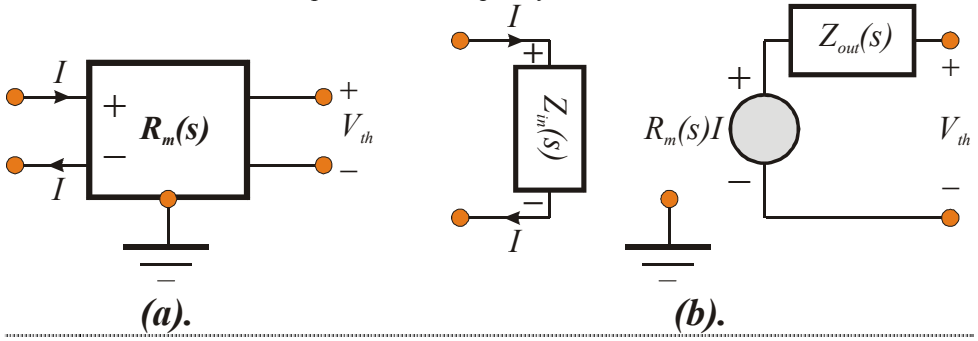


Figure (1.19). (a). Circuit Schematic Symbol Of A Transresistor. **(b).** Circuit Model Of The Amplifier In (a). Parameter $Z_{in}(s)$ Is The Driving Point Input Impedance, $Z_{out}(s)$ Is The Driving Point Output Impedance, and $R_m(s)$, Is The Thévenin Transimpedance Of The Device.

In system level applications of the transresistor, the input signal energy derives from a current source, I_s, whose presumably large Thévenin impedance is $Z_s(s)$, as depicted in Figure (1.20a). Also shown in this schematic diagram is a load impedance, $Z_l(s)$, that is incident with the transresistor output port and supports the resultant differential voltage response, V_o, to the input signal current source. The corresponding equivalent circuit in Figure (1.20b) delivers an I/O transimpedance, $Z_f(s)$, given by

$$Z_f(s) = \frac{V_o}{I_s} = \frac{V_o}{I} \times \frac{I}{I_s} = R_m(s)\left[\frac{Z_l(s)}{Z_l(s)+Z_{out}(s)}\right]\left[\frac{Z_s(s)}{Z_s(s)+Z_{in}(s)}\right]. \qquad (1\text{-}9)$$

An inspection of this relationship underscores the obvious fact that in the steady state, the magnitude, $|Z_f(j\omega)|$, of the overall transimpedance is less than the magnitude, $|R_m(j\omega)|$, of the Thévenin output port voltage -to- input port transimpedance. Accordingly, maximal forward

transimpedance is afforded when both $Z_{in}(s)$ and $Z_{out}(s)$ approach the impedance of a short circuit. This observation readily leads to the definition of an ***ideal transimpedance amplifier***.

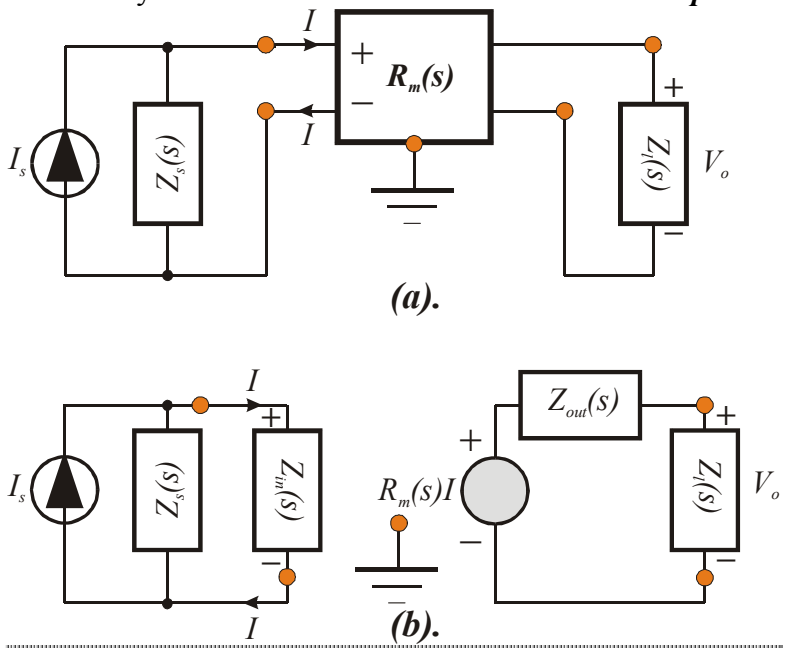


Figure (1.20). (a). System Schematic Diagram Of A Transimpedance Amplifier Terminated In A Load Impedance And Driven At Its Input Port By A Current Source. **(b).** Equivalent Circuit Of The System In (a).

(1). *The driving point input impedance, $Z_{in}(s)$, is zero for all signal frequencies and for all load terminations.* Zero input impedance means that no signal voltage can be sustained across the input port of a transresistor, which in turn suggests the impropriety of driving the input port of a transresistor with a voltage source.

(2). *The driving point output impedance, $Z_{out}(s)$, is zero for all signal frequencies and for all signal source impedances.* This characteristic implies that the output voltage developed in response to applied input current is theoretically independent of all load terminations.

(3). *In an ideal transresistor or transimpedance amplifier, $R_m(s)$ is a constant, independent of signal frequency*. Properties #1 and #2 allow for a system transimpedance that is identical to the transimpedance of the amplifying device. Pragmatically, this forward transfer relationship is generally a large, constant, real number, say r_m, at low frequencies. At high frequencies in the steady state, the low frequency value of this transimpedance attenuates because of unavoidable intrinsic energy storage parasitics.

In Figure (1.21), the foregoing electrical properties are reviewed and the electrical model of an ideal transimpedance amplifier is cast as a voltage controlled current source.

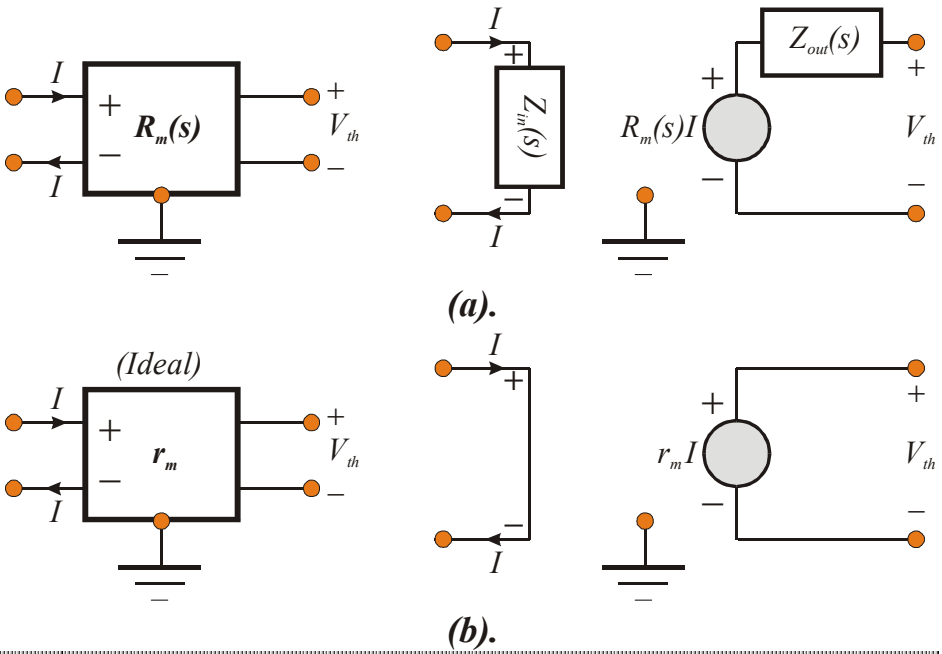


Figure (1.21). (a). System Schematic Diagram And Circuit Level Model Of A Transimpedance Amplifier, Or Transresistor. **(b).** System Schematic Diagram And Circuit Level Model Of An Ideal Transresistor. The Transresistance Parameter, r_m, Is A Constant, Independent Of Frequency.

1.3.4. CURRENT AMPLIFIER

The circuit schematic symbol of a current amplifier appears in Figure (1.22a). This amplifier responds to applied input current, I, to establish a Norton output current, $I_n = B_o(s)I$. With a driving point input impedance of $Z_{in}(s)$ and a driving point output impedance of $Z_{out}(s)$, the electrical model of a current amplifier is the network in Figure (1.22b).

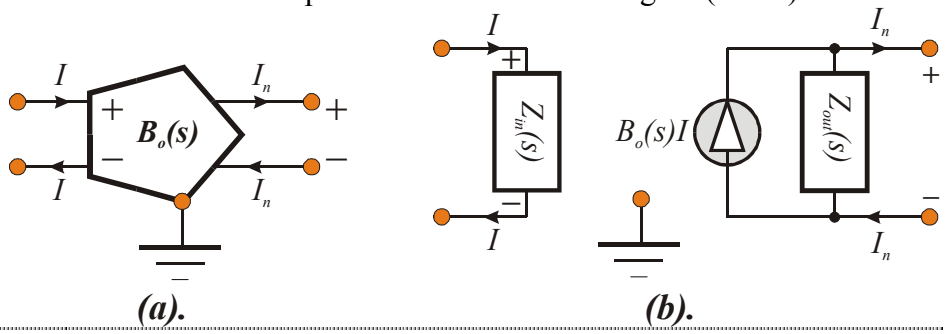


Figure (1.22). (a). Schematic Symbol Of A Current Amplifier. **(b).** Two Port Model Of The Current Amplifier In (a). Parameters $Z_{in}(s)$ and $Z_{out}(s)$ Respectively Denote The Driving Point Input And Output Impedances, While $B_o(s)$ Is The Norton Current Gain Of The Amplifier.

As in transresistor applications, the signal source applied to the input port of a current amplifier is a current source, I_s, having a relatively large source impedance, $Z_s(s)$. The resultant output response to this applied current is itself a current, I_o, conducted by load impedance $Z_l(s)$, which is connected across the amplifier output port. The system application at hand is abstracted in Figure (1.23a), for which the pertinent electrical model is the circuit diagram shown in Figure (1.23b). This model generates a system current gain expression whose algebraic form is similar to that of the transfer relationships derived for the three previously studied amplification systems; namely,

$$A_i(s) = \frac{I_o}{I_s} = \frac{I_o}{I} \times \frac{I}{I_s} = B_o(s)\left[\frac{Z_{out}(s)}{Z_{out}(s)+Z_l(s)}\right]\left[\frac{Z_s(s)}{Z_s(s)+Z_{in}(s)}\right]. \quad (1\text{-}10)$$

Clearly, $A_i(s)$ approximates $B_o(s)$, which is the maximum system current gain afforded by the utilized current amplification device, when $Z_{in}(s)$ is a very small impedance and $Z_{out}(s)$ is very large. It follows that an ***ideal current amplifier*** satisfies the requirements itemized herewith.

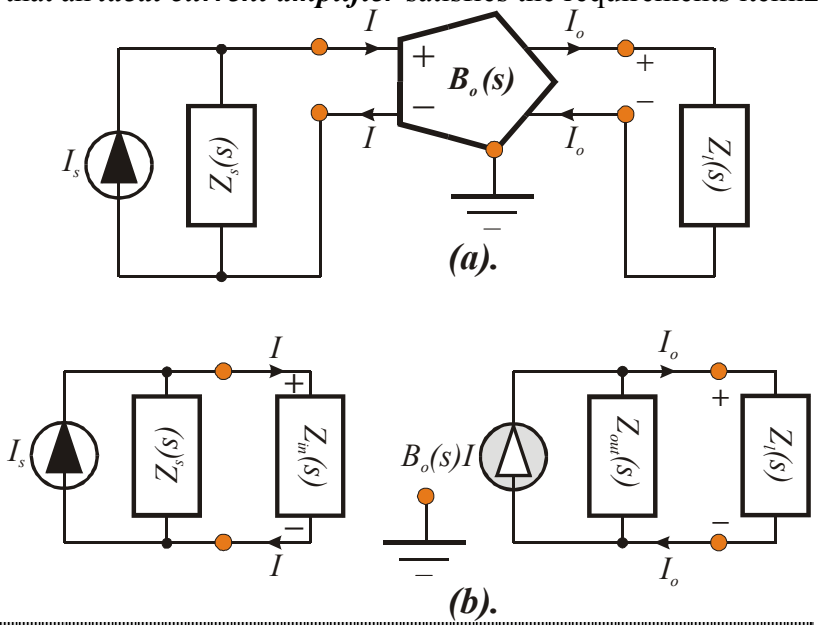


Figure (1.23). (a). System Level Application Of A Linear Current Amplifier. **(b).** Equivalent Circuit Of The Current Amplification System In (a).

(1). *The driving point input impedance, $Z_{in}(s)$, is zero for all signal frequencies and for all load terminations.*

(2). *The driving point output impedance, $Z_{out}(s)$, is infinitely large for all signal frequencies and for all signal source impedances.* This characteristic implies that the output current developed in response to applied input current is theoretically independent of all load terminations.

(3). *In an ideal current amplifier, $B_o(s)$ is a constant, independent of signal frequency*. Properties #1 and #2 allow for a system current gain that is identical to the maximum current gain allowed by the amplifying device. This current gain is generally a large, constant, real number, say A_{io}, at low frequencies. At high frequencies in the steady state, the low frequency value of the current gain attenuates at a minimum rate of *20 dB/decade* because of unavoidable intrinsic energy storage parasitics.

Figure (1.24) overviews the foregoing electrical properties and in the process, it depicts the electrical model of an ideal current amplifier as a current controlled current source.

1.3.5. BUFFERS

As might be suspected, the four types of amplifiers discussed in the preceding subsections of material are most commonly used to boost relatively anemic voltage or current signal amplitudes into more robust voltages and currents that can deliver required amounts of energy to specified loads. For example, consider the futility of connecting an audio speaker directly to the output terminals of a compact disc (CD) player. Typical audio speakers have nominal input impedances in the range of eight -to- sixteen ohms and may require as many as tens of volts of

excitation for proper performance and acceptable fidelity. In contrast, the Thévenin output impedance of representative CD units is *500 ohms* or larger. Moreover, CD players rarely deliver open circuit output voltages larger than a few tens of millivolts. Since a *16 Ω* speaker connected across a voltage source whose internal resistance is *500 Ω* comprises a voltage divider of roughly *1/32*, a CD unit having a *20 mV* open circuit output voltage capability delivers only about *620 microvolts* to the speaker terminals. This miniscule voltage is hardly sufficient to enjoy the Rolling Stones and thus, an appropriate amplifier (most likely a cascade of several amplifiers intertwined with requisite filters and signal processing subsystems) must be inserted between the CD player and the speaker.

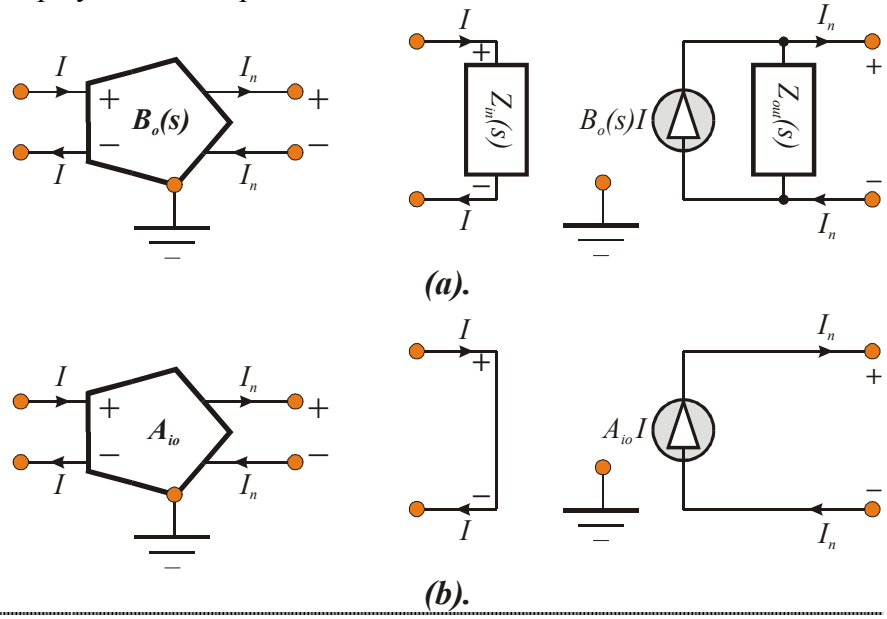


Figure (1.24). (a). System Schematic Diagram And Circuit Level Model Of A Current Amplifier. **(b).** System Schematic Diagram And Circuit Level Model Of An Ideal Current Amplifier. The Current Gain, A_{io}, Is A Constant, Independent Of Frequency.

If signal amplitude amplification is the dominant function of amplifiers, impedance buffering is the second most important application of amplifying networks. Buffers, which are ubiquitous in both analog and digital circuit technologies, perform impedance transformation between input and output ports so that the output voltage -to- signal source voltage transfer function or the output current -to- signal source current gain is maintained very close to unity for wide ranges of signal source and load impedances. Two types of buffers –the ***voltage buffer*** and the ***current buffer***– are commonly found in electronic systems.

1.3.5.1. Voltage Buffer

With reference to the generalized ideal voltage amplifier diagrammed symbolically in Figure (1.14b), an ***ideal voltage buffer*** has a frequency invariant Thévenin voltage gain of unity *(A_o = 1)* in addition to infinitely large input impedance and zero output impedance for all load and source terminations, respectively. Since the Thévenin voltage gain is the largest possible voltage gain achievable in a system into which a voltage amplifier is embedded within the I/O signal path, it is only natural to question the pragmatism of an active device capable of only unity voltage gain.

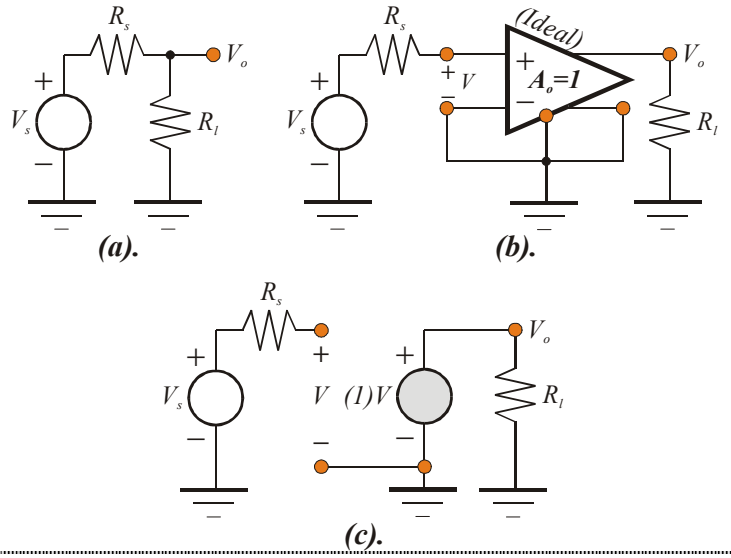


Figure (1.25). (a). A Voltage Divider For Which The Signal Voltage Of A Source Whose Thévenin Resistance Is R_s Is To Be Delivered To Load Resistance R_l. **(b).** Ideal, Buffer Inserted In I/O Signal Flow Path. **(c).** Model Of The Buffered System In (b).

A response to the foregoing inquiry begins by considering the simple voltage divider in Figure (1.25a). In this divider, the output voltage, V_o, is an attenuated version of the Thévenin signal source voltage, V_s, since

$$\frac{V_o}{V_s} = \frac{R_l}{R_l + R_s} . \tag{1-11}$$

If the hypothetical CD example considered in the preceding subsection is revisited herewith, the divider in question is *16/(16+500) = 1/32.25*, which suggests that only *3.1%* of the Thévenin signal voltage is actually delivered to the load resistance, R_l. In other words, *96.9%* of this signal voltage is "lost" in the internal resistance, R_s, of the signal source. In an attempt to mitigate this signal loss, an ideal buffer is inserted between the source and the load, as suggested in Figure (1.25b). Since the subject buffer has infinitely large input impedance, no current is drawn from the signal source and as a result, no voltage is "lost" in the Thévenin resistance of the source. Moreover, the zero output resistance of the buffer allows an output voltage response to be established across a load resistance of any value. The propriety of these assertions is confirmed by the model in Figure (1.25c), which produces

$$\frac{V_o}{V_s} = \frac{V_o}{V} \times \frac{V}{V_s} = (1)(1) = 1 . \tag{1-12}$$

Thus, *100%* of the Thévenin signal source voltage appears across the network output port as voltage V_o, independent of either load termination or source resistance.

Of course, no physically realizable voltage buffer is ideal. The practical buffer addressed in Examples (1.1) and (1.2), delivers a large, but nonetheless finite, input resistance of *344.7 KΩ*, a small, but nonzero, output resistance of *20.51 Ω*, and a nearly unity gain of *0.993*. If this buffer supplants its idealized counterpart in Figure (1.25), R_s = *500 Ω*, R_l = *16 Ω*, and (1-7)

lead to a voltage transfer function of $V_o/V_s = 1/2.3$. This result is hardly the desired ideal unity value, but it is *14-times* better than the non-buffered value of *1/32.25*.

EXAMPLE #1.3:

Operational amplifiers (op-amps) of reasonable quality can be gainfully exploited as voltage buffers in broadband electronic system applications. To this end, Figure (1.26a) depicts a voltage buffer realized with an op-amp having a single ended output port. For the purpose of this problem, assume that the op-amp has a Thévenin voltage gain (often referred to in the literature as the ***open loop gain***) of $A_o = 80\ dB$, an output resistance, r_o, of $35\ \Omega$, and an input impedance that is purely capacitive. The net value of the input capacitance, which is plausibly attributed to the combined effects of the op-amp, incorporated compensation, and circuit parasitics, is $C_i = 300\ pF$. The Thévenin resistance, R_s, of the signal source is $500\ \Omega$, while the load resistance, R_l, driven by the buffer is $16\ \Omega$. Derive general expressions for, and discuss the engineering significance of, the system voltage gain, $A_v(s) = V_o/V_s$, the output impedance, $Z_{out}(s)$, seen by the load resistance, R_l, and the input impedance, $Z_{in}(s)$, seen by the signal source.

SOLUTION #1.3:

(1). Recalling Figure (1.14b) and using the information provided in this problem, Figure (1.26b) is the equivalent circuit of the buffer in Figure (1.26a). In terms of the branch currents delineated in this diagram, KVL gives

$$A_oV = -r_o\left(sC_iV - \frac{V_o}{R}\right) + V_o\ ,$$

$$V_s = R_s\left(sC_iV\right) + V + V_o\ .$$

Subsequent to elimination of variable V from these equilibrium relationships, a bit of algebra confirms an I/O voltage transfer function of the form,

$$A_v(s) = \frac{V_o}{V_s} = \left(\frac{kA_o}{1+kA_o}\right)\left(\frac{1+\frac{s}{z}}{1+\frac{s}{p}}\right), \qquad \text{(E3-1)}$$

where

$$k = \frac{R_l}{R_l + r_o} \qquad \text{(E3-2)}$$

is a voltage divider between the resistances, r_o and R_l. Moreover, the input port capacitance appears to generate a left half plane pole at frequency p, as well as a left half plane zero at frequency z. These critical frequencies are given by

$$p = \frac{1+kA_o}{\left(R_s + kr_o\right)C_i} \qquad \text{(E3-3)}$$

and

$$z = \frac{A_o}{r_oC_i}\ . \qquad \text{(E3-4)}$$

(2). Several features of the voltage transfer function in (E3-1) warrant highlighting. First, observe that the system gain at zero frequency is

$$A_v(0) = \frac{kA_o}{1+kA_o}, \qquad \text{(E3-5)}$$

which is almost one by virtue of very large A_o. In the present case, $A_o = 80\ dB = 10{,}000$ and $k = 0.3137$, whence $A_v(0) = 0.9997$. It therefore appears that at least at low signal frequencies, the circuit in Figure (1.26a) very nearly satisfies the unity voltage gain objective of an ideal voltage buffer.

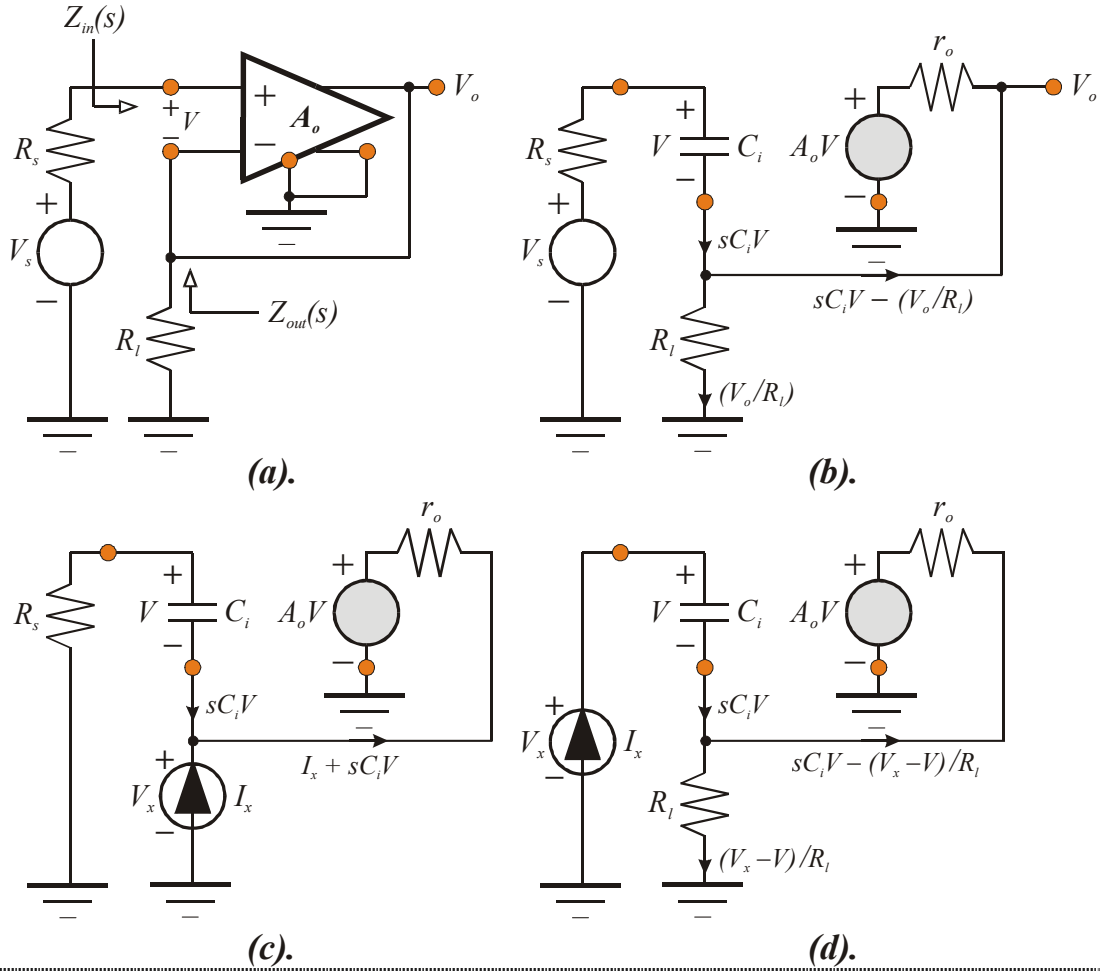


Figure (1.26). (a). Operational Amplifier With Single Ended Output Configured As A Voltage Buffer. The Signal Source Is Represented As The Series Interconnection Of Voltage V_s And Resistance R_s, While The Load Driven By The Buffer Is Taken To Be The Resistance, R_l. **(b).** Equivalent Circuit Of The System In (a). The Indicated Branch Currents Are Appropriate To A Determination Of The System Voltage Gain, $A_v(s) = V_o/V_s$. **(c).** Equivalent Circuit For The Determination Of The Driving Point Output Impedance, $Z_{out}(s)$. **(d).** Equivalent Circuit For Evaluating The Driving Point Input Impedance, $Z_{in}(s)$.

The locations of the pole and zero of the voltage transfer function define the frequency response of the buffer at hand. In the present case, $p = 2\pi(3.26\ GHz)$, and $z = 2\pi(151.6\ GHz)$. The frequency of the zero is better than *46-times* larger than the frequency of the pole and is, in fact, so large as to render dubious its validity in light of the frequency response limitations implicit to the utilized simple model. Numerical validity notwithstanding, the frequency of the zero is so much larger than that of the pole as to warrant its tacit neglect over a frequency passband extending from zero through, and somewhat beyond, the pole frequency. Accordingly,

$$A_v(s) = \frac{V_o}{V_s} \approx \frac{kA_o/(1+kA_o)}{1+\dfrac{s}{p}}, \tag{E3-6}$$

from which it is apparent that the *3-dB* bandwidth, say ω_b, is

$$\omega_b \approx p = \frac{1+kA_o}{(R_s+kr_o)C_i} \approx \frac{kA_o}{(R_s+R_l\|r_o)C_i} = 2\pi(3.26\ GHz). \tag{E3-7}$$

Thus, the buffer undergoing examination delivers very nearly unity gain from zero signal frequency to almost *3.3 GHz*.

(3). The "ohmmeter" model pertinent to computing the driving point output impedance, $Z_{out}(s)$, seen by the load resistance, R_l, is depicted in Figure (1.26c). For the branch currents indicated in this diagram, KVL produces

$$\begin{aligned} 0 &= R_s(sC_iV) + V + V_x \\ V_x &= r_o(I_x + sC_iV) + A_oV. \end{aligned} \tag{E3-8}$$

Upon elimination of the voltage variable, V, in these two relationships, it is easily demonstrated that the output impedance, expressed in terms of steady state frequency variables, is

$$\boxed{Z_{out}(j\omega) = \frac{V_x}{I_x} = \left(\frac{r_o}{1+A_o}\right)\left(\frac{1+j\omega\tau_z}{1+j\omega\tau_p}\right),} \tag{E3-9}$$

where the time constant, τ_z, associated with the zero of the impedance function and the time constant, τ_p, attributed to the impedance function pole are respectively given by

$$\tau_z = R_sC_i \tag{E3-10}$$

and

$$\tau_p = \frac{(R_s+r_o)C_i}{1+A_o}. \tag{E3-11}$$

(4). From (E3-9), the low frequency output impedance is

$$Z_{out}(0) = \frac{r_o}{1+A_o}, \tag{E3-12}$$

which is virtually zero because of the very large amplifier gain, A_o. Indeed, $Z_{out}(0)$ computes herewith to *0.0035 Ω*, which assuredly emulates the zero output impedance indigenous to an ideal voltage buffer.

The time constant associated with the impedance zero is $\tau_z = 150\ nSEC$, which corresponds to a frequency of $1/\tau_z = 2\pi(1.07\ MHz)$. On the other hand, $\tau_p = 16.05\ pSEC$, corresponding to a frequency, $1/\tau_p = 2\pi(9.92\ GHz)$. Clearly, the pole frequency is significantly larger (over *9,000-times* larger) than the zero frequency. It follows that for frequencies as large as an octave or two below the pole frequency,

$$Z_{out}(j\omega) \approx \left(\frac{r_o}{1+A_o}\right)(1+j\omega\tau_z), \tag{E3-13}$$

which suggests that the driving point output impedance is inductive. Specifically, this impedance reflects a resistance, say R_{eff}, connected in series with an inductance, say L_{eff}, such that

$$R_{eff} = \frac{r_o}{1+A_o}, \tag{E3-14}$$

and

$$L_{eff} = \left(\frac{r_o}{1+A_o}\right)\tau_z = \frac{r_o R_s C_i}{1+A_o}. \qquad \text{(E3-15)}$$

The indicated effective resistance is, as anticipated, the previously determined zero frequency value of the output impedance. Although the effective series inductance is small, it can cause poor transient circuit responses and/or even resonant frequency responses when, as is commonly encountered, the buffer drives a strongly capacitive load.

(5). Figure (1.26d) is the equivalent circuit pertinent to the evaluation of the driving point input impedance seen by the signal source. KCL and KVL applied to this circuit yield

$$I_x = sC_iV$$

$$0 = -A_oV + r_o\left(\frac{V_x - V}{R_l} - sC_iV\right) + V_x - V\ . \qquad \text{(E3-16)}$$

Solving the second of these two equations for voltage V and substituting the solution into the first equation results in

$$\boxed{Z_{in}(j\omega) = \frac{V_x}{I_x} = \left(\frac{1+kA_o}{j\omega C_i}\right)\left[1 + j\omega\left(\frac{kr_oC_i}{1+kA_o}\right)\right],} \qquad \text{(E3-17)}$$

which is clearly capacitive for all signal frequencies.

(6). Two interesting observations surface from an inspection of the result in (E3-17). First, note that at low frequencies, the effective input capacitance, say C_{ieff}, is very small and in particular, it is

$$C_{ieff} = \frac{C_i}{1+kA_o} = 95.6\ fF\ . \qquad \text{(E3-18)}$$

This small capacitance contributes to the relatively broadband response of the buffer. To confirm this assertion, recall from preceding modeling exercises that the input port of an amplifier, where C_{ieff} is established in this exercise (at least at low signal frequencies), directly faces the signal source circuit. In this case, the signal source has an internal resistance of R_s, which implies that C_{ieff} establishes a time constant at the input port of $R_sC_{ieff} = 47.8\ pSEC$. This time constant forges an input port pole at a frequency of $1/R_sC_{ieff} = 2\pi(3.33\ GHz)$. Since C_{ieff} is the only capacitance in the buffering system, this pole frequency is necessarily the *3-dB* bandwidth of the buffer. Indeed, the currently computed bandwidth of *3.33 GHz* differs from that calculated previously in (E3-7) by only *2.1%*. This miniscule computational difference is certainly understandable in light of the approximations invoked with respect to both (E3-7) and (E3-18).

A second observation derives from analytical considerations at very high signal frequencies. Specifically, (E3-17) shows that

$$Z_{in}(j\infty) = kr_o = r_o \| R_l\ . \qquad \text{(E3-19)}$$

Not only is the input impedance purely resistive at high frequencies, its specific resistive value is obvious from an inspection of the model in Figure (1.26b). In particular, capacitance C_i becomes a short circuit at infinitely large frequencies. This short circuit constrains voltage V to zero, which nulls the dependent voltage, A_oV. When A_oV is zero, resistance r_o is placed in parallel with load resistance R_l. It follows that with C_i effectively shorted, the signal source sees little more than the shunt interconnection of resistances r_o and R_l

COMMENTS: This example demonstrates how a generalized voltage amplifier model, which is itself predicated on basic Thévenin and Norton concepts, can be

judiciously exploited for the purpose of assessing the performance of a simple voltage buffer. Specifically, the example shows that a commonly used operational amplifier topology can deliver a broadband frequency response having a low frequency voltage gain very near unity. The considered buffer also has an output resistance that is very low at low frequencies, a very large input impedance at low frequencies, and a driving point output impedance that is inductive at high signal frequencies. Although these performance metrics are generally evident in practical voltage buffers, caution must be exercised with respect to the numerical values gleaned for these metrics. Numerical errors accrue because the model invoked in this exercise is elementary in that it exploits but a single energy storage element (the input capacitance) in the system. In actual buffers, additional energy storage elements invariably prevail, as does a frequency dependence on the Thévenin gain parameter, $A_o(s)$.

1.3.5.2. Current Buffer

The electrical model pertinent to examining the electrical characteristics at the input and output ports of an ideal current amplifier is provided in Figure (1.24b). Note therein that the input impedance is zero for all signal frequencies and for all load terminations and that the output impedance is infinitely large for all frequencies and source impedances. An ***ideal current buffer*** boasts these two impedance signatures, in addition to a frequency invariant Norton current gain of unity $(A_{io} = 1)$.

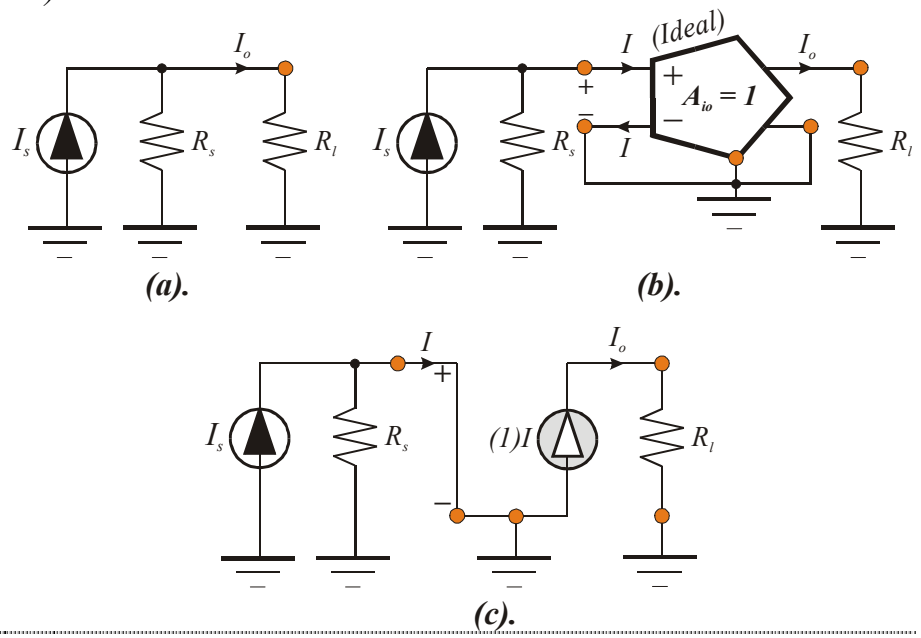


Figure (1.27). (a). A Simple Current Divider For Which The Signal Current Of A Source Whose Thévenin Resistance Is R_s Is To Be Delivered To A Load Resistance, R_l. **(b).** Ideal, Single Ended Current Buffer Inserted In The Signal Flow Path Between The Signal Source And The Load Of The Divider In (a). **(c).** Model Of The Buffered System In (b).

The utility of ideal current buffers can be rendered transparent with the help of the diagrams in Figure (1.27). In Figure (1.27a), a current source having an internal resistance of R_s is applied to a load resistance, R_l, with the result that the current, I_o, conducted by the load derives from

$$\frac{I_o}{I_s} = \frac{R_s}{R_s + R_l} . \tag{1-13}$$

If R_l is comparable to, or even larger than, R_s, the current actually delivered to the load is an appreciably attenuated version of the current, I_s, available from the signal source. Obviously, negligible signal attenuation, or loss, occurs only if $R_l << R_s$. Rendering this desired inequality apparently true is the fundamental purpose of a current buffer.

To the foregoing end, let a unity gain version of the current amplifier abstracted in Figure (1.24b) be inserted between the source and load, as indicated in Figure (1.27b). The corresponding model is the structure in Figure (1.27c), which offers

$$\frac{I_o}{I_s} = \frac{I_o}{I} \times \frac{I}{I_s} = (1)(1) = 1 . \tag{1-14}$$

As in the case of the voltage buffer considered previously, the current buffer provides an impedance transformation vehicle by which the load can be isolated from the source. Specifically, the signal source now drives a short circuit network input port, as opposed to the actual load resistance, R_l, thereby allowing the entire signal source current to be processed with unity gain. In turn, the load now faces an ideal current source, as opposed to the source resistance, R_s, wherein all of the processed signal current can be delivered to the load termination. The obvious keys to proper current buffering are a very low (ideally zero) input port impedance and a very high (ideally infinitely large) output impedance.

EXAMPLE #1.4:

Transconductors, which can be realized straightforwardly with either metal-oxide-semiconductor field-effect transistors (MOSFETs) or bipolar junction transistors (BJTs), can be configured to emulate ideal current buffers. To this end, consider the single ended current buffering configuration in Figure (1.28a), where the input signal is a current source comprised of current I_s and Thévenin resistance R_s, and the output response is taken as the current, I_o, conducted by the load resistance, R_l. Derive expressions for the current transfer ratio, I_o/I_s, the input resistance, R_{in}, seen by the signal source and the output resistance, R_{out}, seen by the load. Assume that only low signal frequencies are of interest, which allows the transconductor to be modeled by a shunt input resistance, R_i, shunt output resistance, R_o, and a frequency invariant transconductance of g_m.

SOLUTION #1.4:

(1). Recalling the transconductor models in Figure (1.18), the equivalent circuit of the current buffer in Figure (1.28a) is the circuit shown in Figure (1.28b). KVL applied to this model, in which branch currents have been delineated for analytical convenience, produces

$$\begin{aligned} 0 &= R_l I_o + R_o\left(I_o - g_m V\right) + R_s\left(\frac{V}{R_i} + I_o - I_s\right) \\ 0 &= V + R_s\left(\frac{V}{R_i} + I_o - I_s\right) . \end{aligned} \tag{E4-1}$$

A simultaneous solution of these two equilibrium relationships, followed by the obligatory algebra, results in a current transfer ratio of

$$A_i \triangleq \frac{I_o}{I_s} = \frac{\left(1+g_m R_o\right)\left(R_i \| R_s\right)}{R_l + \left(R_i \| R_s\right) + \left[1+g_m\left(R_i \| R_s\right)\right] R_o} . \qquad \text{(E4-2)}$$

It is clear that this gain is smaller than one. However, $A_i \approx 1$ if

$$g_m R_o >> 1 , \qquad \text{(E4-3)}$$

$$g_m\left(R_i \| R_s\right) >> 1 , \qquad \text{(E4-4)}$$

and

$$R_o >> \frac{R_l}{1+g_m\left(R_i \| R_s\right)} + R_i \| R_s \left\| \frac{1}{g_m} \right. . \qquad \text{(E4-5)}$$

Observe that satisfying the foregoing three inequalities fundamentally requires suitably large R_o and sufficiently large g_m. Both of these parametric constraints are implicit to reasonably high performance transconductors.

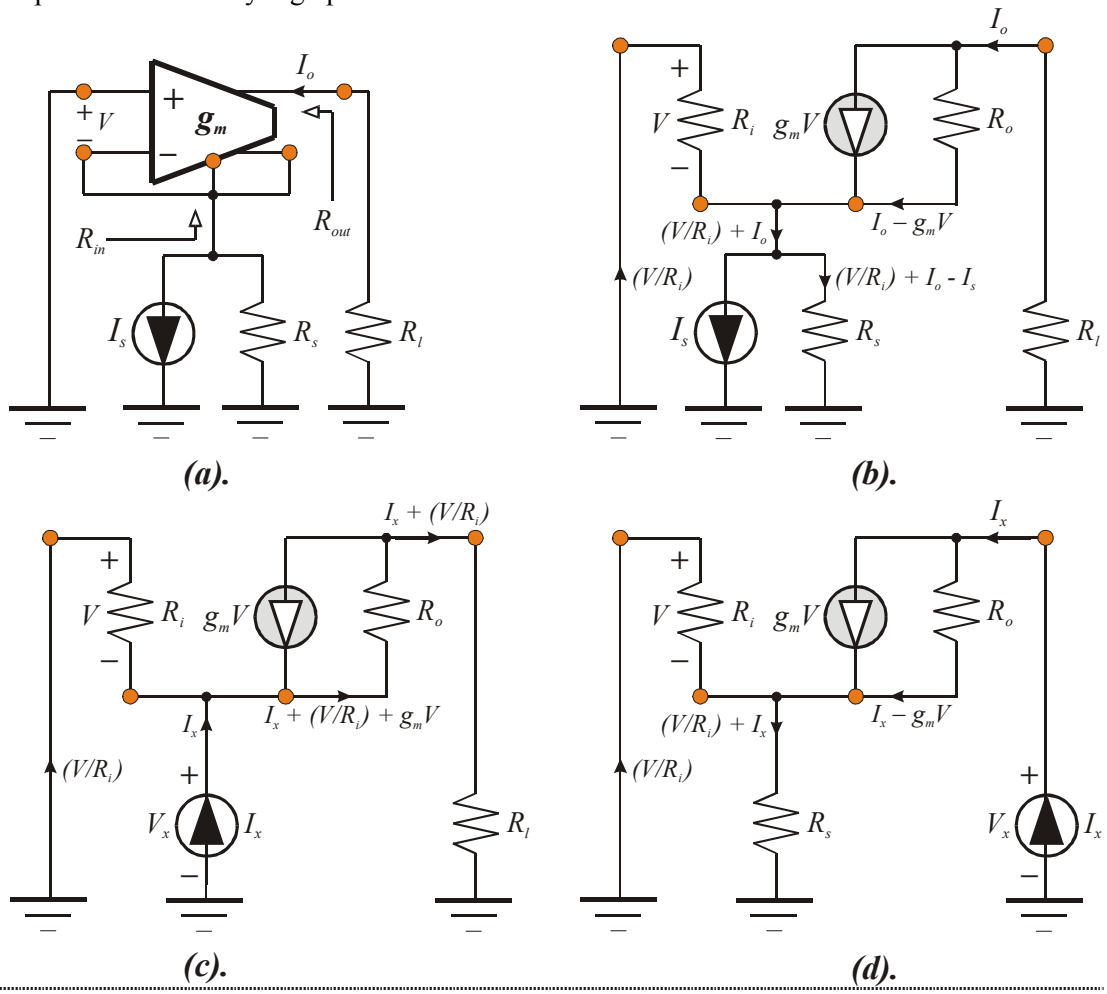


Figure (1.28). (a). Transconductor With Single Ended Output Configured As A Current Buffer. The Signal Source Is Represented As The Shunt Interconnection Of Current I_s And Resistance R_s, While The Load Is Taken To Be The Resistance, R_l. **(b).** Equivalent Circuit Of The System In (a). The Indicated Branch Currents Are Appropriate To A Determination Of The System Current Gain, $A_i = I_o/I_s$. **(c).** Equivalent Circuit For The Determination Of The Driving Point Input Resistance, R_{in}. **(d).** Equivalent Circuit For Evaluating The Driving Point Output Resistance, R_{out}.

(2). In the "ohmmeter" model of Figure (1.28c), which pertains to the evaluation of the driving point input resistance, R_{in}, note that $V \equiv -V_x$. Hence,

$$V_x = R_o\left(I_x - \frac{V_x}{R_i} - g_m V_x\right) + R_l\left(I_x - \frac{V_x}{R_i}\right), \tag{E4-6}$$

whence

$$\boxed{R_{in} = \frac{V_x}{I_x} = \frac{\left(R_o + R_l\right)\|R_i}{1 + g_m R_o\left(\frac{R_i}{R_i + R_o + R_l}\right)}}. \tag{E4-7}$$

To the extent that $g_m R_o$ is a large number, the input resistance is relatively small and given approximately by

$$R_{in} \approx \frac{1}{g_m}\left(1 + \frac{R_l}{R_o}\right), \tag{E4-8}$$

which collapses to $R_{in} \approx 1/g_m$ for the typically encountered circumstance of $R_o >> R_l$.

(3). For the output resistance model in Figure (1.29d),

$$V = -R_s\left(\frac{V}{R_i} + I_x\right),$$

which implies

$$V = -\left(R_i \| R_s\right) I_x . \tag{E4-9}$$

Since

$$V_x = R_o\left(I_x - g_m V\right) - V = R_o I_x + \left(1 + g_m R_o\right)\left(R_i \| R_s\right) I_x ,$$

$$\boxed{R_{out} = \frac{V_x}{I_x} = \left(R_i \| R_s\right) + \left[1 + g_m\left(R_i \| R_s\right)\right] R_o .} \tag{E4-10}$$

The driving point output resistance is seen to be a number larger than R_o, which is itself presumably large. Indeed, R_{out} can be substantially larger than R_o, since a transconductor is routinely designed to ensure relatively large g_m and large R_i. Moreover, if the transconductor is driven by a current source, as indicated in Figure (1.29a), R_s is, like R_i and R_o, also a large resistance.

COMMENTS: The foregoing analyses confirm that the transconductor configuration in Figure (1.28a) is a reasonable approximation of an ideal current buffer. The approximation is good only if the subject transconductance element is designed to offer large input resistance *(R_i)*, large output resistance *(R_o)*, and reasonably large forward transconductance *(g_m)*. For these design constraints, the resultant input resistance of the buffer is small and roughly equal to the inverse of the transconductance of the transconductor, the output resistance is larger (and possibly significantly larger) than the transconductor output resistance, and the realized current transfer ratio is very near unity.

1.3.6. LOAD POWER CONSIDERATIONS

The principle purpose of a voltage buffer is to ensure the transfer of maximum voltage between a signal source and the load imposed on this source. On the other hand, a current buffer functions to effect maximum current transfer between source and load. Neither of these two buffers serves to transfer maximum power from signal -to- load. For example, the power, which is fundamentally the product of voltage and current, delivered by a signal source to the input port

of an ideal voltage buffer is zero because the infinitely large input impedance of this buffer precludes the flow of an input port current. Similarly, the power delivered to the input port of an ideal current buffer is zero by virtue of the fact that the zero input impedance indigenous to the current buffer precludes the establishment of a non-zero input port voltage. Obviously, practical buffers sustain non-zero input port power levels because their driving point input impedances are neither zero nor infinitely large. But well-designed voltage and current buffers certainly do not support input power levels that mirror the maximum power levels that applied signal source circuits are capable of generating.

Most digital electronic circuits and low -to- moderate frequency analog circuits and systems operate on applied signals whose implicit power levels are generally robust. As a result, the inherent inefficiency accompanying subcircuit, circuit, and subsystem interconnects that do not achieve the transfer of maximum signal power between a source and a load is of little, if any, concern in such applications. In other systems, such as high frequency and/or broadband communication electronics, signal power transfer is a major design issue because the available signal power levels are anemic. For example, consider the ubiquitous cellular telephone. The signal energy available at the antenna output terminals of a cell phone are typically so small as to be in danger of being masked by interference, or noise, generated either parasitically within the environment in which the cell phone operates or by the actual electronics used to detect, amplify, and otherwise process the antenna responses. Substantive signal power loss in this and analogous other applications must therefore be mitigated to maximize the likelihood of faithfully capturing and processing a low level signal in an unavoidably noisy electrical environment. To this end, care must be exercised to ensure that maximum signal power is indeed transferred to prescribed load terminations over the frequency response passband of interest. Stated quite simply, this means that for low level signal processing applications, maximum voltage transfer and maximum current transfer assume second place status to the fundamental design objective of assuring maximum signal power transfer.

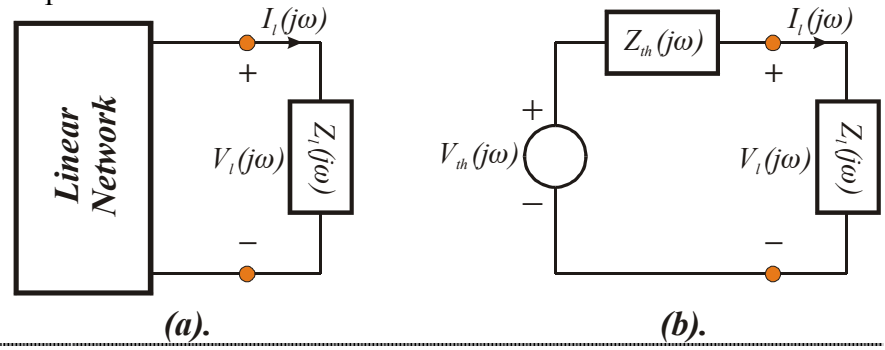


Figure (1.29). (a). A Linear Network Terminated In A Two Terminal Load Impedance, $Z_l(j\omega)$. The System Is Presumed To Operate In The Sinusoidal Steady State. **(b).** Thévenin Equivalent Circuit Of The System In (a).

The development of design criteria underlying the realization of maximum power transfer between a signal source and its imposed load commences with a study of the linear electrical system abstracted in Figure (1.29a). Assuming that the indicated linear network is excited by a sinusoid at radial frequency ω and that analytical attention focuses herewith on only steady state system performance, the pertinent Thévenin equivalent circuit is the model in Figure (1.29b). In the later diagram, $Z_l(j\omega)$ is the load impedance imposed on the linear network, $Z_{th}(j\omega)$ is the Thévenin impedance seen by this load, and $V_{th}(j\omega)$ is the phasor representation of the Thévenin

voltage that drives the two terminal load impedance branch. Without loss of generality, the phase angle of $V_{th}(j\omega)$ can be taken as zero, so that $V_{th}(j\omega)$ is the real number,

$$V_{th}(j\omega) = \sqrt{2}V_{trms}e^{j0} = \sqrt{2}V_{trms}\,, \tag{1-15}$$

where V_{trms} symbolizes the root mean square (RMS) value of the sinusoidal Thévenin voltage. For clarity, it should be understood that the time domain value, say $v_{th}(t)$, of this Thévenin voltage is

$$v_{th}(t) = \sqrt{2}V_{trms}\cos(\omega t)\,. \tag{1-16}$$

In response to the prevailing Thévenin voltage, a load voltage, $v_l(t)$, and a load current, $i_l(t)$, is established. Because of system linearity, both of these load variables are, like the applied Thévenin voltage, sinusoids at frequency ω. But depending on the nature of the load and Thévenin impedances in the circuit, the phase angles of these voltage and current variables are likely to be nonzero and non-identical. Thus,

$$v_l(t) = \sqrt{2}V_{lrms}\cos\left(\omega t + \theta_v\right) \tag{1-17}$$

and

$$i_l(t) = \sqrt{2}I_{lrms}\cos\left(\omega t + \theta_i\right), \tag{1-18}$$

where V_{lrms} and I_{lrms} are the RMS values of the load voltage and load current, respectively, while θ_v and θ_i denote the respective phase angles, measured with respect to the presumed phase angle of the input signal, of these variables. In phasor notation,

$$V_l(j\omega) = \sqrt{2}V_{lrms}e^{j\theta_v} \tag{1-19}$$

and

$$I_l(j\omega) = \sqrt{2}I_{lrms}e^{j\theta_i}\,. \tag{1-20}$$

The instantaneous power, $p_l(t)$, delivered to, and dissipated by, the load impedance is, using (1-17), (1-18), and a good old fashioned trigonometric identity, is

$$p_l(t) = v_l(t)\,i_l(t) = V_{lrms}I_{lrms}\left[\cos\left(\theta_v - \theta_i\right) + \cos\left(2\omega t + \theta_v + \theta_i\right)\right]. \tag{1-21}$$

The average power, say P_l, delivered to the load is found by integrating this instantaneous power over one complete period, $T = 2\pi/\omega$, of the sinusoidal load voltage or current and then dividing this integrated value by T. In particular

$$P_l = \frac{1}{T}\int_0^T p_l(t)\,dt = V_{lrms}I_{lrms}\cos\left(\theta_v - \theta_i\right). \tag{1-22}$$

Several insightful observations pertain to this result. First, a purely resistive load termination sustains a terminal voltage and branch current that are in phase with one another. Accordingly, $(\theta_v - \theta_i) = 0$, and the average power dissipated by the load collapses to simply the product of the RMS values of load voltage and load current. Second, it is well known that capacitors store the energy delivered to them but do not dissipate any average power. Since a strictly capacitive load supports a load voltage that lags its branch current by exactly $90°$, (1-22) confirms this zero

average power fact, since $(\theta_v - \theta_i) = -\pi/2$ radians, whence $\cos(\theta_v - \theta_i) = 0$. Similarly, for a load comprised of a pure inductance, which also dissipates no average power, $(\theta_v - \theta_i) = +\pi/2$, whence $P_l = 0$.

1.3.6.1. Maximum Power Transfer

As a prelude to determining the criteria for maximum power transfer between load and source, (1-22) must be related to the power made available by the Thévenin signal source circuit that drives the load impedance. To this end, it is initially convenient to express the average dissipated power defined by (1-22) in terms of phasor load variables. Note in (1-20) that the complex conjugate of the phasor load current is

$$I_l(-j\omega) = \sqrt{2}\, I_{lrms}\, e^{-j\theta_i} , \tag{1-23}$$

whereupon from (1-19),

$$\begin{aligned} V_l(j\omega)I_l(-j\omega) &= 2V_{lrms}I_{lrms}\, e^{j(\theta_v - \theta_i)} \\ &= 2V_{lrms}I_{lrms}\left[\cos(\theta_v - \theta_i) + j\sin(\theta_v - \theta_i)\right]. \end{aligned} \tag{1-24}$$

It follows from (1-22) that

$$P_l = \frac{1}{2} Re\left[V_l(j\omega)I_l(-j\omega)\right]. \tag{1-25}$$

An inspection of the circuit in Figure (1.29b) reveals a phasor load voltage of

$$V_l(j\omega) = \left[\frac{Z_l(j\omega)}{Z_l(j\omega) + Z_{th}(j\omega)}\right] V_{th}(j\omega) \tag{1-26}$$

and a phasor load current given by

$$I_l(j\omega) = \frac{V_{th}(j\omega)}{Z_l(j\omega) + Z_{th}(j\omega)}. \tag{1-27}$$

Decomposing the load and Thévenin impedances into their real (resistive) and imaginary (reactive) components,

$$Z_l(j\omega) = R_l + jX_l \tag{1-28}$$

and

$$Z_{th}(j\omega) = R_{th} + jX_{th} , \tag{1-29}$$

where it is understood that reactances X_l and X_{th} can be positive, negative, or zero, corresponding respectively to inductive, capacitive, or purely resistive impedances. On the other hand, R_{th} must be either a zero or a positive resistance for a strictly linear network, and R_l must be non-negative if $Z_l(j\omega)$ is a physically realizable passive load impedance. Inserting (1-28) and (1-29) into (1-26) and (1-27), and then substituting the resultant latter two expressions into (1-25), the average load power is found to be

$$P_l = \frac{1}{2}\frac{R_l\left|V_{th}(j\omega)\right|^2}{\left(R_l+R_{th}\right)^2+\left(X_l+X_{th}\right)^2}. \tag{1-30}$$

The preceding result comprises a useful engineering disclosure in that expresses the average steady state power dissipated in a complex load impedance in terms of load parameters and the Thévenin parameters of the linear network that drives the load. Interestingly enough, this power is reduced by load and Thévenin reactances despite the fact that such reactances are incapable of dissipating power. Fortunately, reactances can be positive or negative and thus, a first step toward maximizing the load power entails choosing a load impedance having $X_l = -X_{th}$. Thus, an inductive load requires a capacitive Thévenin impedance, and vice versa, for load power maximization. Under this power maximization constraint, (1-30) reduces to

$$P_l\big|_{X_l=-X_{th}} = \frac{R_l\left|V_{th}(j\omega)\right|^2}{2\left(R_l+R_{th}\right)^2}. \tag{1-31}$$

Clearly, the resultant load power displays a maximum with respect to the resistive component, R_l, of the load impedance, since the subject power is never negative and vanishes at both $R_l = 0$ and $R_l = \infty$. Remember that $V_{th}(j\omega)$ is discerned under an open circuit load condition and is therefore independent of all load parameters. The desired maximum can be determined by setting to zero the derivative of power with respect to R_l. When this analysis is executed, it is found that $R_l = R_{th}$ maximizes the power expression in (1-31), whence the maximum load power, say P_{lmax}, is

$$P_{lmax} = \frac{\left|V_{th}(j\omega)\right|^2}{8R_{th}} = \frac{V_{trms}^2}{4R_{th}}, \tag{1-32}$$

where (1-15) is used. Observe that the combined constraints, $R_l = R_{th}$ and $X_l = -X_{th}$, that lead to (1-32) imply a load impedance that is the complex conjugate of the Thévenin impedance, $Z_{th}(j\omega)$, of the linear network; that is,

$$Z_l(j\omega) \equiv Z_{th}(-j\omega). \tag{1-33}$$

Equation (1-33) defines the design condition commensurate with the transfer of maximum power between signal and load. When it is satisfied, the terminating load impedance is said to be ***match terminated*** to the source, and the equation itself is often referred to as the ***match terminated design condition***. The resultant maximum average power delivered to the load termination is given by (1-32), which, in effect, also stipulates the maximum power capability of the signal source.

1.3.6.2. The dBm Power Measure

The maximum signal power levels routinely encountered in such low level electronics as audio preamplifiers, video amplifiers, and radio frequency (RF) communication networks are rarely larger than a few milliwatts. In many communication circuits, such as those exploited as first stages in cellular telephones, these power levels can be as small as only hundreds of picowatts. To illustrate, consider the simplified system level diagram of the front end of a high frequency communications receiver shown in Figure (1.30a). In this diagram, the antenna is the medium by which the signal earmarked for ultimate signal processing is captured. This antenna

is coupled electrically to the input port of the first stage, or front end, amplifier of the communication cell by a cable or some other form of distributed transmission line that, under certain designable conditions, is characterized by a *50 Ω*, purely resistive impedance. As suggested in Figure (1.30b), the input port of the amplifier is driven by a simple Thévenin equivalent circuit consisting of the Thévenin antenna voltage, $V_{th}(j\omega)$, and a Thévenin *50 Ω* resistance, R_{th}, established by the transmission line interconnect. A match termination to this signal source medium therefore mandates an amplifier input impedance, Z_{in}, that is purely real and identical to *50 Ω*. Assuming a RMS Thévenin signal of *300 μV*, the available antenna signal power, and the signal power actually delivered to the amplifier when its input port displays a driving point impedance of $Z_{in} = 50\ \Omega$, is, by (1-32), $P_{lmax} = (300\ \mu V)^2/(4)(50) = 450\ pW$.

Signal power levels that are so low as the level just computed are commonly expressed as a normalized power in units of ***decibels referred to a milliwatt***, or simply, ***dBm***. For a signal power of P, the *dBm* value of P is

$$P\ (in\ dBm) = 10 log_{10}\left(\frac{P}{0.001}\right). \tag{1-34}$$

A logarithmic multiplier of *10* is used in this definition, as opposed to the multiplier of *20* invoked in Example (1.1), because power is proportional to the square of either voltage or current. Thus, (1-34) is equivalent to a *20-times* logarithm of voltage or current response. For the previously computed P_{lmax} of *450 pW*, $P_{lmax} = -63.47\ dBm$, and it is therefore inferred that the indicated maximum load power is about *63.5 dB below a milliwatt*. Note, for example, that *0 dBm* corresponds to a signal power of *one milliwatt*, which is equivalent to *223.6 mV* of RMS voltage established across *50 ohms* of resistance.

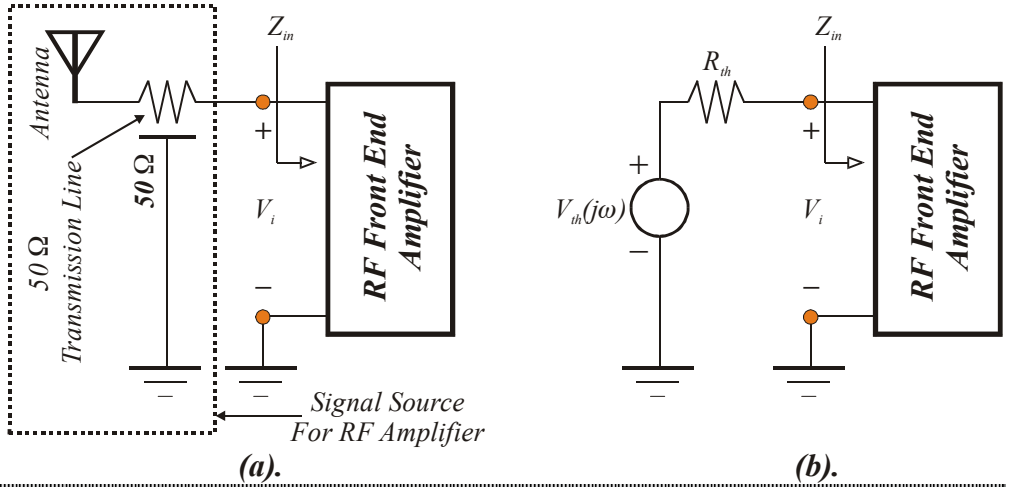


Figure (1.30). (a). Simplified System Level Diagram Of The Antenna Signal Source And Front End (First Stage) Amplifier Of A Communication Network. **(b).** The System In (a) With The Antenna Signal Source Replaced By Its Thévenin Equivalent Network.

1.3.6.3. Match Termination and Tuned Responses

Matched terminated loads comprise an effective vehicle for capturing the maximum signal power that an energy source is capable of delivering. But in the absence of design heroics that entail the incorporation of reasonably complex filters in the signal flow path of an electronic system, impedance matches can generally be effected at only a single frequency and at best, only

over a restricted frequency passband that is geometrically centered about this so called ***center frequency***. This operational circumstance provides the engineering backdrop for ***tuned amplifiers*** or in general, for electronic systems exhibiting ***bandpass frequency responses***. ***Bandpass amplifiers*** provide zero gain at both low and high frequencies and offer nonzero gain in only the immediate neighborhood of the center frequency to which the system is ***tuned***.

To illustrate the limitations and attributes of match terminated amplifier design, consider the system in Figure (1.31a). The diagram at hand depicts a signal source represented by its Thévenin equivalent circuit consisting of the series interconnection of the voltage phasor, V_s, and the resistance, R_s, applied to the input port of a transimpedance amplifier. For the purpose of this discussion, the subject amplifier is terminated at its output port in resistance R_l, has a frequency invariant transresistance, r_m, and a purely real output impedance, r_o. Moreover, the transimpedance unit, as is the case with many practical realizations of such cells, has a driving point input impedance that can be represented as a series connection of a small resistance, R_i, and an inductance, L_i. Because of the desire to match terminate the front end of the indicated system, a capacitor, C_s, is inserted in series with the Thévenin source resistance, R_s. The electrical model corresponding to the foregoing stipulations is the topology depicted in Figure (1.31b).

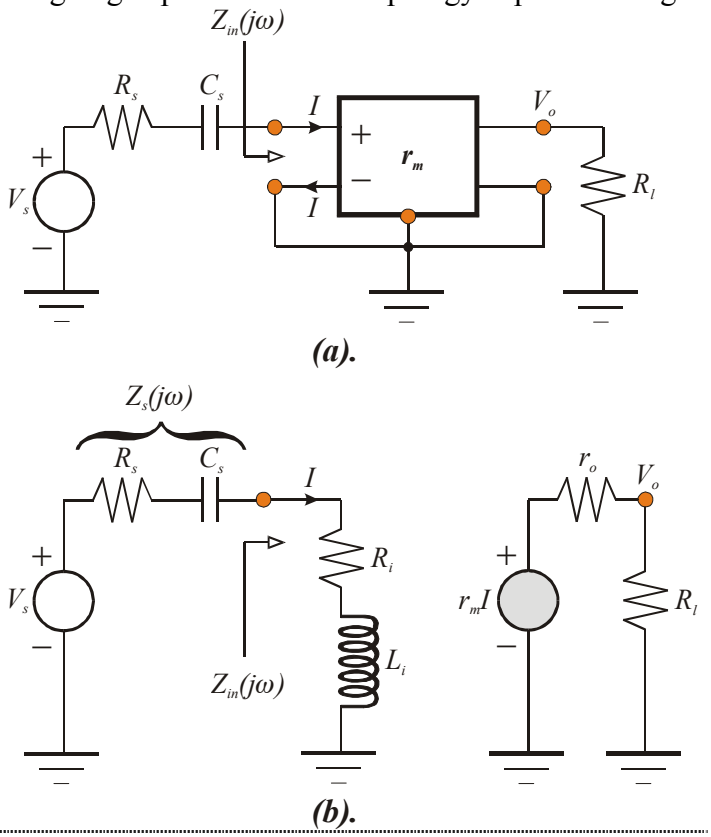


Figure (1.31). (a). System Level Diagram Of A Tuned Transimpedance Amplifier. **(b).** Electrical Model Of The System In (a).

An inspection of Figure (1.31b) suggests an effective source impedance of $Z_s(j\omega) = R_s - j/\omega C_s$, and an effective driving point amplifier input impedance of $Z_{in}(j\omega) = R_i + j\omega L_i$. Match terminated operation at the front end therefore requires $R_i = R_s$ and $(1/\omega C_s) = \omega L_i$. The latter of these two mandates can be satisfied at only one frequency, the center frequency, ω_o, such that

$$\omega_o = \frac{1}{\sqrt{L_i C_s}} . \tag{1-35}$$

Armed with this result and the requirement, $R_i = R_s$, KVL applied to the input loop of the model in Figure (1.31b) yields

$$I = \frac{V_s}{R_s + \frac{1}{j\omega C_s} + R_i + j\omega L_i} = \frac{V_s}{2R_s + j\omega_o L_i \left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega} \right)} . \tag{1-36}$$

At the center frequency. current I is simply $V_s/2R_s$, which is as expected since at $\omega = \omega_o$, $(1/j\omega_o C_s) + j\omega_o L_i = 0$; that is, the inductive impedance is precisely the negative of the capacitive impedance at the center frequency of the input port. Moreover, (1-36) confirms that I reduces to zero at both very low and very high frequencies. This observation mirrors engineering expectations since at very low frequencies, the capacitor is effectively an open circuit, while at very high signal frequencies, the inductor behaves as an open circuit.

The voltage gain, $A_v(j\omega)$, of the network follows forthwith from Figure (1.31b) and (1-36) as

$$A_v(j\omega) = \frac{V_o}{V_s} = \frac{V_o}{I} \times \frac{I}{V_s} = \left(\frac{R_l}{R_l + r_o} \right) \left(\frac{\frac{r_m}{2R_s}}{1 + jQ_o \left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega} \right)} \right) , \tag{1-37}$$

where

$$Q_o = \frac{\omega_o L_i}{2R_s} = \frac{\sqrt{L_i / C_s}}{2R_s} \tag{1-38}$$

is known as the ***quality factor***, or simply the *"Q,"* of the input port circuit. Note that the quality factor is little more than a comparison of the inductive reactance at the center frequency -to- the net series resistance in the electrical loop in which the inductance is embedded. In practice, this "net series resistance" also includes the parasitic resistance unavoidably implicit to the conductive coil or metallization winding that comprises the inductor. Because this undesirable resistance can be lumped into the effective source resistance, R_s, Q_o in (1-38) diminishes and therefore, the reactive impact, or "quality" of the inductive coil is impaired.

Equation (1-37) confirms that the voltage gain at the tuned center frequency of the system in Figure (1.31) is

$$A_v(j\omega_o) = \left(\frac{R_l}{R_l + r_o} \right) \frac{r_m}{2R_s} . \tag{1-39}$$

This gain is the maximum available voltage gain since the magnitude of the gain in (1-37) decreases for both $\omega > \omega_o$ and $\omega < \omega_o$. It is important to understand that high frequency gain deterioration is the result of the limited input port current caused by high inductive impedance. On the other hand, low frequency gain degradation is attributed to the high capacitive impedance in the input port of the transimpedance amplifier.

The resultant bandpass frequency response is illustrated in Figure (1.32), which plots the normalized voltage gain magnitude,

$$|A_n(j\omega)| \triangleq \left|\frac{A_v(j\omega)}{A_v(j\omega_o)}\right| = \left|\frac{1}{1+jQ_o\left(\frac{\omega}{\omega_o}-\frac{\omega_o}{\omega}\right)}\right| = \frac{1}{\sqrt{1+Q_o^2\left(\frac{\omega}{\omega_o}-\frac{\omega_o}{\omega}\right)^2}}, \qquad (1\text{-}40)$$

-versus- the normalized signal frequency,

$$x = \omega/\omega_o \equiv f/f_o, \qquad (1\text{-}41)$$

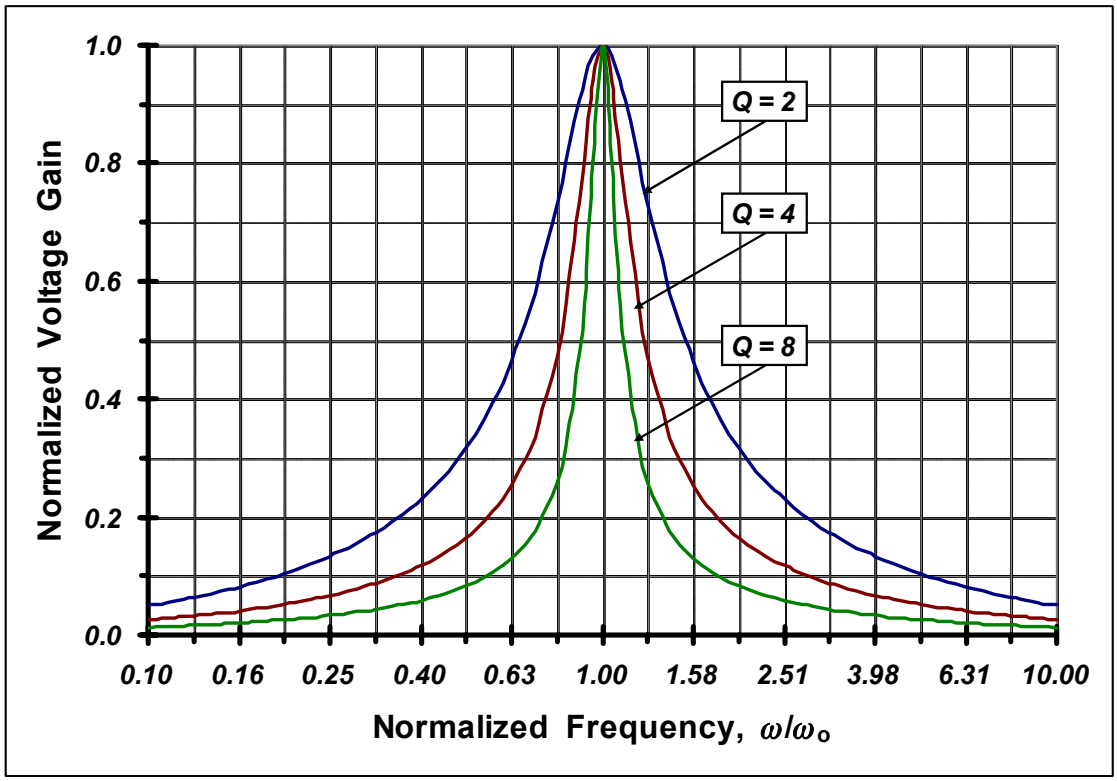


Figure (1.32). Frequency Response Of The Tuned Transimpedance Amplifier In Figure (1.31) For Various Values Of The Quality Factor For The Source/Input Port Circuit.

for various values of quality factor Q_o. Independent of Q_o, the normalized gain magnitude is one at the tuned frequency, ω_o, and falls off with frequency both above and below ω_o. The rate at which the magnitude rolls off with signal frequency is strongly influenced by Q_o. In particular, progressively larger quality factors result in increased rates of frequency response roll off and give less nebulously defined, crisper tuning at the center frequency.

At first blush, the limited frequency range over which substantive gains are possible in a tuned amplifier appear disadvantageous. Indeed, this narrowband response is a shortfall in applications that mandate circuit processing over broad frequency passbands. In other applications, and notably in commercial communications, narrow banding offers distinct operational advantages. One such advantage is that while a tuned electronic network assuredly amplifies signals whose frequencies are in the immediate neighborhood of the center frequency, ω_o, it implicitly rejects proximate frequencies, thereby minimizing potential interference incurred by undesirable, but nonetheless, unavoidable signal energies at frequencies proximate to the tuned

center frequency. This property is essential in commercial radio or television, wherein tuning to one broadcast station should preclude reception of another station that is broadcasting at a frequency near to that which is being received. For example, with $Q_o = 8$, a signal at a frequency that is one octave above ω_o (meaning twice as large as ω_o) has a normalized gain of *0.083*. In comparison to the gain available at ω_o, the signal at frequency $2\omega_o$ is therefore attenuated by about *21.6 dB*, or by a factor of roughly *12*. Accordingly, this higher frequency signal may not pose a significant interference problem with respect to the signal at ω_o. A second advantage embraces electrical noise, to which the reader is exposed in due time. For the present, suffice it to say that the amount of random, spurious, electrical noise indigenous to an amplifier determines the minimum signal that can be faithfully detected, captured, and amplified by the utilized electronics. For progressively larger levels of electrical noise, applied input signals must be commensurately larger to ensure their accurate detection. As it materializes, such noise levels are directly proportional to the passband of the network frequency response. It follows that narrowband electronic systems are generally more capable of processing low-level signals than are otherwise comparable broadband systems.

Like the passband of a lowpass network, the passband of a tuned, or bandpass, system is defined as the frequency range over which the observable gain is within three decibels of the maximum available gain. In bandpass electronics, however, two *3-dB* frequencies are evident, as is illustrated in Figure (1.33). In the subject diagram, which plots normalized gain magnitude as a function of normalized frequency, the *3-dB* frequencies are defined as those frequencies for which the gain magnitude is the inverse of root two, or *0.707*. To this end, a higher than ω_o frequency, ω_2, and a lower than ω_o frequency, ω_1, are evidenced at the *3-dB* down points. Since the normalized gain magnitude is the inverse of root two when the imaginary term coefficient on the right hand side of (1-40) is either plus one or negative one,

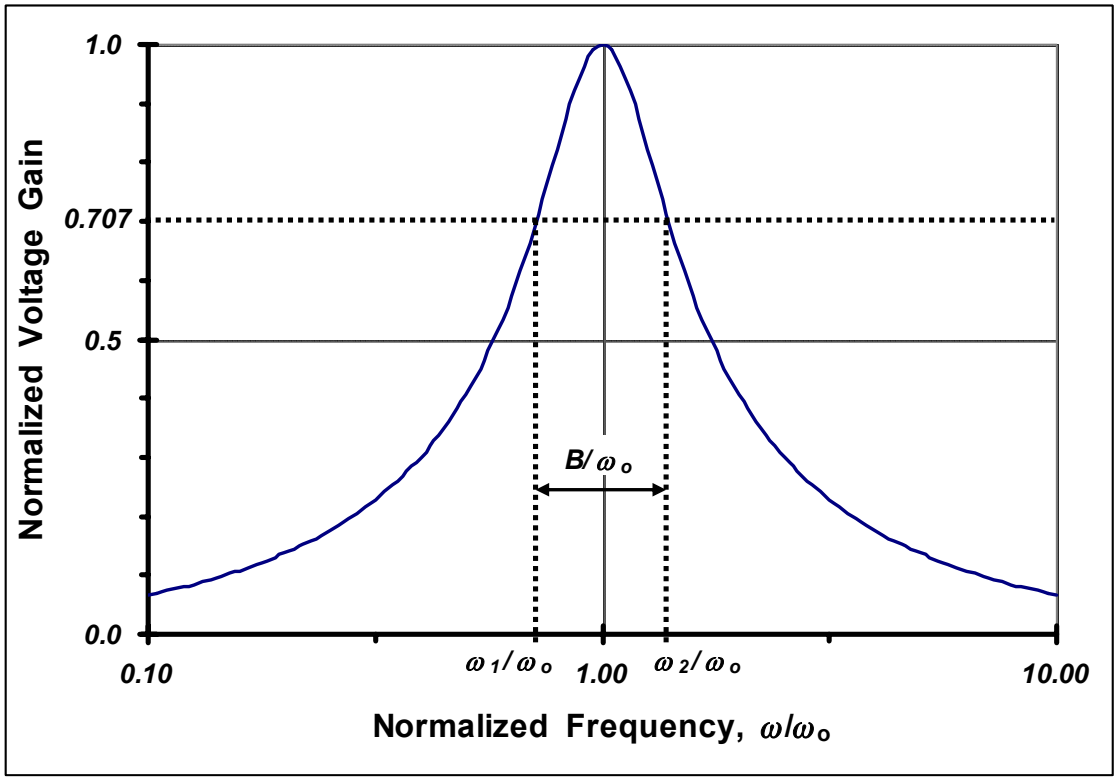


Figure (1.33). Generalized Version Of The Frequency Response For The Tuned Amplifier In Figure (1.31). The Plot Conceptually Illustrated The Calculation Of The Circuit *3-dB* Bandwidth.

$$Q_o\left(\frac{\omega_2}{\omega_o}-\frac{\omega_o}{\omega_2}\right) = 1\ , \tag{1-42}$$

and

$$Q_o\left(\frac{\omega_1}{\omega_o}-\frac{\omega_o}{\omega_1}\right) = -1\ . \tag{1-43}$$

Solving these two equations for ω_2 and ω_1, respectively (both of which must be positive numbers),

$$\omega_2 = \frac{\omega_o}{2Q_o}\left(\sqrt{1+4Q_o^2}+1\right), \tag{1-44}$$

$$\omega_1 = \frac{\omega_o}{2Q_o}\left(\sqrt{1+4Q_o^2}-1\right). \tag{1-45}$$

It follows that the *3-dB* bandwidth, B, is

$$B = \omega_2-\omega_1 = \frac{\omega_o}{Q_o}\ , \tag{1-46}$$

which supports an earlier contention of relative tuning sharpness with increasing circuit quality factor.

Interestingly enough, these results also suggest that

$$\omega_o = \sqrt{\omega_1\,\omega_2}\ ; \tag{1-47}$$

that is, the center frequency is the geometric mean of the two *3-dB* frequencies. However for very large Q_o, (1-44) and (1-45) give

$$\begin{aligned}\omega_2 &\approx \omega_o+\frac{\omega_o}{2Q_o} = \omega_o+\frac{B}{2}\\ \omega_1 &\approx \omega_o-\frac{\omega_o}{2Q_o} = \omega_o-\frac{B}{2}\end{aligned}\ , \tag{1-48}$$

which collectively depict ω_o as an approximate arithmetic mean of the upper and lower *3-dB* frequencies.

1.4.0. SECOND ORDER CIRCUITS AND SYSTEMS

Although first order circuits containing but a single energy storage element, such as those addressed in Examples (1.1), (1.2), and (1.3), are relatively straightforward to analyze and assess, most electronic circuits and systems contain a multiplicity of energy storage elements and are therefore multi order in nature. Circuits whose transfer functions exhibit several poles and zeros are cumbersome to analyze and as a result, an engineering evaluation of their performance attributes and limitations can be a daunting undertaking. Fortunately, the salient properties of these high order circuits and systems can often be represented by second order mathematical

models. Although these second order approximations are mathematically and topologically more intricate than are their first order counterparts, they do produce response estimates that, when carefully interpreted in light of all invoked approximations, track satisfactorily with the observable behavior of the circuits and systems they model.

The disclosure cited above comprises a sufficient reason to establish an adequate comfort level with the frequency and time domain electrical characteristics of second order networks. An additional justification for second order studies is that a broad class of programmable and reconfigurable electronic filters, known as ***biquadratic filters***, are implemented as cascade interconnections of second order structures. These filters can be synthesized for virtually any type of requisite frequency response. For example, they can be bandpass units, such as the network in Figure (1.31), which attenuate all signal frequencies except those that lie in the immediate neighborhood of a desired tuned center frequency. They can exhibit lowpass response properties, wherein low signal frequencies are processed with relatively constant gain, but high frequency signals are attenuated. The result is a reduction of potential high frequency interference threats imposed on an otherwise low -to- moderate frequency signal processor. Highpass biquadratic filters are the converse of lowpass architectures; that is, highpass units attenuate low frequencies while processing high frequencies with nominally constant gain. Finally, biquadratic filters can be realized as notch filters, which are the converse of bandpass units. They process all signal frequencies except those in the neighborhood of a center frequency. A common application of a notch filter entails the mitigation of the annoying *60-cycle* "hum" evidenced in sensitive electronic units that are energized by conventional *60-Hz* sinusoidal electric power.

1.4.1. SECOND ORDER FILTERS

Although filters are not the dominant focus of this discussion, they do provide a convenient vehicle for demonstrating the practical realization of a second order circuit. To this end, consider the lowpass active filter depicted in Figure (1.34), which utilizes four *(4)* single ended transconductors, or OTAs, and two *(2)* capacitors. In the interest of analytical simplicity, the four transconductors are taken herewith to be ideal; that is, each has infinitely large input impedance, infinitely large output impedance, and constant, frequency independent transconductance. The initial objective herewith is a delineation of the transfer function, $H(s) = V_o/V_s$, of the filter. To this end, the concepts set forth by the idealized transconductor model in Figure (1.18b) allow for the stipulation of the key circuit branch currents indicated in the subject schematic diagram. For example, since no current flows into the input port of an ideal transconductor, the input port voltage, measured from non-inverting -to- inverting terminals, of the transconductor on the far left of the diagram is the signal source voltage, V_s. Accordingly, the current flowing into the output port of this active element is simply $g_{ma}V_s$. If the output port voltage of the second transconductor (transconductance of g_{mb}) is denoted as V_i, the feedback around this element forces the input port voltage to mirror V_i, whence an output port current flowing into the transconductor of $g_{mb}V_i$. The transconductor symbolized as g_{m1} has a resultant input port voltage of $(V_o - V_i)$, which produces an output port current of $g_{m1}(V_o - V_i)$. This output current is constrained to flow through the capacitance, C_1, because the subsequent transconductor (labeled g_{m2}) conducts zero input current. Finally, if the voltage developed across capacitance C_1 is symbolized as V_x, the input port voltage to the transconductor labeled g_{m2} is $(V_x - V_o)$, polarized from the inverting terminal -to- the non-inverting terminal. Consequently, an output port current of $g_{m2}(V_x - V_o)$ flows out of the output port of the transconductance element on the far right of the subject sche-

matic diagram. This current is forced to flow through the capacitance, C_2, because zero current is drawn by the non-inverting input terminals of the third and fourth transconductors.

Nodal analysis applied to the output terminal of the g_{ma}–transconductor stipulates $g_{ma}V_s + g_{mb}V_i = 0$, whence

$$\frac{V_i}{V_s} = -\frac{g_{ma}}{g_{mb}} . \tag{1-49}$$

Before proceeding with the analysis, it is instructive to understand that the g_{mb}–transconductor functions as a load that presents an effective resistance of $(1/g_{mb})$ to a phase inverting transconductor amplifier whose transconductance is g_{ma}. In support of this contention, Figure (1.35a) is submitted to posture the second transconductor of the filter in Figure (1.34) in a form appropriate to determining the effective resistance, V_i/I_i, established across the terminals of this subcircuit. Using Figure (1.18b), the pertinent model is the structure depicted in Figure (1.35b), which verifies that $I_i = g_{mb}V_i$ and hence, $V_i/I_i = 1/g_{mb}$. It follows that the cascade of the first two transconductors in the filter at hand is electrically equivalent to the macromodel offered in Figure (1.35c), whose voltage gain clearly subscribes to (1-49).

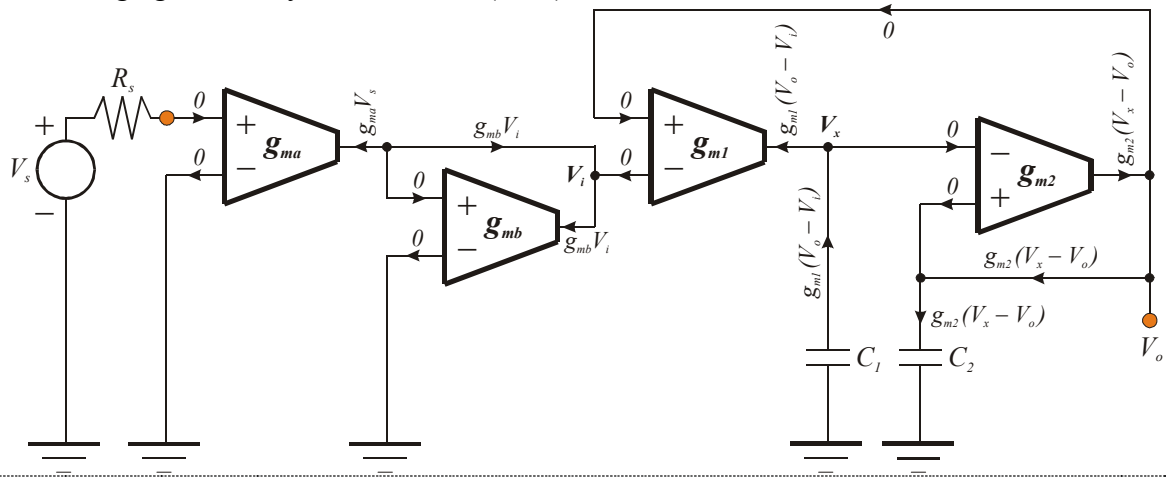


Figure (1.34). Schematic Diagram Of A Second Order Lowpass Filter Realized With Single Ended Operational Transconductor Amplifiers (OTAs).

Having established that the g_{mb}–transconductor in Figure (1.34) merely emulates a two terminal resistance, questions naturally arise as to the propriety of using this active subcircuit when, in fact, a simple resistor whose resistance value is numerically equal to $(1/g_{mb})$ ostensibly suffices. To be sure, the simple resistance approach may be preferred in numerous applications because of noise, power dissipation, linearity, and other considerations. But one advantage to actively realizing the required terminating resistance is the ability to adjust actual resistance value electronically. Specifically, the value of OTA transconductance, g_{mb}, can be varied over at least a small range of values by adjusting the biasing voltages applied to the OTA. In general, ***biasing*** (not shown in the schematic diagrams) consists of one or more constant (or static) voltages appropriately applied to the transconductor amplifier to ensure its reasonably linear signal processing performance over the requisite range of signal amplitudes and frequencies. In effect, the g_{mb}–transconductor functions as a kind of electronic potentiometer, thereby allowing the design engineer to fine tune, or "tweak," the nominal design to achieve desired performance in the face of parametric device, circuit, or system uncertainties.

Returning to the analysis problem, the current conducted by capacitance C_1 is

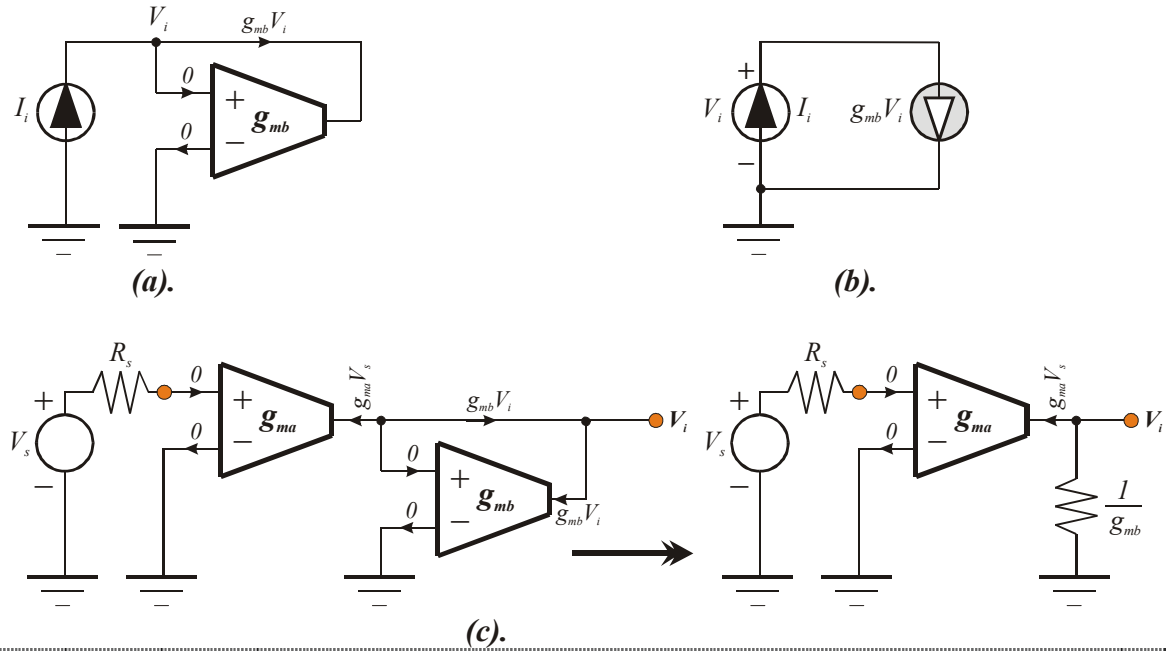


Figure (1.35). (a). Subcircuit Consisting Of The Second Transconductance Unit In The Filter Of Figure (1.34). **(b).** Electrical Model For Determining The Terminal Resistance Of The Subcircuit In (a). **(c).** Subcircuit Consisting Of The First Two Transconductance Element Stages In The Filter Of Figure (1.34). The Representation Suggests That The Second Transconductance Unit Functions As an Equivalent, Two Terminal Resistance.

$$sC_1V_x = -g_{m1}\left(V_o - V_i\right), \tag{1-50}$$

while capacitor C_2 conducts

$$sC_2V_o = g_{m2}\left(V_x - V_o\right). \tag{1-51}$$

Upon elimination of the voltage variable, V_x, from these two relationships, the voltage ratio, V_o/V_i, is found to be

$$\frac{V_o}{V_i} = \frac{1}{1 + \dfrac{sC_1}{g_{m2}} + \dfrac{s^2C_1C_2}{g_{m1}g_{m2}}}, \tag{1-52}$$

which is clearly a second order transfer function. Recalling (1-49), the desired transfer function is

$$H(s) = \frac{V_o}{V_s} = \frac{V_o}{V_i}\times\frac{V_i}{V_s} = -\frac{g_{ma}/g_{mb}}{1 + \dfrac{sC_1}{g_{m2}} + \dfrac{s^2C_1C_2}{g_{m1}g_{m2}}}. \tag{1-53}$$

Equation (1-53) renders immediately transparent the fact that the zero frequency gain, $H(0)$, of the active filter in Figure (1.34) is

$$H(0) = -\frac{g_{ma}}{g_{mb}}. \tag{1-54}$$

The negative algebraic sign in this result indicates phase inversion between the input and output ports. This is to say that a rising input signal over time results in an amplified, but decreasing output signal in the steady state. Conversely, a decreasing input is accompanied by an increasing steady state response. Since capacitors behave as open circuits for steady state, zero frequency inputs, the current conducted by C_1 at zero frequency is necessarily zero. By (1-50), this fact forces $V_o \equiv V_i$, whence (1-49) is seen to corroborate with (1-54).

In an attempt to garner insights about the responses evidenced by second order networks, it is expedient to write the second order transfer relationship of (1-53) in one of the two traditional generalized forms,

$$H(s) = \frac{H(0)}{1 + \frac{2\zeta s}{\omega_n} + \frac{s^2}{\omega_n^2}}, \tag{1-55}$$

or

$$H(s) = \frac{H(0)}{1 + \frac{s}{Q\omega_n} + \frac{s^2}{\omega_n^2}}, \tag{1-56}$$

where $H(0)$ symbolizes the circuit gain at zero signal frequency, which in this case is given by (1-54). Parameter ω_n is termed the ***undamped natural frequency of oscillation***, or the ***undamped self-resonant frequency***, of the system under consideration. A comparison of (1-55) or (1-56) with (1-53) suggests that for the filter at hand, ω_n (in units of radians -per- second) is

$$\omega_n = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}. \tag{1-57}$$

Moreover, ζ is called the ***damping factor*** of the system, while Q is termed the system ***quality factor***. From (1-55), (1-56), and (1-53),

$$\frac{2\zeta}{\omega_n} = \frac{1}{Q\omega_n} = \frac{C_1}{g_{m1}}, \tag{1-58}$$

whence, by (1-57),

$$\zeta = \frac{1}{2Q} = \frac{1}{2}\sqrt{\frac{g_{m2}C_1}{g_{m1}C_2}}. \tag{1-59}$$

The engineering significance of damping factor ζ and of undamped self-resonant frequency ω_n is clarified by the subsections that follow. For the moment, suffice it to say that for nonzero damping factor, ω_n is a measure of the circuit *3-dB* bandwidth. This is to say that for $\zeta \neq 0$, large ω_n produces large bandwidth, while small ω_n results in small circuit bandwidth. On the other hand, damping factor ζ is a measure of the ***stability*** of the circuit undergoing investigation. A stable linear circuit can be interpreted herewith as implying a circuit that is capable of establishing a steady state output response that is exclusively determined by, and linearly proportional to, the steady state input signal. A stereo amplifier is presumably stable since it delivers an electrical response to its connected speakers that is linearly related to the electrical signal established

at the output terminals of a compact disc player, despite any interference caused by minor disc imperfections, local fluorescent lighting, or proximately operated household appliances. It is shown shortly that a negative damping factor is disastrous from a stability perspective. On the other hand, large ζ ensures consummate stability at the expense of a system inability to achieve steady state operation quickly. Damping factors slightly less than one offer the best compromise between adequate stability margins and expeditious response speeds.

1.4.2. FREQUENCY RESPONSE

The frequency response is a traditional metric for evaluating the steady state performance of a linear circuit or system. This graphical tool effectively provides a snapshot of the manner in which the gain magnitude varies in the steady state with the frequency of an applied input sinusoid. An even cursory inspection of the frequency response therefore conveys information as to whether the circuit or system gain is too small or too large at certain signal frequencies, whether the gain is increasing too fast or too slowly over a range of frequencies, and whether the rate at which the gain magnitude diminishes with frequency is too dramatic.

Analytically, a frequency response study of a generalized lowpass second order network begins by supplanting the Laplace variable, s, in (1-55) by $j\omega$, since steady state responses to applied sinusoids are the order of the business at hand. In order to minimize algebra and forge analytical efficiency, it is convenient both to normalize the transfer function to its zero frequency gain and to normalize the signal frequency to the undamped self-resonant frequency. Accordingly, let the normalized transfer function, $H_n(j\omega)$, be

$$H_n(j\omega) \triangleq \frac{H(j\omega)}{H(0)}, \tag{1-60}$$

and the normalized frequency, x, be

$$x \triangleq \frac{\omega}{\omega_n}. \tag{1-61}$$

Then (1-55) can be recast as

$$H_n(jx) = \frac{1}{1 - x^2 + j2\zeta x}, \tag{1-62}$$

whose magnitude is

$$\left|H_n(jx)\right| = \frac{1}{\sqrt{\left(1 - x^2\right)^2 + \left(2\zeta x\right)^2}}. \tag{1-63}$$

Figure (1.36) plots the decibel value of the normalized gain magnitude delineated in (1-63) (*20-times* the base *10* logarithm of the magnitude) as a function of the normalized signal frequency for several values of the damping factor, ζ. Ideally, the normalized frequency response is a constant *0 dB*, which is indicative of a constant gain in the amount of the "DC" gain, *H(0)*, over a frequency passband stretching from essentially zero frequency -through- to the *3-dB* bandwidth of the circuit undergoing scrutiny. Obviously, the responses depicted in Figure (1.36) are far from ideal. One observable problem is that considerable response peaking is evidenced for small damping factors. For example, $\zeta = 0.05$ results in a *20-dB* peak, which implies that the network

gain magnitude at some relatively high signal frequency is *10-times* larger than the zero frequency gain. A slightly larger than *8-dB* peak materializes for $\zeta = 0.2$.

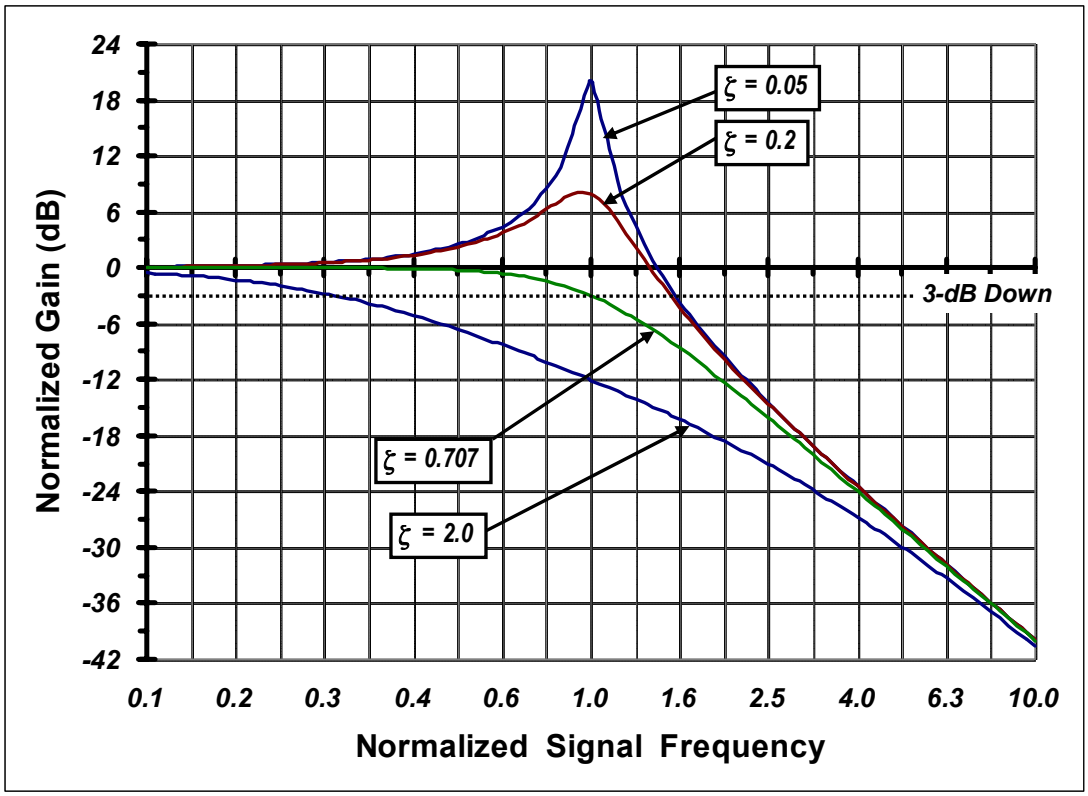


Figure (1.36). Frequency Response Of A Generalized, Lowpass Second Order Circuit. The Gain Scale Is Normalized To The Zero Frequency Gain Of The Circuit. The Frequency Scale Is Normalized To The Undamped Self-Resonant Frequency Of The Network.

Excessive response peaking in lowpass configurations is undesirable for at least two reasons. First, such peaking accents high frequency signal amplitudes, while amplifying low frequencies with relatively constant, and often considerably smaller, gain. In a stereo system, the indicated peaking would result in shrill treble responses and anemic base responses. A second, and more alarming, consequence of excessive response peaking is the potential system instability it implies. For example, if ζ were to be nulled, (1-63) shows infinitely large gain magnitude at $x = 1$, which is equivalent to asserting infinitely large gain at the undamped (meaning $\zeta = 0$) self-resonant frequency. Infinitely large gain magnitude in the presence of finite output responses means that the network is curiously generating a response without a driving forcing function. As astonishing as this circumstance appears to be, it can happen in poorly designed electronics for which the interaction of high order energy storage parasitics with network gain elements reduce the effective circuit damping factor to zero. The network for which $\zeta = 0$ is said to oscillate, and since the infinitely large gain that results in a finite output response for zero inputs occurs at only the frequency, ω_n, the subject oscillatory response is a sinusoid of frequency ω_n.

1.4.2.1. Response Peaking

Because excessive peaking of the frequency response is undesirable and generally indicative of potential instability problems, exploring design-oriented means to avoid such peaking is a prudent undertaking. Steady state frequency response peaking is accompanied by a magnitude response that projects zero slope in the frequency domain. Accordingly, return to (1-

63) and determine the value, say x_p, of the normalized frequency variable, x, where the derivative of the magnitude response with respect to x is zero; that is,

$$\left.\frac{d\left|H_n(jx)\right|}{dx}\right|_{x=x_p} = \left.\frac{d}{dx}\left[\frac{1}{\sqrt{\left(1-x^2\right)^2+\left(2\zeta x\right)^2}}\right]\right|_{x=x_p} = 0 . \tag{1-64}$$

The execution of this admittedly sloppy task results in two solutions for x_p; namely, $x_p = 0$ and

$$x_p \triangleq \frac{\omega_p}{\omega_n} = \sqrt{1-2\zeta^2} = \sqrt{1-\frac{1}{2Q^2}} , \tag{1-65}$$

where ω_p symbolizes the radial frequency corresponding to zero frequency domain slope of the magnitude characteristic. The solution, $x_p = 0$, bodes no particular significance other than reaffirming the expectation of nominally constant gain in the immediate neighborhood of zero signal frequency. Equation (1-65) is the interesting solution in that it implies a second frequency at which zero slope is evidenced. The existence of this second solution implies a frequency response that does not diminish monotonically as the signal frequency increases from zero. However, note that for $\zeta > 1/\sqrt{2}$, or equivalently, $Q < 1/\sqrt{2}$, x_p in (1-65) is an imaginary number, which suggests that no real second frequency of zero magnitude response slope exists; in other words, no response peaking can be observed. In support of this disclosure, observe further that $x_p \equiv 0$ if ζ or Q is precisely $1/\sqrt{2}$. The constraint, $\zeta = 1/\sqrt{2}$, is therefore understandably referred to as the condition for ***maximally flat magnitude (MFM)*** frequency response in that it produces zero slope in the magnitude response at only a single frequency which is, in fact, zero frequency.

The solution in (65) can be plugged into (1-63) to ascertain the peak value, say M_p, of the frequency response magnitude at non-zero frequency. Biting this proverbial algebraic bullet results in

$$M_p = \frac{1}{2\zeta\sqrt{1-\zeta^2}} = \frac{Q}{\sqrt{1-\left(\frac{1}{2Q}\right)^2}} . \tag{1-66}$$

It should be understood that (1-66) is applicable only for $0 < \zeta \le 1/\sqrt{2}$ or equivalently, for $1/\sqrt{2} \ge Q < \infty$, which ensure that x_p in (1-65) is a real number. Figure (1-37) graphically depicts both the dependence of response peak and the frequency corresponding to response peaking on circuit quality factor.

1.4.2.2. Bandwidth

A common misperception of the maximally flat magnitude condition is that the MFM response yields maximal *3-dB* bandwidth. Figure (1.36) confirms otherwise and shows that substantive bandwidth increases can be attained through a reduction in circuit damping factor. The generally unacceptable price paid for this bandwidth enhancement is progressively more pronounced response peaking.

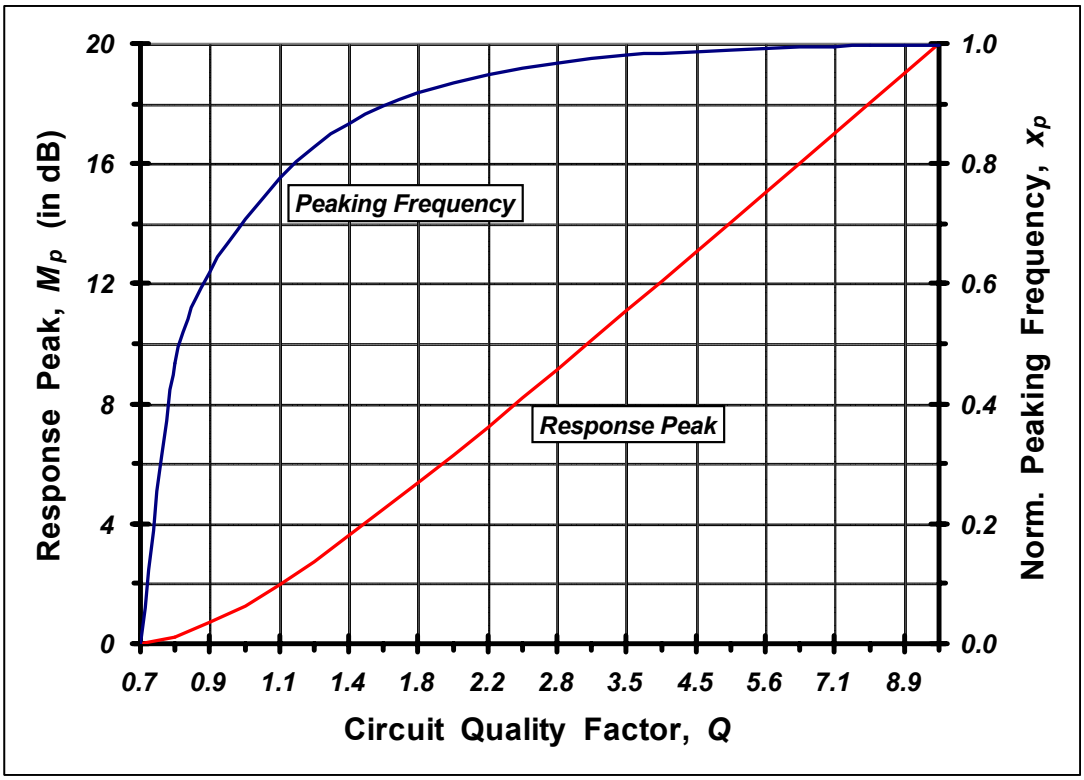


Figure (1.37). Peak Transfer Function Magnitude And The Normalized Frequency At Which Peaking Is Evidenced For a Second Order Network As A Function Of The Network Quality Factor.

The dependence of the *3-dB* bandwidth on network damping factor can be discerned through another return to (1-63). In this case, the analytical objective is the value, say x_b, of the normalized frequency that results in a normalized transfer function magnitude equal to the inverse of root two. After a few pages of annoying algebra, it can be shown that

$$x_b \triangleq \frac{\omega_b}{\omega_n} = \sqrt{\left(1 - 2\zeta^2\right) + \sqrt{1 + \left(1 - 2\zeta^2\right)^2}} \quad , \tag{1-67}$$

where ω_b symbolizes the radial *3-dB* bandwidth. Obviously, ω_b is directly proportional to the self-resonant frequency, ω_n. Indeed, $\omega_b \equiv \omega_n$ when the damping factor is $\zeta = 1/\sqrt{2}$. But the damping factor also impacts the achievable *3-dB* bandwidth in the form that is depicted graphically in Figure (1.38).

The last plot motivates a few useful observations and related considerations. First, note that the bandwidth falls dramatically in the damping range, $0 < \zeta < 1$. For example, at $\zeta = 1/\sqrt{2}$, the normalized bandwidth, x_b, is one, while at $\zeta = 1$, $x_b = 0.64$, which suggests a significant *36%* bandwidth degradation with respect to the bandwidth evidenced under maximally flat operating conditions. For $\zeta > 1$, the bandwidth falls monotonically with damping factor, degrading to slightly more than *20%* of the MFM bandwidth at $\zeta = 2.5$. The lesson to be learned here is that while large ζ is comforting in the sense of achieving network stability, the price paid for unconditional stability is reduced network bandwidth; that is a progressive inability of the subject network to process faithfully high frequency signals. This observation justifies the common design objective of ensuring a damping factor that nominally satisfies the inequality,

$1/\sqrt{2} < \zeta < 1$. A damping factor significantly smaller than $1/\sqrt{2}$ risks unacceptable response peaking, which hints at potential system stability problems, while a damping factor that is significantly larger than unity results in unacceptable bandwidth degradation.

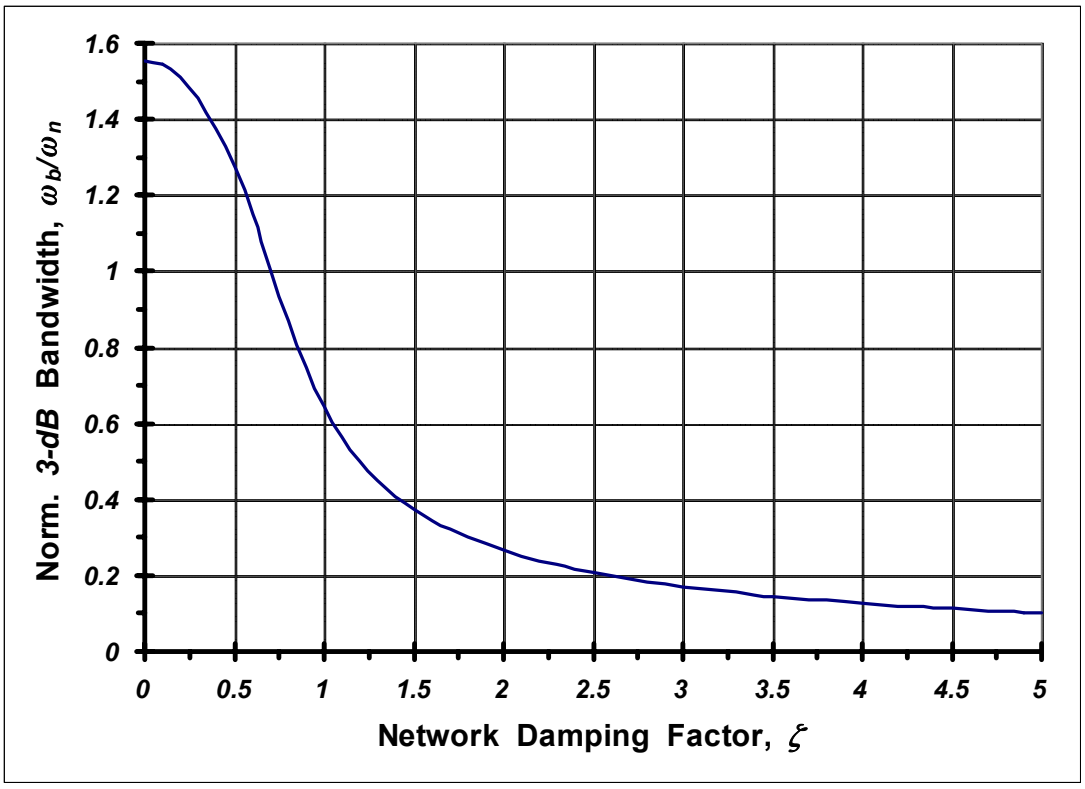


Figure (1.38). The Dependence Of Network *3-dB* Bandwidth On The Damping Factor.

Second, the case of a damping factor sufficiently larger than unity gives rise to a useful bandwidth approximation. With $\zeta > 1$, $(1 - 2\zeta^2)$ in (1-67) is a negative number. Accordingly, (1-67) can be recast as

$$\left(\frac{\omega_b}{\omega_n}\right)^2 = -\left(2\zeta^2 - 1\right) + \sqrt{1 + \left(2\zeta^2 - 1\right)^2}$$

$$= -\left(2\zeta^2 - 1\right) + \left(2\zeta^2 - 1\right)\sqrt{1 + \frac{1}{\left(2\zeta^2 - 1\right)^2}}\ .$$

For $(2\zeta^2 - 1)^2 >> 1$, the radical on the right hand side of this relationship can be approximated by a two-term power series, with the result that

$$\left(\frac{\omega_b}{\omega_n}\right)^2 \approx -\left(2\zeta^2 - 1\right) + \left(2\zeta^2 - 1\right)\left[1 + \frac{1}{2\left(2\zeta^2 - 1\right)^2}\right],$$

and for $2\zeta^2 >> 1$,

$$\left(\frac{\omega_b}{\omega_n}\right)^2 \approx \frac{1}{4\zeta^2}\ .$$

It follows that for sufficiently large ζ, the radial *3-dB* bandwidth can be approximated by the simple relationship,

$$\omega_b \approx \frac{\omega_n}{2\zeta} . \tag{1-68}$$

A numerical comparison of (1-68) with (1-67) readily demonstrates that (1-68) incurs a bandwidth error of less than *10.9%* for all $\zeta \geq 1.5$. Moreover, this error is always negative; that is, the approximated bandwidth is always smaller than the true *3-dB* bandwidth. In integrated circuit design situations that are routinely plagued by a plethora of uncertainties surrounding the modeling of active devices, energy storage elements engendered by the physical layout of the circuit, and nonzero component tolerances, it is comforting to be afforded the opportunity of using a simple bandwidth expression that is guaranteed to yield slightly pessimistic bandwidth results. Computational simplicity aside, it is especially interesting to note that the bandwidth approximation in (1-68) is exactly the inverse of the *s-term* coefficient in the denominator of the second order transfer function delineated in (1-55). In other words,

$$H(s)\Big|_{\zeta \geq 1.5} \approx \frac{H(0)}{1 + \frac{s}{\omega_b} + \frac{s^2}{\omega_n^2}} , \tag{1-69}$$

which suggests an approximate bandwidth evaluation deriving merely through discovery of the coefficient of the linear frequency term in the characteristic polynomial of the network transfer function.

1.4.2.3. Phase and Delay Responses

If the sinusoid,

$$v_s(t) = V_{sp} \cos \omega t , \tag{1-70}$$

is applied to a second order network whose transfer function is given by (1-55), the resultant steady state response is of the form,

$$v_o(t) = |H(0)| V_{sp} \cos\left[\omega t + \theta(\omega)\right] . \tag{1-71}$$

For a linear system, the frequency, ω, of the steady state output response is identical to the frequency of the applied, single frequency excitation. Equation (1-71) reaffirms the anticipated result that the amplitude of the steady state response is the amplitude, V_{sp}, of the input signal excitation, amplified (or multiplied) by the magnitude of the zero frequency gain, $|H(0)|$, of the network transfer function. Additionally, the steady state response is phase displaced by an amount, $\theta(\omega)$. Thus, for example, if $\theta(\omega) = -\pi/3$ *radians*, the output voltage is said to lag the input signal by *60°*. The visible impact of this example phase angle is shown in Figure (1.39), which plots, -versus- the normalized time, $\omega t/\pi$, the input signal of (1-70) and the output response of (1-71) for the case of a gain magnitude of $|H(0)| = 3$.

In general, the phase shift, $\theta(\omega)$, between the steady state input and output responses is a function of the input signal frequency. This generality is tacitly disturbing because, as is suggested by the plots in Figure (1.39), the phase shift of a linear network is indicative of steady state delay incurred in the signal processing between applied input and the resultant output

response. It just takes a bit of time for all those electrons to navigate the interconnected electrical and electronic maze that comprises the signal flow path between input and output network ports. If the phase shift, and hence the signal delay, is dependent on frequency, it is conceivable that the processed low frequency components of a non-sinusoidal input signal waveform do not arrive at the output port at the same times that do the high frequency components of said waveform. This disparity comprises ***phase distortion***, which can be acutely troublesome in certain applications. For example, if one is sitting in the front row of a concert hall listening to a live rock concert, one hears the bass guitar (low frequencies) accompanying a singing voice (higher frequencies) at nominally the same time that the voice is heard. But in a CD recording of the same interlude, a pronounced frequency dependence of the phase angle indigenous to the utilized stereo equipment can result in the speakers receiving the bass guitar input at a time that is appreciably delayed with respect to the voice response. In low cost stereo systems, this effect is typified by the "hollow" or "tunnel" sound, which is the bane of audiophiles.

Ideally, the foregoing delay issue can be mitigated by a phase angle that depends linearly on signal frequency. To wit, if $\theta(\omega)$ in (1-71) is given by

$$\theta(\omega) = -T_d\omega \ , \tag{1-72}$$

where T_d is a constant, independent of frequency, the steady state sinusoidal output response in (1-71) becomes

$$v_o(t) = |H(0)|V_{sp}\cos\left[\omega\left(t - T_d\right)\right]. \tag{1-73}$$

The last result is interesting in that it projects the impact of linear phase as a constant time delay in the amount of the proportionality constant, T_d, in (1-72). This is to say, that although the input signal is not processed instantaneously by the linear network, all input signal frequency components arrive in the steady state at precisely the times dictated by the applied input excitation. Referring to the preceding hypothetical rock concert, a stereo system boasting a linear phase response means that Keith Richard's guitar superimposed with Mick Jagger's voice would be heard through the speaker at the same times that they would be heard in a live concert setting.

Unfortunately, no physically realizable network can produce a linear phase response over frequency. But linear phase can be emulated over restricted frequency passbands. To this end, the ***envelope delay***, $D(\omega)$, of a linear network or system is introduced in accordance with the definition,

$$D(\omega) = -\frac{d\theta(\omega)}{d\omega} \ . \tag{1-74}$$

Note that if $\theta(\omega)$ is the linear frequency relationship of (1-72), $D(\omega)$ is the constant delay, T_d, discussed in conjunction with (1-73). For any other phase function, the passband over which $D(\omega)$ is a reasonable approximation of a constant defines the signal frequency range over which nominally constant I/O delay is evidenced in the steady state.

For the second order network whose normalized, frequency domain transfer function is the expression in (1-62), the phase response, in terms of the normalized frequency variable, x, in (1-61) is

$$\theta(x) = -\tan^{-1}\left(\frac{2\zeta x}{1-x^2}\right) \ . \tag{1-75}$$

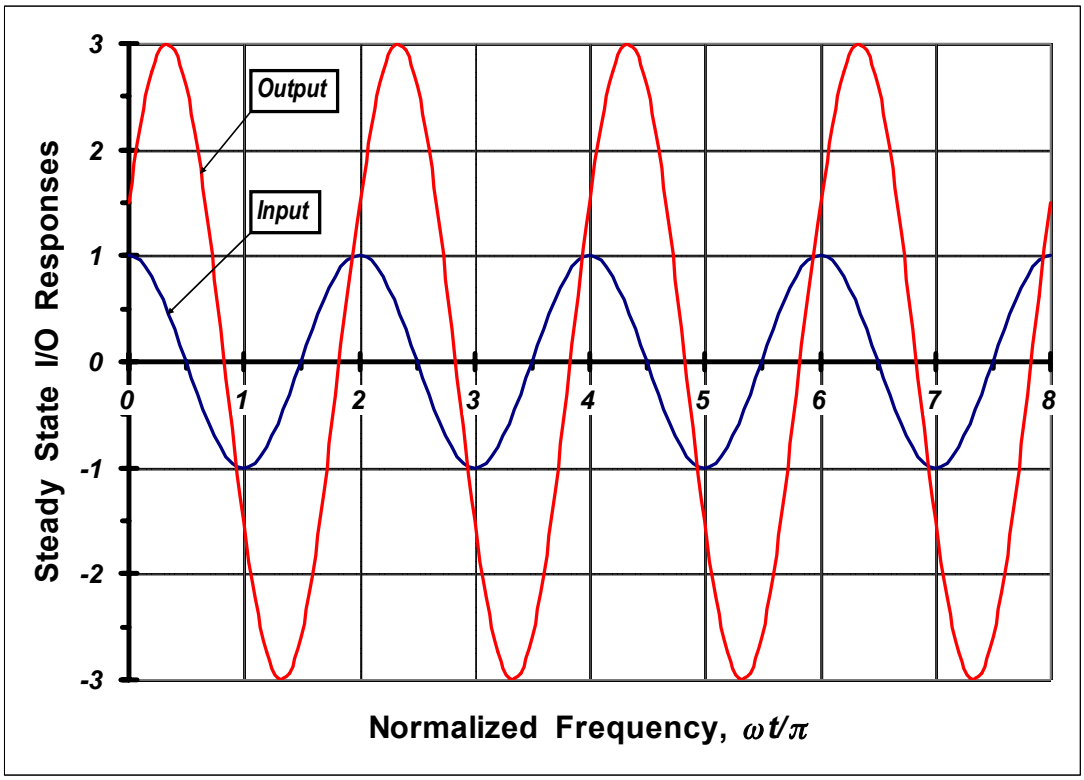


Figure (1.39). Steady State Input And Output Waveforms For Linear Second Order Network Having A Zero Frequency Gain Magnitude Of *3*. The Applied Input Excitation Is A Single Frequency Sinusoid. At This Frequency, The Phase Angle Attributed To The Linear Network Is *–60°*.

Recalling (1-74) and (1-61), the envelope delay, $D(x)$, as a function of x, is

$$D(x) = -\frac{d\theta(x)}{\omega_n\, dx},$$

whence a normalized envelope delay, $D_n(x)$, of

$$D_n(x) \triangleq \omega_n D(x) = -\frac{d\theta(x)}{dx}. \tag{1-76}$$

It follows that (1-75) and (1-76) combine to produce

$$D_n(x) = \frac{2\zeta\left(1 + x^2\right)}{1 + 2\left(2\zeta^2 - 1\right)x^2 + x^4} \tag{1-77}$$

as the normalized envelope delay of the second order network undergoing investigation. Figure (1.40) depicts (1-77) graphically in normalized format.

Several features of (1-77) warrant attention. First, observe a zero frequency normalized envelope delay of $D_n(0) = 2\zeta$ and hence, a zero frequency envelope delay of $D(0) = 2\zeta/\omega_n$. This delay is actually observable at not only zero frequency, but also at all low signal frequencies that conform to $x << 1$. Recall that $2\zeta/\omega_n$ is exactly the *s-term* coefficient in the denominator of the network transfer characteristic in (1-55). Moreover, and to the extent that the damping factor is at least as large as *1.5*, $2\zeta/\omega_n$ approximates the inverse *3-dB* bandwidth of the subject second

order system. Thus, the low frequency delay of a second order system is precisely the *s-term* coefficient in the network characteristic polynomial, and for $\zeta \geq 1.5$, this envelope delay is nominally the inverse of the *3-dB* bandwidth, ω_b.

The foregoing observations are rendered transparent by (1-75). In particular, for small x, the argument of the arctangent function is small. Since the arctangent of a small numerical argument is approximately the argument itself,

$$\theta(x)\big|_{x<<1} = -\tan^{-1}\left(\frac{2\zeta x}{1-x^2}\right)\Bigg|_{x<<1} \approx -2\zeta x \ . \tag{1-78}$$

It follows that

$$D_n(x)\big|_{x<<1} \approx -2\zeta \ , \tag{1-79}$$

as hypothesized in the preceding paragraph.

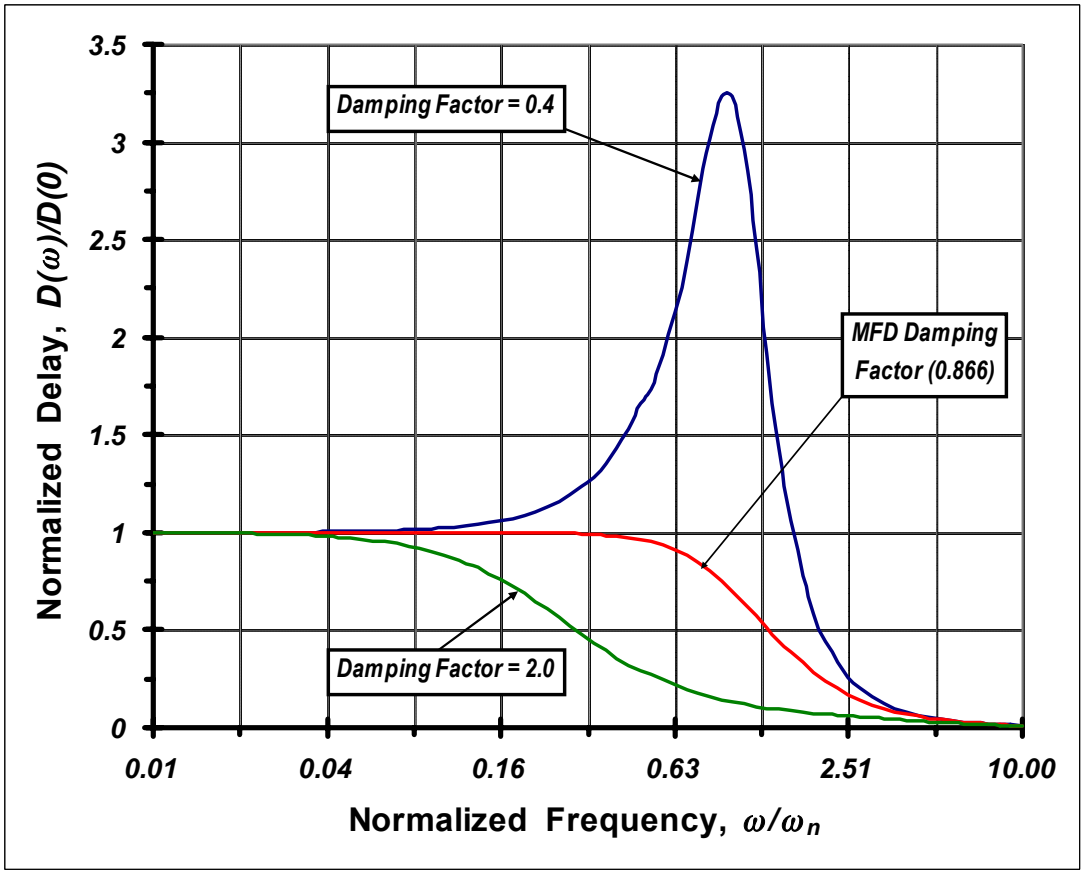


Figure (1.40). The Frequency Response Of The Envelope Delay For A Second Order Network For Various Values Of The Damping Factor, ζ. Note That The Maximally Flat Delay (MFD) Condition Yields A Flat Delay Response Over A Reasonably Wide Range Of Signal Frequencies. For A Damping Factor That Is Larger Than That Of The MFD Value, Flat Delay Also Results, But Over A More Restricted Frequency Interval.

A second observation is the fact that the envelope delay approaches zero at infinitely large frequencies. Thus, low frequency input signal components are delayed more than are high frequency components. Unfortunately, the envelope delay does not necessarily decay monotonically with increasing frequency, principally because the factor, $(2\zeta^2 - 1)$, in the denominator on

the right hand side of (1-77) can be a negative number. Since nominally constant delay is a desirable performance metric, it is of interest to determine the operating condition that ensures a monotonically decreasing delay response. This constraint, which defines the so-called ***maximally flat delay (MFD)*** condition, is determined by ensuring that the first derivative, with respect to x, of the normalized delay function, $D_n(x)$, is zero at no real normalized frequency other than zero. Upon execution of this analytical task, the MFD condition is found to be $\zeta = \sqrt{3}/2$. Smaller damping factors incur non-monotonicity, and hence peaking, in the delay response, while larger damping factors ensure a monotonic decreasing delay with signal frequency at the expense of a reduced frequency passband over which nominally constant delay is projected.

EXAMPLE #1.5:

Assume that the voltage transfer function of a preamplifier of one channel of a stereo system is the second order relationship given by (1-55). This preamplifier is to be designed for a maximally flat delay response that delivers constant delay to within *5%* for signal frequencies extending to the upper limit of the audio spectrum; namely *20 KHz*. Determine the minimum *3-dB* bandwidth that the preamplifier must deliver, as well as its self-resonant frequency. What is the low frequency delay of the designed amplifier?

SOLUTION #1.5:

(1). Maximally flat delay (MFD) in a second order circuit requires a damping factor, ζ, of

$$\zeta = \frac{\sqrt{3}}{2}. \qquad \text{(E5-1)}$$

An examination of the numerical computations precipitating the plots in Figure (1.40) reveals that the resultant envelope delay remains within *5%* of its zero, or low, frequency value through a normalized signal frequency that satisfies the inequality,

$$\frac{\omega}{\omega_n} = \frac{f}{f_n} < 0.5. \qquad \text{(E5-2)}$$

If (E5-2) is to be satisfied for a frequency as large as $f = 20\ KHz$, it is clear that the required self-resonant frequency of the preamplifier must satisfy

$$\boxed{f_n \geq \frac{f}{0.5} = \frac{20\ KHz}{0.5} = 40\ KHz.}$$

(2). For a damping factor chosen in accordance with (E5-1), (1-67) stipulates the *3-dB* bandwidth as

$$\frac{f_b}{f_n} = 0.786, \qquad \text{(E5-3)}$$

whence a bandwidth requirement of

$$\boxed{f_b \geq 0.786(40\ KHz) = 31.5\ KHz.}$$

(3). From (1-76) and (1-77), the zero, and approximate low frequency, envelope delay, $D(0)$, evaluates as

$$\boxed{D(0) = \frac{2\zeta}{\omega_n} = \frac{\zeta}{\pi f_n} = 6.89\ \mu SEC.}$$

COMMENTS: It is interesting that a maximally flat delay response in an audio amplifier requires a bandwidth that exceeds the *20 KHz* upper frequency limit of the audio spectrum.

1.4.3. POLES AND SECOND ORDER SYSTEM PARAMETERS

The preceding subsections of material underscore the significance of the damping factor, ζ, the quality factor, Q, and the radial undamped natural frequency, ω_n, as metrics that define the steady state frequency, phase, and delay responses of second order networks. It is often illuminating to cast these system parameters in terms of the network pole positions in the complex frequency plane. The most straightforward way of implementing this alternative characterization strategy is to relate the pole frequencies directly to the damping factor and self-resonant frequency.

The second order nature of the transfer function in (1-55) suggests the existence of two ***critical frequencies***, or ***poles***, say p_1 and p_2, such that

$$H(s) = \frac{H(0)}{1 + \frac{2\zeta s}{\omega_n} + \frac{s^2}{\omega_n^2}} = \frac{H(0)}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)} . \tag{1-80}$$

From a purely algebraic perspective, the poles define little more than the roots of the network characteristic polynomial, or denominator, of the transfer function. In particular, the roots herewith lie at $s = -p_1$ and at $s = -p_2$. On the presumption that p_1 and p_2 are real numbers, a necessary condition for network stability is that <u>both</u> p_1 and p_2 be positive. This requirement ensures that the two pole frequencies are negative and that the subject poles resultantly lie in the left half complex frequency plane. If p_1 and p_2 are complex numbers, physical realizability with lumped passive and active circuit elements demands that the two poles be complex conjugates. Additionally, network stability in the case of complex conjugate poles, like the stability constraint associated with real poles, mandates that complex poles also lie in the left half s-plane.

If the denominator on the far right hand side of (1-80) is expanded, $H(s)$ is expressible as

$$H(s) = \frac{H(0)}{1 + \frac{2\zeta s}{\omega_n} + \frac{s^2}{\omega_n^2}} = \frac{H(0)}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)} = \frac{H(0)}{1 + \left(\frac{1}{p_1} + \frac{1}{p_2}\right)s + \frac{s^2}{p_1 p_2}} . \tag{1-81}$$

A simple comparison of like coefficients in the Laplace variable, s, produces

$$\omega_n = \sqrt{p_1 p_2} \tag{1-82}$$

and

$$\frac{2\zeta}{\omega_n} = \frac{1}{p_1} + \frac{1}{p_2} ,$$

whence

$$\zeta = \frac{1}{2}\left(\sqrt{\frac{p_2}{p_1}} + \sqrt{\frac{p_1}{p_2}}\right) . \tag{1-83}$$

Observe that the undamped natural frequency of oscillation is exposed herewith as little more than the geometric mean of the two pole frequencies of a second order network. Moreover, the damping factor of the network is intimately related to the ratio of pole frequencies. Since negative damping factor ζ in (1-81) guarantees at least one right half plane pole (a characteristic polynomial having at least one root with a positive real part), a necessary condition for network stability is that the real solution of (1-83) must be a positive number.

Three special cases are of interest. The first of these is the ***underdamped*** case, wherein p_1 and p_2 are complex conjugate poles. From (1-82), underdamping necessarily implies that the pole frequencies satisfy

$$\left.\begin{aligned} p_1 &= \omega_n e^{j\varphi} = \omega_n \cos\varphi + j\omega_n \sin\varphi \\ p_2 &= \omega_n e^{-j\varphi} = \omega_n \cos\varphi - j\omega_n \sin\varphi \end{aligned}\right\} , \tag{1-84}$$

where angle φ must be larger than (and not equal to) $\pi/2$ *radians* and smaller than (but not equal to) $3\pi/2$ *radians* to guarantee network stability. Note that ω_n is observed to be the magnitude of either pole frequency. If (1-84) is substituted into (1-83), the damping factor for the underdamped network condition is found to be smaller than one, since

$$\zeta = \frac{1}{2}\left(e^{-j\varphi} + e^{j\varphi}\right) = -\cos\varphi , \tag{1-85}$$

and $\pi/2 < \varphi < 3\pi/2$. Thus, both the MFM and the MFD cases considered earlier correspond to underdamped operating conditions. In particular, MFM requires $\zeta = 1/\sqrt{2}$, which corresponds to a pole angle, φ, of $3\pi/4$ *radians*. On the other hand, MFD stipulates $\zeta = \sqrt{3}/2$, or $\varphi = 5\pi/6$ *radians*. Observe that the pole angle difference between MFM and MFD responses is a mere $\pi/12$ *radians*, or $15°$.

A special case of underdamping is an angle, φ, of $\pi/2$ *radians*, for which $\zeta = 0$ in (1-83). From (1-84), the poles corresponding to this zero damping case lie exclusively on the $j\omega$-axis of the complex frequency plane since $p_1 = +j\omega_n$ and $p_2 = -j\omega_n$; that is, the pole frequencies have null real parts. As is demonstrated subsequently, a network having zero damping responds to an impulsive input with a free running sinusoidal oscillation. This is to say that the output response is an eternal sinusoid even though the input excitation reduces ultimately to zero. Such an operating condition is certainly undesirable in linear amplification networks. For example, it would be annoying to hear a single frequency tone at the speakers of a stereo system as a background to the music recorded on a CD. However, zero damping is an essential design constraint of sinusoidal oscillators, which are exploited extensively in radios, television receivers, and numerous other communication media.

A second special interest is the ***overdamped*** case, for which the network poles are real numbers. If poles p_1 and p_2 are real, such that $p_2/p_1 = k$, a positive number, the damping factor in (1-83) becomes

$$\zeta = \frac{1}{2}\left(\sqrt{k} + \frac{1}{\sqrt{k}}\right), \tag{1-86}$$

which can be demonstrated to yield $\zeta > 1$ for all positive values of k. For $k >> 1$, the pole at frequency p_1 is said to be ***dominant***, for the frequency, p_1, effectively determines the *3-dB* bandwidth of the overdamped system. To demonstrate this contention, observe in (1-86) that

$$\zeta|_{k>>1} \approx \frac{\sqrt{k}}{2}. \tag{1-87}$$

From (1-87) and (1-68), the resultant *3-dB* bandwidth computes as

$$\omega_b|_{k>>1} \approx \frac{\omega_n}{2\zeta} \approx p_1. \tag{1-88}$$

While p_1 is said to be the dominant pole of an overdamped system having

$$p_2 = k p_1 \tag{1-89}$$

and $k >> 1$, p_2 is commonly termed the ***non-dominant network pole***. The implication of this jargon is that since the *3-dB* bandwidth is almost entirely determined by p_1, the dominant pole, p_2 is relatively unimportant or "non-dominant."

The third special case is critical damping, for which p_1 and p_2 are real, positive, identical numbers. With $p_2 \equiv p_1$, k in (1-89) is one, whence a damping factor, from (1-86), of unity. Moreover, the undamped natural frequency, from (1-82), is now $\omega_n \equiv p_1$. Although a critically damped circuit is a stable structure, it is nonetheless undesirable for at least two reasons. The first of these reasons, which is explored later, is the fact that certain commonly encountered feedback signal paths around a critically damped circuit can incur unstable responses to bounded input excitations. The second reason is a deterioration of *3-dB* bandwidth, which is the bane of design engineers tasked to realize broadbanded frequency responses. To wit, $\zeta = 1$ in (1-67) results in a *3-dB* bandwidth, ω_b, of $\omega_b = 0.644\omega_n = 0.644p_1$, which is an almost *36%* reduction from the bandwidth indigenous to a dominant pole response.

1.4.4. TIME DOMAIN TRANSIENT RESPONSES

The frequency, phase, and delay responses of linear networks are steady state performance indices that quantify such commonly invoked metrics as I/O gain at zero or any other frequency, *3-dB* bandwidth, and envelope delay at zero or another frequency of interest. Because these steady state performance barometers are relatively easy to deduce both analytically and experimentally, there is an industry-wide tendency to forego more intricate time domain characterizations of electronic networks. Unfortunately, a steady state performance characterization in the absence of companion transient response investigations documents an incomplete picture of network functionality and utility. Such a characterization is akin to walking into a theater at the concluding moments of a film; the viewer sees the ending scene without comprehending the vagaries of a compelling plot that leads to the concluding scene.

The steady state response is the output voltage or current produced after a sufficiently long time has elapsed subsequent to the time at which the input signal excitation is applied. It is literally the "concluding scene" of the circuit response. A circuit assessment limited to only the steady state fails to establish the length of time required by the circuit to achieve the steady state.

It also fails to reveal the time domain nature of the ***transient response***, which is a picture of the electrical response waveforms that prevail between the instant of time at which the input is applied and the time at which nominal steady state behavior is produced. These waveforms may be very slowly varying functions of time that imply an inordinately long time for the realization of steady state outputs. Or, the waveforms may significantly overshoot or undershoot the steady state response before actual steady state is achieved, thereby leading to unacceptable, potentially unstable, or even damaging electrical transients.

The impulse response and the step response are two commonly invoked tools for assessing the transient behavior of linear networks. In the subsections that follow, the impulse response of a second order oscillatory network is derived and scrutinized, as are the step responses to more general overdamped, critically damped, and underdamped second order circuits.

1.4.4.1. Impulse Response

The oscillatory nature of an undamped lowpass system can be established directly in the time domain through an investigation of the ***impulse response*** of the subject system. As is symbolically illustrated in Figure (1.41), the impulse response, say *h(t)*, of a linear network having an I/O transfer function of *H(s)* is the time domain output generated as a result of an applied impulse input, say *δ(t)*. An impulsive source in the time domain is a pulse of infinitely large amplitude and zero time duration enclosing precisely unity area. This area is related to the energy said waveform delivers to the network port it drives. Idealized impulsive inputs are physically unrealizable, but mathematically, they forge a useful model for assessing the manner in which a linear system responds to abrupt excitation whose time duration is very short. For example, the laser tracking system within a compact disc player may encounter a speck of dust or a scratch on the disc media. This environmental parasitic causes a momentary undesirable input signal for which the system response hopefully abates quickly and inconsequentially. Communication systems also suffer from impulsive-like inputs when, for example, a fraction of the energy released by local lightening electromagnetically couples to the system antenna. In short, impulse responses are an ideal, but mathematically effective, way of gauging the impact exerted on a linear system by undesirably large and abrupt input energies.

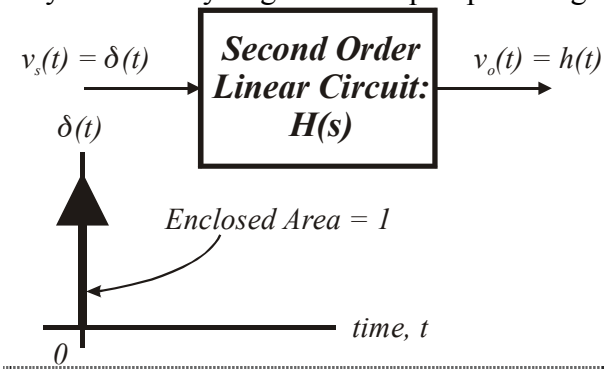


Figure (1.41). An Abstraction Of A Second Order Circuit Excited At Its Input Port By A Unit Impulse Of Energy.

For the undamped second order situation implied by $\zeta = 0$, the transfer function in (1-55) collapses to

$$H(s)\big|_{\zeta=0} = \frac{V_o(s)}{V_s(s)} = \frac{H(0)}{1 + \dfrac{s^2}{\omega_n^2}}, \tag{1-90}$$

whose poles lie on the $j\omega$–axis at $s = \pm j\omega_n$. Since the Laplace transform of a unit impulse function is unity, the transform of the unit impulse response is simply the applicable transfer function. Accordingly the undamped time domain impulse response, say $h_o(t)$, is the inverse transform of the function appearing on the right hand side of (1-90). In particular,

$$v_o(t) \triangleq h_o(t) = H(0)\omega_n \sin\left(\omega_n t\right); \tag{1-91}$$

that is, the impulse response of interest is a bounded sinusoid whose radial frequency is the undamped natural frequency, ω_n, of the considered system. The curiosity here is that for time $t > 0$, the input energy, as is depicted in Figure (1.41), is zero. Accordingly, the steady state gain, which is the amplitude, $H(0)\omega_n$, of the output sinusoid at frequency ω_n, divided by the input signal (which is zero for all nonzero time) is infinitely large. This deduction is confirmed by (1-90), which verifies infinite gain in the steady state at frequency ω_n, where s can be equated to $j\omega_n$. If frequency ω_n lies within the audio spectrum, for example, a stereo amplifier regrettably characterized by zero damping under certain operating conditions produces a piercing whistling tone in its speakers in response to a single, sharp beat of a drum in a musical passage recorded on a compact disc. More generally, the determination of the steady state response of an undamped linear network to any type of input is a pointless undertaking. The reason underlying this contention is that in the immediate neighborhood of the instant of time at which input signal is applied, said input emulates an impulse that produces a sinusoidal background response whose amplitude is not proportional to the steady state input signal amplitude. In a word, the network ceases to emulate input -to- output linearity.

Two other points surrounding (1-91) are noteworthy. The first of these points, and the one easiest to understand, is the explanation of why parameter ω_n is commonly referred to as the "undamped natural frequency of oscillation" for a second order system. In particular, note that zero damping not only gives rise to a sinusoidal impulse response, it produces an output sinusoid whose radial frequency is exactly ω_n. As such, ω_n is a natural resonant frequency evidenced only when zero damping (hence, "undamped") prevails in the system undergoing study.

The second point is more abstract but nonetheless important conceptually. In particular, the impulse response in (1-91) is an eternal sinusoid or equivalently, a sinusoid whose amplitude never diminishes. This eternal oscillation prevails despite the fact that the input giving rise to this response is zero for all times immediately subsequent to the application of said input. In other words, the output immediately after input application requires no input. Moreover, ostensibly nothing within the network serves to diminish the energy implicit to the sinusoidal response, which means that the subject network behaves as an ideal lossless entity. It follows that the damping factor, ζ, in an electrical or electronic circuit is a measure of the losses incurred by the resistances embedded within the I/O signal flow path of the circuit. Zero damping corresponds to zero energy losses and thus, no effective resistances in the signal flow path. Conversely, damping factors larger than zero imply a progressively more lossy circuit.

In any practical circuit, losses are inevitable. Thus, eternal oscillations cannot be sustained in a simple inductor-capacitor tank circuit because practical inductors have parasitic series resistances and practical capacitors have unavoidable shunt resistances. Accordingly, circuits

expressly designed to behave as sinusoidal oscillators must exploit electronic amplifiers that utilize such devices as bipolar or metal-oxide-semiconductor (MOS) transistors. To be sure, these amplifiers supply gain when appropriately biased for nominally linear operation. But they can also establish requisite negative resistances that effectively cancel the net positive resistance implicit to I/O signal paths. As a result, they serve to constrain the effective network damping factor to zero, thereby conducing sinusoidal responses to virtually any form of input excitation (such as the turn on transient associated with switching in the batteries that bias the electronic circuits or the electrostatic noise coupled to network input ports by Aunt Milly's kitchen mixer). Once generated, the sinusoidal output response continues until the biasing power required to linearize embedded amplifying networks is removed or otherwise switched off. In short, sinusoidal input responses can never be generated in passive circuits, but they can be supported in active architectures that are configured to produce appropriate amounts of effective negative resistances.

1.4.4.2. Step Response

For practical, non-impulsive inputs that are applied suddenly to a linear network, the energy storage elements within said network (and implicit to the interconnected passive and active components embedded within the electrical network) prohibit an instantaneous realization of steady state output responses. As a result, the ***settling time*** of a circuit, which is the time (measured immediately after input energy application) required to reach and maintain steady state output behavior to within an acceptable error tolerance, bodes obvious design-oriented interest. It is futile to deduce settling times for all possible input voltage and current waveforms. To this end, the unit step has been adopted as the applicable standard test vehicle for settling time delineation. As is abstracted in Figure (1.42), the unit step of applied voltage or current changes instantaneously from zero value to unit value at an arbitrary time which, for convenience, can be taken as time $t = 0$. The step input arguably establishes a worst case measure of settling time since any "real" excitation, which cannot slew instantaneously at its time point of application, inherently provides the considered system with time to react. In other words, practical input waveforms offer the system a chance to track faithfully the applied excitation, thereby masking settling transients. Since the step input offers no such reaction opportunity at its point of application, an investigation of the step response and its associated settling time paints a picture of the inherent transient response limitations of the system undergoing study.

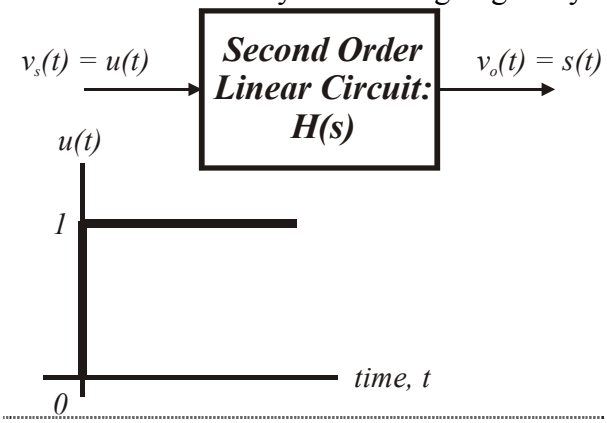


Figure (1.42). An Abstraction Of A Second Order Circuit Excited At Its Input Port By A Unit Step Of Energy.

In general, the Laplace transform of the step response for the linear second order network in Figure (1-42) is

$$V_o(s) = \mathscr{L}[s(t)] = \frac{H(0)}{s\left(1 + \frac{2\zeta s}{\omega_n} + \frac{s^2}{\omega_n^2}\right)} = \frac{H(0)}{s\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)}, \qquad (1\text{-}92)$$

where $\mathscr{L}[s(t)]$ denotes "Laplace transform of $s(t)$," (1-80) is recalled, and use is made of the fact that the Laplace transform of the unit step, $u(t)$, is $1/s$. Obviously, the time domain step response, $s(t)$, is little more than the inverse transform of either of the functional forms on the right hand side of (1-92). The consideration of three special cases expedites this inverse transformation task.

OVERDAMPED CASE

In an overdamped network, the damping factor, ζ, exceeds unity. Correspondingly, the pole frequencies, p_1 and p_2, are positive real numbers. If the pole ratio, k, in (1-89) is exploited, it can be demonstrated that the overdamped step response, say $s_o(t)$, normalized to the zero frequency gain, $H(0)$, is

$$\frac{s_o(t)}{H(0)} = 1 - \left(\frac{k}{k-1}\right)e^{-p_1 t} + \left(\frac{1}{k-1}\right)e^{-kp_1 t}, \quad t \geq 0+. \qquad (1\text{-}93)$$

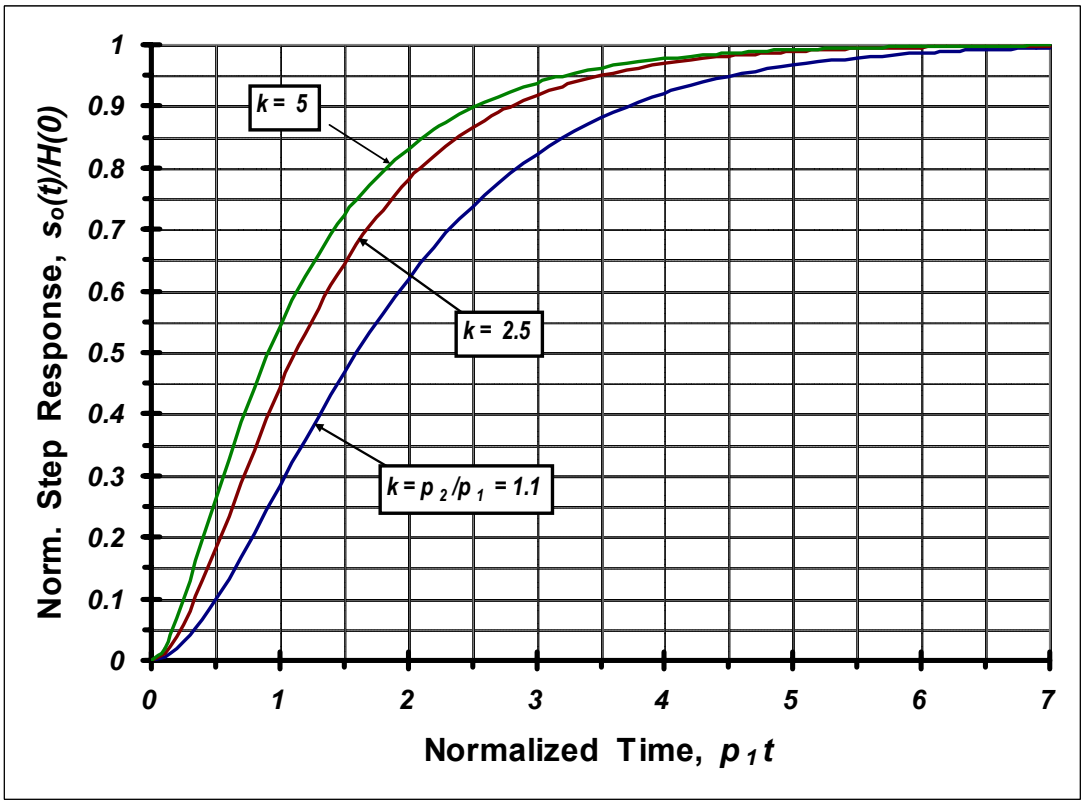


Figure (1.43). The Normalized Step Response Of An Overdamped, Linear, Second Order Network For Various Values Of The Pole Ratio, $k = p_2/p_1$.

Figure (1.43) displays this step response as a function of the normalized time, $p_1 t$, for various values of the pole ratio, k. The plot at hand clearly shows a monotonically rising response over time. Moreover, it shows that progressively larger values of k result in faster responses and hence, reduced settling times. If the settling time, say t_s, is formally defined to be the time required for the step response to rise to within *95%* of its normalized steady state value of one,

$$\frac{s_o(t_s)}{H(0)} = 1 - \left(\frac{k}{k-1}\right)e^{-p_1 t_s} + \left(\frac{1}{k-1}\right)e^{-kp_1 t_s} \triangleq 0.95 . \tag{1-94}$$

For generalized k, this relationship requires an iterative numerical solution. To wit, $p_1 t_s = 4.53$ for $k = 1.1$, $p_1 t_s = 3.50$ for $k = 2.5$, and $p_1 t_s = 3.22$ for $k = 5$. Thus, the *95%* settling time for $k = 5$ is about *41%* smaller than the settling time with $k = 1.1$. The fact that it is only about *8.7%* smaller than the $k = 2.5$ settling time suggests that a point of diminishing returns is reached as attempts are made to displace the less dominant pole to progressively higher frequencies.

For a network characterized by a dominant pole response, the pole at frequency $p_2 = kp_1$ is relatively inconsequential. The second term on the right hand side of (1-94) is resultantly negligible, thereby precipitating the approximate closed form solution,

$$p_1 t_s \approx 3 + \ln\left(\frac{k}{k-1}\right) \approx 3 . \tag{1-95}$$

Note that the settling time for very large k differs from that of $k = 5$ by only *7.3%*.

CRITICALLY DAMPED CASE

For critical damping, the damping factor, ζ, is unity, and the pole frequencies, p_1 and p_2, are positive, real, and identical numbers. The resultant step response, say $s_c(t)$, normalized to the zero frequency gain, $H(0)$, is

$$\frac{s_c(t)}{H(0)} = 1 - (1 + p_1 t)e^{-p_1 t}, \; t \geq 0+ . \tag{1-96}$$

Figure (1.44) plots this critically damped step response against the normalized time, $p_1 t$. An iterative numerical solution of (1-96) for the *95%* settling time yields

$$p_1 t_s \approx 4.75 , \tag{1-96}$$

which indicates a settling time that is better than *58%* larger than the settling time indigenous to a dominant pole network. The significance of this larger settling time can be underscored through consideration of a hypothetical circumstance in which a dominant pole network and a critically damped network are to produce identical *95%* settling times. In this situation, the frequencies of the two identical poles in the critically damped configuration must be *58%* larger than the frequency of the lone significant pole in the dominant pole system; that is, the critically damped network must be substantively broadbanded. As the reader ultimately learns, broadbanding a single pole, yet alone two poles, is rarely a trivial exercise, particularly since individual poles of a linear network are invariably dependent on the same, or parametrically related, circuit variables. Other reasons, such as stability issues that arise when global feedback is connected around a network, also discourage the exploitation of critical damping scenarios in electronic networks.

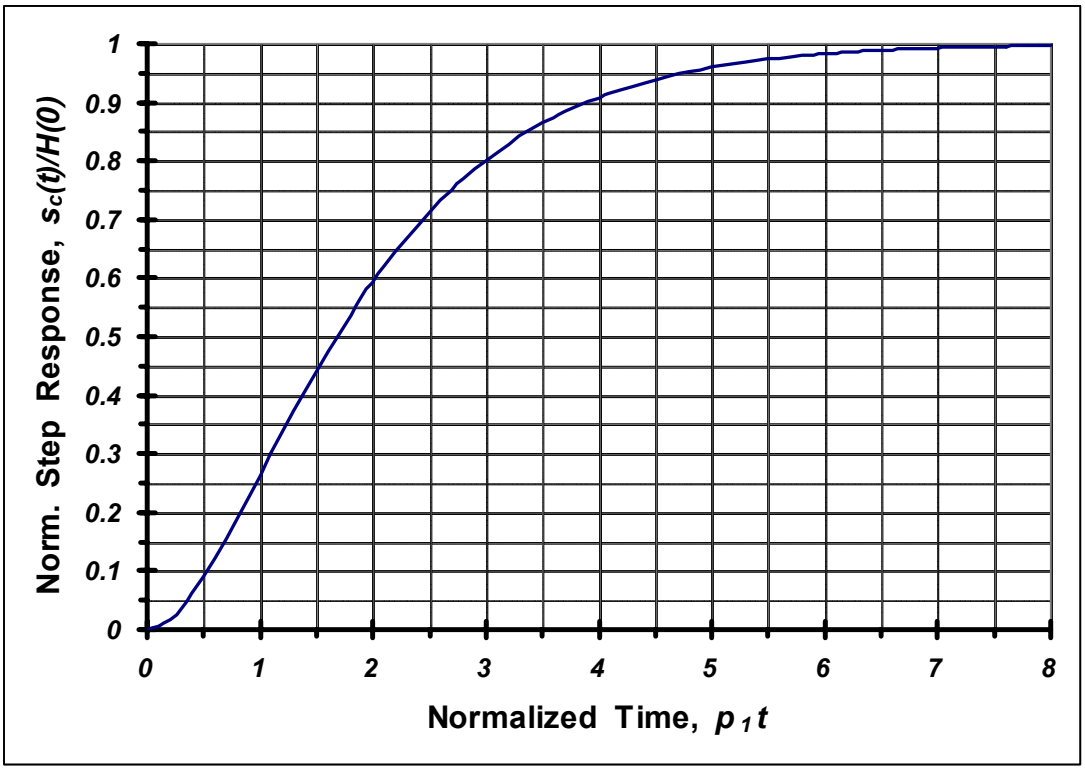


Figure (1.44). The Normalized Step Response Of A Critically Damped, Linear, Second Order Network Plotted As A Function Of The Normalized Time Variable, $p_1 t$.

UNDERDAMPED CASE

An underdamped network having a bounded output step response has $0 \le \zeta < 1$, which corresponds to complex conjugate poles having non-negative real parts. In this case, the step response, say $s_u(t)$, is the damped sinusoid,

$$\frac{s_u(t)}{H(0)} = 1 - \frac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}} \sin\left[\sqrt{1-\zeta^2}\,(\omega_n t) + \cos^{-1}(\zeta)\right],\ t \ge 0+ . \tag{1-97}$$

The time domain nature of this function is dramatized in Figure (1.45), which depicts step responses displaying potentially significant overshoot and undershoot of the steady state response value, depending on the value of the damping factor.

The non-monotonic nature of the underdamped step response complicates the task of delineating the settling time. Before attempting to discern the time required for the response to achieve and maintain *95%*, or any other percentage, of its steady state value, it is useful to note that the first term on the right hand side of (1-97) is indeed the normalized steady state output. Accordingly, the second term on the right hand side of the subject relationship can be viewed as an error response, $\varepsilon(t)$, such that

$$\frac{s_u(t)}{H(0)} = 1 + \varepsilon(t), \tag{1-98}$$

where

$$\varepsilon(t) = -\frac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}} sin\left[\sqrt{1-\zeta^2}\,(\omega_n t) + cos^{-1}(\zeta)\right] \tag{1-99}$$

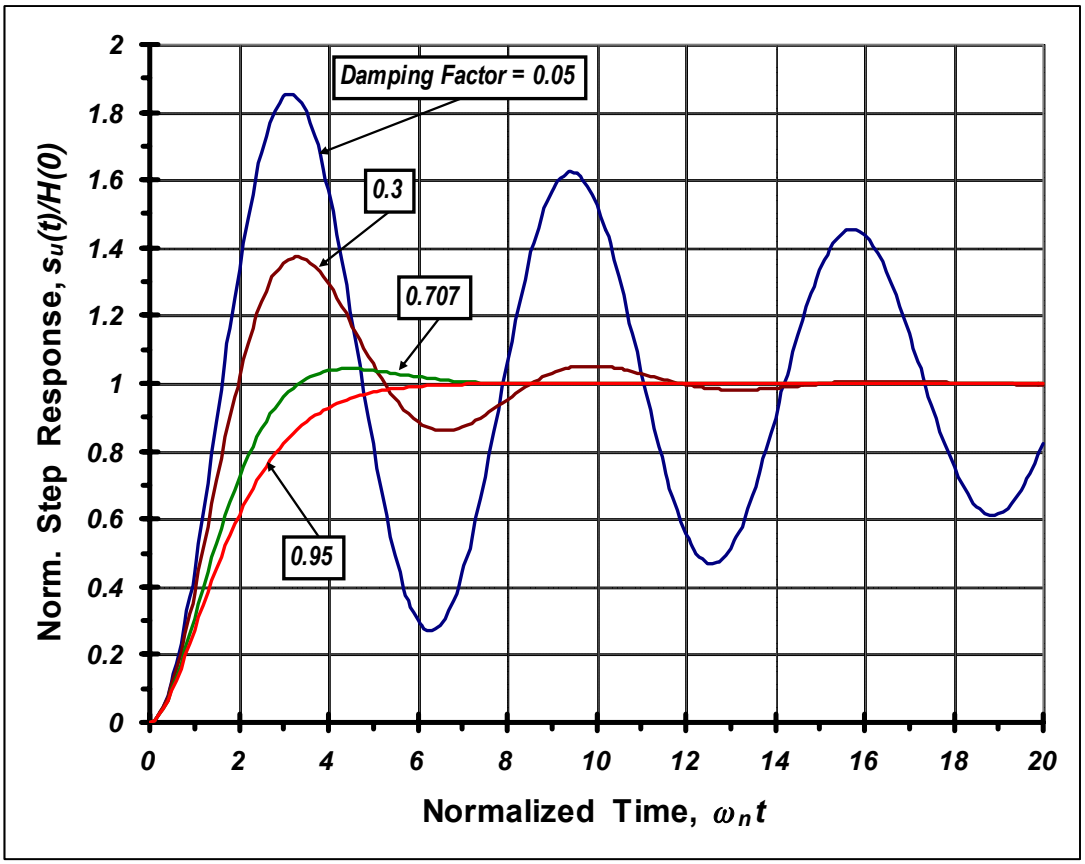


Figure (1.45). The Normalized Step Response Of An Underdamped, Linear, Second Order Network Plotted For Various Values Of The Damping Factor, ζ, As A Function Of The Normalized Time Variable, $\omega_n t$.

is plotted in Figure (1.46). Note that for $\zeta > 0$, the amplitude of this error function diminishes with increasing time. It follows that a plausible analytical strategy for determining the settling time is to set the time slope, $d\varepsilon(t)/dt$, to zero in order to determine the time, say t_m, corresponding to the first error maximum beyond zero time. Ensuring that the maximum, or peak, error corresponding to this time lies below an acceptable value assures acceptably small response errors at any other time. The conduct of these messy tasks results in

$$\omega_n t_m = \frac{\pi}{\sqrt{1-\zeta^2}}\,, \tag{1-100}$$

and

$$\varepsilon_m = e^{-\zeta\omega_n t_m} = exp\left(-\frac{\zeta\pi}{\sqrt{1-\zeta^2}}\right). \tag{1-101}$$

Figure (1.46) depicts $\omega_n t_m$ and ε_m for the case of a damping factor of $\zeta = 0.05$; in particular, $\omega_n t_m = 3.15$ and $\varepsilon_m = 0.85$. It follows that if ε_m is the tolerable maximum error associated with the

settling time, t_s, (1-101) sets the requisite damping factor, which establishes the normalized settling time, $\omega_n t_s$, in (1-100).

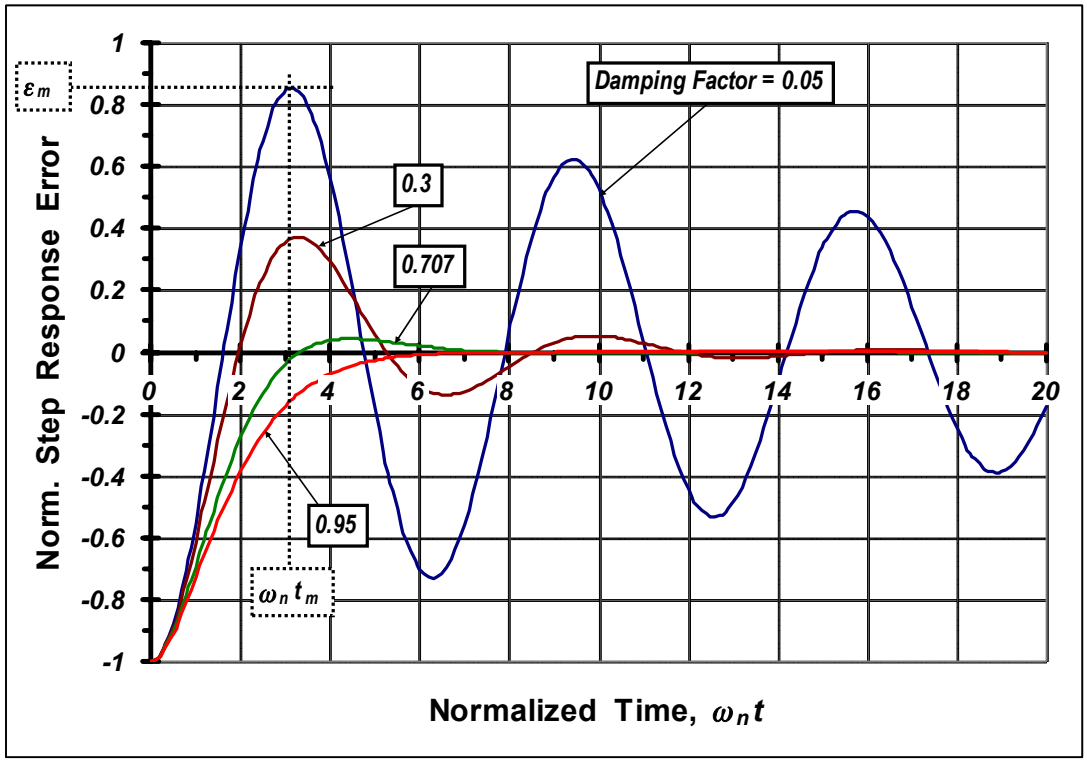


Figure (1.46). The Normalized Error Response, With Respect To The Steady State Output, Of An Underdamped, Linear, Second Order Network Plotted For Various Values Of The Damping Factor, ζ, As A Function Of The Normalized Time Variable, $\omega_n t$. The Peak Error, ε_m, And The Time, $\omega_n t_m$, Corresponding To This Peak Are Specifically Delineated For The Case Of A Damping Factor Of $\zeta = 0.05$.

EXAMPLE #1.6:

Assume that the voltage transfer function of a preamplifier of one channel of a stereo system is the second order relationship given by (1-55). This preamplifier is to be designed for *95%* step response settling at a time that does not exceed the period associated with the theoretic upper frequency limit of the audio spectrum. What is the required *3-dB* bandwidth of the amplifier?

SOLUTION #1.6:

(1). If settling to within *95%* of the steady state step response value is the required performance specification, εm in (1-101) must satisfy $\varepsilon_m \leq 0.05$. The corresponding damping requirement is therefore found to be $\zeta \geq 0.6901$.

(2). For a damping factor of 0.6901 (1-67) confirms a *3-dB* bandwidth of

$$\frac{f_b}{f_n} = 1.024 . \qquad \text{(E6-1)}$$

(3). The upper frequency limit of audio responses is *20KHz*. In accordance with the performance requirements of the amplifier at hand, the settling time must be no larger

than $t_s = 1/2\pi(20\ KHz) = 7.958\ \mu sec$. Using (1-100), the self- resonant frequency of the amplifier is

$$f_n = \frac{1}{2t_s\sqrt{1-\zeta^2}} \geq 86.82\ KHz\,. \qquad \text{(E6-2)}$$

(4). Combining the foregoing two results, the requisite *3-dB* bandwidth, f_b, must be at least as large as

$$\boxed{f_b = (1.024)(86.82\ KHz) = 88.9\ KHz\,.}$$

COMMENTS: Superior performance in at least the senses of very short settling time and stringent settling error demands high bandwidth. It should be noted that the damping requirement herewith is not consistent with either maximally flat magnitude or maximally flat delay responses in the steady state. This observation underscores the necessity of investigating both the transient and the steady state responses in any electronic circuit and system design scenario. It also highlights the perennial need for design compromises. In this particular case, and in the absence of any compensation invoked on the second order transfer characteristic, decisions are mandated to ascertain whether settling time, maximally flat frequency response, maximally flat delay response, or some other performance metric comprises the dominantly important design theme.

EXERCISES

PROBLEM #1.1

Under commonly encountered operating conditions, Figure (P1.1) is a valid linearized equivalent circuit of a voltage buffer realized in MOSFET device technology. The input signal source is represented by its Thévenin equivalent circuit, which consists of voltage source V_s and resistance R_s. The response to this input signal is the indicated voltage, V_o, which is developed across the shunt interconnection of load resistance R_l and load capacitance C_l. The actual MOS transistor is modeled by the two voltage controlled current sources, $g_m V_i$ and $\lambda_b g_m V_b$, where g_m (typically of the order of hundreds of micromhos to a few millimhos) is the forward transconductance of the transistor, and λ_b (a dimensionless number generally smaller than *0.1*) emulates the impact exerted by the substrate on device forward transfer characteristics. Note that regardless of the nature of the transistor parameters, the model in Figure (P1.1) is a linear active circuit, not unlike the circuits addressed in this chapter.

(a). Determine, and express as a function of V_s, the Thévenin equivalent voltage, say V_{ot}, that drives the load capacitor, C_l. Simplify the expression for V_{ot} for the special case of an infinitely large load resistance, R_l. If R_l were to be omitted from the diagram in Figure (P1.1), would the resultant expression for V_{ot} be identical to the originally derived expression?

(b). What is the low frequency value of the voltage gain, V_o/V_s, of the circuit and how does this gain relate to the ratio, V_{ot}/V_s?

(c). Derive an expression for the Thévenin equivalent resistance, R_{out}, facing capacitance C_l.

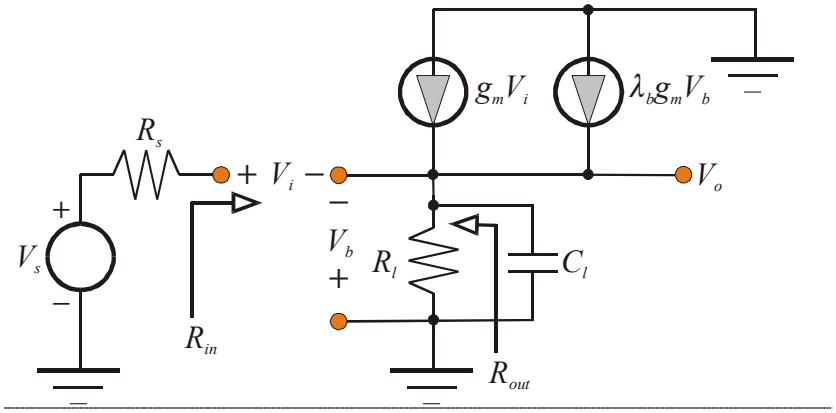


Figure (P1.1)

(d). Derive an expression for the low frequency input resistance, R_{in}, "seen" by the signal source.

(e). What is the significance of the time constant, $R_{out}C_l$, to the frequency domain transfer function, $H(j\omega) = V_o(j\omega)/V_s(j\omega)$? Give an expression for this transfer relationship in terms of V_{ot}/V_s and the subject time constant.

(f). Give a simple expression for the *3–dB* bandwidth of the circuit.

(g). Is there anything interesting about the gain bandwidth product, which is cleverly defined as the product of the magnitude of zero frequency gain and *3–dB* bandwidth?

(h). Take $R_s = 300\ \Omega$, $R_l = 1{,}000\ \Omega$, $g_m = 5$ *mmho*, $\lambda_b = 0.08$, and $C_l = 8$ *pF*. Calculate the low frequency voltage gain, the output resistance, the time constant of the circuit, and the circuit *3-dB* bandwidth.

PROBLEM #1.2

Under commonly encountered operating conditions, Figure (P1.2) is a valid linearized equivalent circuit of a voltage amplifier realized in bipolar junction transistor (BJT) device technology. The input signal source is represented by its Thévenin equivalent circuit, which consists of voltage source V_s and resistance R_s. The output, or response, to this input signal is the indicated voltage, V_o, which is developed across the shunt interconnection of load resistance R_l and load capacitance C_l. The actual BJT is modeled by the current controlled current source, βI, and the two resistances, r_b and r_π. Typically, β, which is dimensionless, is of the order of *100* or so, r_b can be as large as *200* Ω, and r_π is of the order of a few thousand ohms. The resistance, R_e, is a circuit element used for biasing and linearity purposes. It is generally chosen to be of the order of fifty to a few hundred ohms.

(a). Determine, and express as a function of V_s, the Thévenin equivalent voltage, say V_{ot}, that drives the load capacitor, C_l. Simplify the expression for V_{ot} for the special case of a very large current gain parameter, β.

(b). What is the low frequency value of the voltage gain, V_o/V_s, of the circuit and how does this gain relate to the ratio, V_{ot}/V_s?

(c). Derive an expression for the Thévenin equivalent resistance, R_{out}, facing capacitance C_l.

(d). Derive an expression for the low frequency input resistance, R_{in}, "seen" by the signal source.

(e). Derive an expression for the net effective resistance, say R_{te}, established across the terminals where resistance R_e is connected.

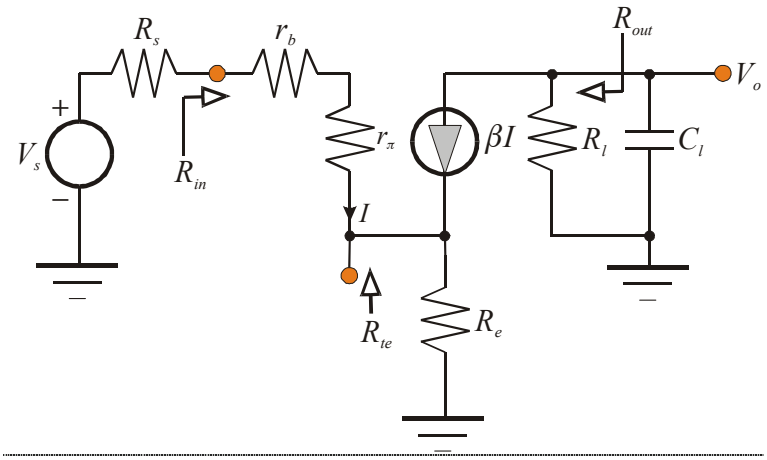


Figure (P1.2)

(f). What is the significance of the time constant, $R_{out}C_l$, to the frequency domain transfer function, $H(j\omega) = V_o(j\omega)/V_s(j\omega)$? Give an expression for this transfer relationship in terms of V_{ot}/V_s and the subject time constant.

(g). Give a simple expression for the *3–dB* bandwidth of the circuit.

(h). Take $R_s = 300\ \Omega$, $R_l = 1{,}000\ \Omega$, $\beta = 120$, $r_b = 190\ \Omega$, $r_\pi = 1.5\ K\Omega$, $R_e = 100\ \Omega$, and $C_l = 8\ pF$. Calculate the low frequency voltage gain, the output resistance, the time constant of the circuit, the circuit *3-dB* bandwidth, and the resistance parameter, R_{te}.

PROBLEM #1.3

Consider the simple *RLC* circuit in Figure (P1.3), which can be viewed as a simplified model of the high frequency parasitics that underlie an interconnect between two integrated circuits on a circuit board. Interconnect lines have unavoidable distributed resistance, inductance, and capacitance which serve to slow output responses to rapidly applied inputs. In extreme cases, these high frequency parasitics can incur undesirable oscillations or, depending on the electrical nature of the circuits they couple together, outright instability. You may unfortunately view this and the next problem as entailing significant mathematical "busy work," but the problems herewith are very practical and are commonly addressed by integrated circuit designers.

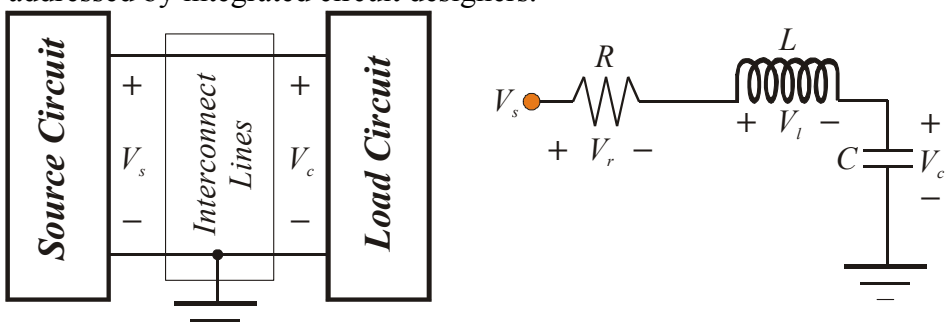


Figure (P1.3)

(a). The quality factor, Q of the circuit at hand is the ratio of the reactance of the inductor to the series resistance at the resonant frequency, say ω_o, of the circuit. Show that Q is given by

$$Q = \frac{1}{\omega_o RC} = \frac{1}{R}\sqrt{\frac{L}{C}}\ .$$

(b). Derive expressions for the transfer functions, $V_r(j\omega_o)/V_s(j\omega_o)$, $V_l(j\omega_o)/V_s(j\omega_o)$, and

$V_c(j\omega_o)/V_s(j\omega_o)$. Use these functions to demonstrate that the magnitudes of the capacitor voltage, V_c, and the inductor voltage, V_l, are *Q–times* larger than the magnitude of the source voltage, V_s, at the resonant frequency of the circuit.

(c). In terms of Q and ω_o, determine the *3–dB* bandwidth, say ω_b, of the circuit transfer function, $V_c(j\omega_o)/V_s(j\omega_o)$. Using EXCEL or other suitable software, plot the normalized bandwidth, ω_b/ω_o, versus Q for $0 < Q \leq 6$.

(d). Show that in the steady state and at circuit resonance, the energy delivered to the inductor is the negative of the energy delivered to the capacitor. Give an engineering interpretation of this observation.

PROBLEM #1.4

Reconsider the circuit of Figure (P1.3) under the condition that the source voltage, V_s, is an idealized unit step function. Moreover, take the capacitor voltage, V_c, as the response to this unit step excitation. In an ideal interconnect between two circuits, it is desirable that the output (V_c) respond instantaneously to the applied input. Clearly, this type of response is unrealizable because the capacitor prohibits instantaneous voltage changes. But in the steady state, the capacitor behaves as an open circuit and the inductor emulates a short circuit, thereby ultimately allowing the output to follow faithfully the applied input. This ability to follow the input is a desirable trait, but questions must be raised as to how much elapses before steady state operating conditions are closely emulated.

(a). Show that the transfer function, say $H(s)$, of the circuit is of the form,

$$H(s) = \frac{V_c(s)}{V_s(s)} = \frac{H(0)}{1 + \left(\frac{2\zeta}{\omega_n}\right)s + \left(\frac{s}{\omega_n}\right)^2}.$$

Provide analytical expressions for $H(0)$, the damping factor, ζ, and the undamped natural frequency, ω_n, and give engineering interpretations of each of these parameters. Relate ζ and ω_n to Q and ω_o, respectively, as introduced in the preceding problem.

(b). What are the initial and steady state time domain values of the capacitor voltage response, $v_c(t)$?

(c). Assume that the circuit is underdamped; that is, $\zeta < 1$. Determine the time domain capacitor voltage, $v_c(t)$, and cast this voltage in the form,

$$v_c(t) = v_c(\infty) - v_e(t),$$

where $v_e(t)$ can be interpreted as an "error" signal between the steady state, or ultimately desired, response and the actual time domain response. Use EXCEL or other suitable software to plot the error signal versus the normalized time, $\omega_n t$, for damping factor, ζ, values of $0.25,\ 0.5,\ 1/\sqrt{2}$, and 0.9.

(d). The one percent settling time, t_s, is the time required for the magnitude of the unit step response to achieve and forever maintain its steady state value to within $\pm 1\%$; that is,

$$|v_e(t_s)| \leq 0.01|v_c(\infty)|.$$

Derive a relationship for this settling time in terms of damping factor.

(e). What is the minimum damping factor commensurate with an error signal that is never any larger than *one per cent* of the steady state response? For a *1%* settling time of *1 nSEC*, what is the minimum tolerable circuit resonant frequency?

PROBLEM #1.5

The circuit depicted in Figure (P1.5) utilizes three ideal transconductor amplifiers to realize a bandpass filter whose center frequency (in units of radians/sec) is ω_o and whose quality factor is Q. Note that two of the transconductors have identical transconductances, g_m, while the third unit has a transconductance of g_{m3}.

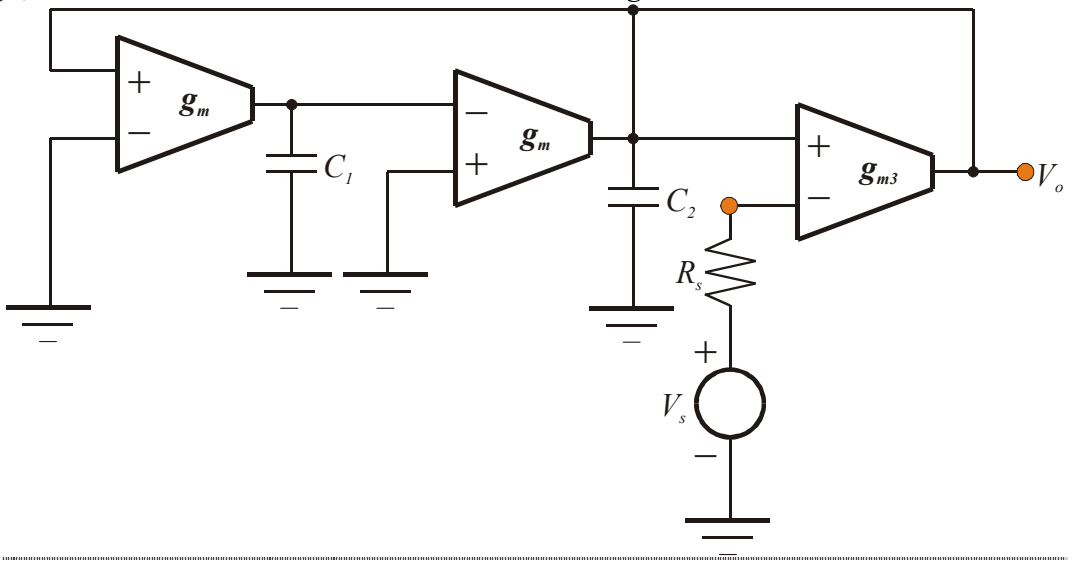


Figure (P1.5)

(a). Derive a generalized expression for the transfer function, $A_v(s) = V_o/V_s$.

(b). From the transfer function expression derived in Part (a), provide general expressions for the center frequency, ω_o, and the quality factor, Q, of the bandpass filter.

(c). What is the voltage gain at the center frequency of the filter?

(d). Assume that the transconductances, g_m and g_{m3}, are electronically adjustable. Can transconductor adjustments be made to control the center frequency and quality factor independently?

(e). Is it advantageous to control center frequency and quality factor independently in a commercial radio application of the filter? Explain briefly.

PROBLEM #1.6

The circuit in Figure (P1.6) is a model of a commonly utilized amplifier that is compensated to ensure stable performance at high signal frequencies.

(a). Derive a generalized expression for the low frequency voltage gain, $A_v(0) \triangleq A_{vo} = V_o/V_s$.

(b). Derive an expression for the time constant attributed to the pole incurred by the indicated capacitance, C.

(c). If the transconductance parameter, g_m, can be varied at will, what is the maximum attainable gain-bandwidth product of the circuit?

(d). Derive an expression for the driving point input impedance seen by the signal source comprised of Thévenin voltage V_s and Thévenin resistance, R_s.

(e). Derive an expression for the driving point output impedance seen by the load resistance, R_l.

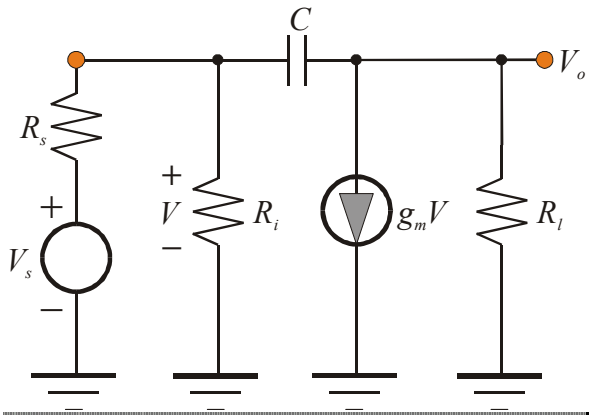


Figure (1.6)

PROBLEM #1.7

Under very high frequency operating conditions, Figure (P1.7) is a reasonable approximation of the equivalent circuit of a tuned amplifier realized in submicron metal-oxide-semiconductor field-effect transistor (MOSFET) device technology. The indicated circuit architecture is a simplified version of a radio frequency (RF) amplifier commonly utilized in the front end of a radio receiver or cellular telephone. The input signal source is represented by its Thévenin equivalent circuit, which consists of voltage source V_s and resistance R_s. In an RF application, the Thévenin resistance, R_s, generally represents the characteristic impedance of the transmission line that couples the antenna signal source to the amplifier input port. The output, or response, to the input signal, V_s, is the indicated voltage, V_o, which is developed across the load inductance L_o. The actual MOSFET is modeled by the frequency dependent current controlled current source, $(\omega_T/s)I$, and the capacitance, C_i. Typically, ω_T is of the order of the mid tens of gigaradians/sec, while C_i is typically in the range of the mid tens of femptofarads. The inductance, L_i, is a circuit element that is exploited to achieve maximum power transfer between the applied input signal and the amplifier input port, whose input impedance is delineated as $Z_{in}(s)$. Note that regardless of the nature and numerical value of the transistor and circuit parameters, the model in Figure (P1.7).

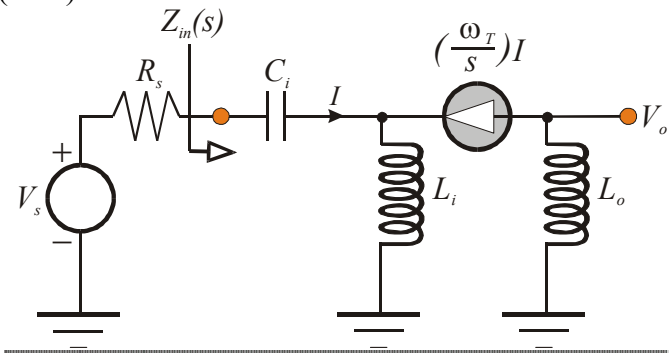


Figure (P1.7)

(a). Show that the indicated input impedance, $Z_{in}(s)$, is expressible as,

$$Z_{in}(s) = R_{eff} + sL_{eff} + \frac{1}{sC_{eff}}.$$

Give, in terms of C_i, L_i, and ω_T, expressions for the effective input resistance, inductance, and capacitance, R_{eff}, L_{eff}, and C_{eff}, respectively.

(b). Let the resonant frequency of the input impedance be denoted as ω_i. What is ω_i in terms of inductance L_i and capacitance C_i? What design condition must be satisfied at the resonant frequency to achieve a match terminated input port; that is, $Z_{in}(j\omega_i) \equiv R_s$?

(c). Show that under steady state sinusoidal operating conditions and the match terminated constraint focused upon in the preceding part of this problem, the voltage gain of the RF amplifier can be written in the form,

$$A_v(j\omega) = \frac{V_o}{V_s} = -\frac{L_o/2L_i}{1 + jQ\left(\frac{\omega}{\omega_i} - \frac{\omega_i}{\omega}\right)},$$

where Q is the quality factor associated with the input amplifier port at the resonant frequency, ω_i.

(d). With a source resistance, R_s, of *50 Ω,* a desired tuned center frequency, ω_i, of $2\pi(1200\ MHz)$, and a transistor that has $\omega_T = 2\pi(20\ GHz)$, compute the requisite values of output inductance, L_o, tuning inductance, L_i, and circuit quality factor, Q for a tuned center frequency gain magnitude of *20 dB*.

PROBLEM #1.8

The circuit in Figure (P1.8) uses two transconductors and two capacitors to realize a notch filter. Notch filters are often used in communication networks whenever an undesired input signal at a known frequency, say ω_o, must be sharply attenuated or even eliminated from the communication channel. Accordingly, an ideal notch filter delivers nonzero transfer function at both very low and very high signal frequencies and zero transfer function at the undesired frequency, ω_o.

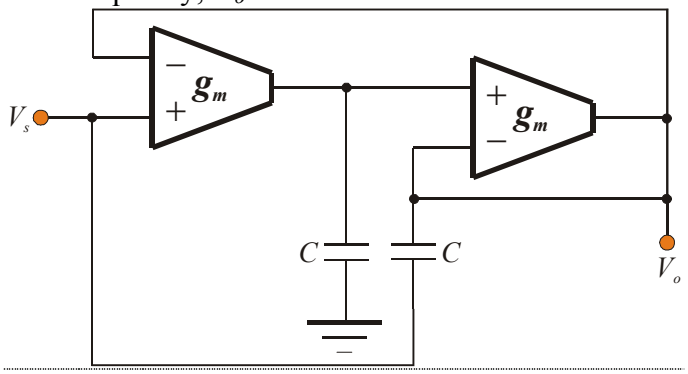


Figure (P1.8)

(a). Derive a generalized expression for the transfer function, $A_v(s) = V_o/V_s$.

(b). What is the notch frequency of the filter?

(c). What is the value of the filter transfer function at <u>both</u> very low and very high frequencies?

PROBLEM #1.9

The circuit in Figure (P1.9a) is an equivalent circuit for a transconductance amplifier whose output port is terminated in a shunt interconnection of a load resistance, R_L, and a load capacitance, C_L. This equivalent circuit is to be reduced to the Norton architecture shown in Figure (P1.9b), where the Norton transadmittance, $Y_n(s)$, is understood to be a function of frequency and pertinent circuit parameters.

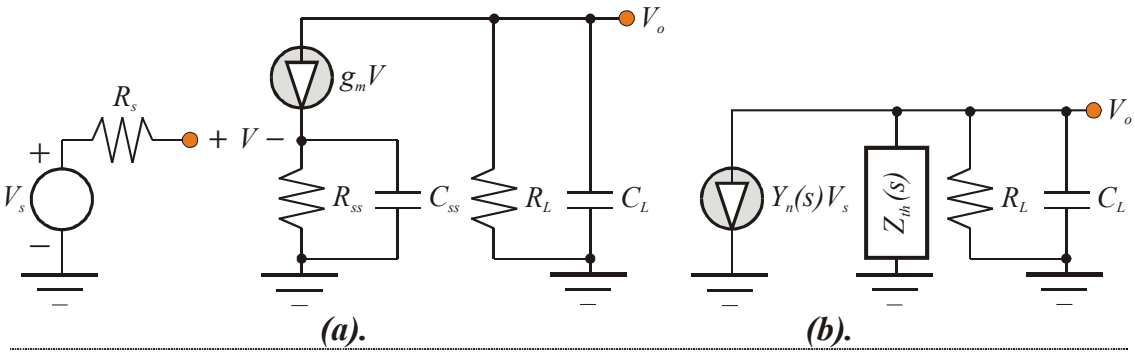


Figure (P1.9)

(a). Derive an expression for the Norton transadmittance function, $Y_n(s)$.

(b). Derive an expression for the indicated Thévenin impedance, $Z_{th}(s)$.

(c). The capacitance, C_{ss}, creates both a left half plane pole and a left half plane zero in the voltage transfer function, V_o/V_s. If the time constant associated with the left half plane zero established by C_{ss} is selected to cancel, the time constant, R_LC_L, of the shunt load, give an expression for the resultant *3-dB* bandwidth of the circuit.

PROBLEM #1.10

Amplifiers are commonly exploited in monolithic analog technologies to synthesize effective resistances whose values can be controlled by suitable biasing voltages. A case in point is the equivalent circuit of such a structure offered in Figure (P1.10). Determine the effective resistance, say R_{Leff}, established by the circuit between Node ① and ground.

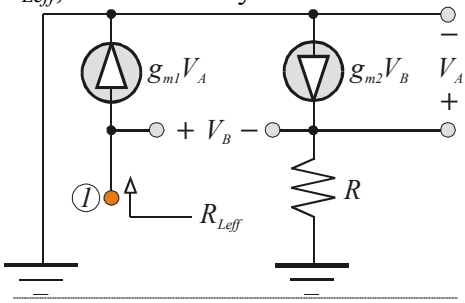


Figure (P1.10)

PROBLEM #1.11

Figure (P1.11a) is a valid linearized equivalent circuit of a voltage amplifier realized in bipolar junction transistor (BJT) device technology. The input signal source is represented by its Thévenin equivalent circuit, which consists of voltage source V_s and resistance R_s. The output response to this input signal is the indicated voltage, V_o, which is developed across the shunt interconnection of load resistance R_l and load capacitance C_l. The actual BJT is modeled by the current controlled current source, βI, and the three resistances, r_o, r_b, and r_π. The resistance, R_e, is a circuit element used for biasing and linearity purposes. It is generally chosen to be of the order of fifty to a few hundred ohms.

(a). Derive expressions for the Norton parameters, transconductance G_{sn} and resistance R_{out}, for the output port Norton equivalent circuit shown in Figure (P1.11b).

(b). In terms of the aforementioned Norton parameters and the load variables, R_l and C_l, derive an expression for the overall voltage gain, $A_v(s) = V_o/V_s$.

(c). Using the results of the preceding two parts of this problem, find the low frequency value of the voltage gain, V_o/V_s, of the circuit. Simplify this gain expression for the

case of large r_o and large β.

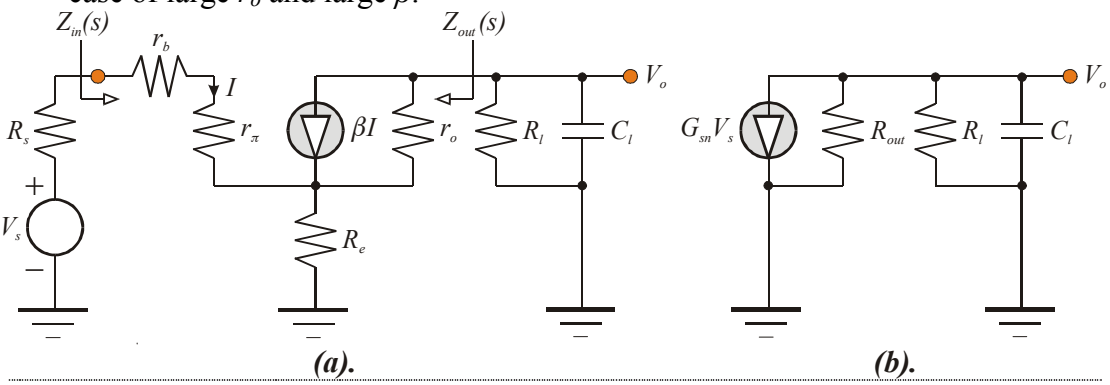


Figure (P1.11)

(d). In terms of R_{out} and R_l, give an expression for the *3-dB* bandwidth, say ω_b, of the circuit. Approximate this result for the case of large r_o and large β.

(e). Derive an expression for the low frequency input resistance, $Z_{in}(0) \triangleq R_{in}$, seen by the entire signal source circuit. Simplify this expression for the case of large r_o.

(f). Take $R_s = 300\ \Omega$, $R_l = 1\ K\Omega$, $\beta = 100$, $r_b = 190\ \Omega$, $r_\pi = 1.5\ K\Omega$, $r_o = 80\ K\Omega$, $R_e = 100\ \Omega$, and $C_l = 10\ pF$. Calculate the exact and the approximate values of the Norton transconductance, G_{sn}, the low frequency voltage gain, $A_v(0)$, the output resistance, R_{out}, the low frequency input resistance, R_{in}, and the circuit *3-dB* bandwidth, ω_b. Compare respective exact and approximate computations by calculating percentage errors of the individual approximations.

PROBLEM #1.12

The transfer function of the circuit studied in PROBLEM # 1.11 is expressible in the form,

$$A_v(s) = \frac{A_v(0)}{1 + s/\omega_b}.$$

(a). Determine the delay response $D(\omega)$ and the zero frequency value $D(0)$, of the input - to- output (I/O) delay in terms of the *3-dB* bandwidth, ω_b.

(b). In terms of ω_b, what is the signal frequency, say ω_d, at which the delay is degraded from its zero frequency value by a factor of the square root of two?

PROBLEM #1.13

The circuit model of the amplifier shown symbolically in Figure (P1.13a) is the structure depicted in Figure (P1.13b). The amplifier in question is utilized in the system offered in Figure (P1.13c).

(a). Derive an expression for the Thévenin voltage gain seen by the terminating load resistance, R_l.

(b). Derive an expression for the Thévenin output resistance seen by the terminating load resistance.

(c). Simplify the expressions determined in the foregoing two parts of this problem for the case of small R_o and large A_o.

(d). What is the driving point input resistance, R_{in}, "seen" by the applied signal source?

(e). Is the system in Figure (P1.13c) better suited for voltage amplification, transimpedance amplification, or transconductor action?

(f). For large R_o and large A_o, how might R_2 be chosen to realize a nearly unity gain voltage buffer?

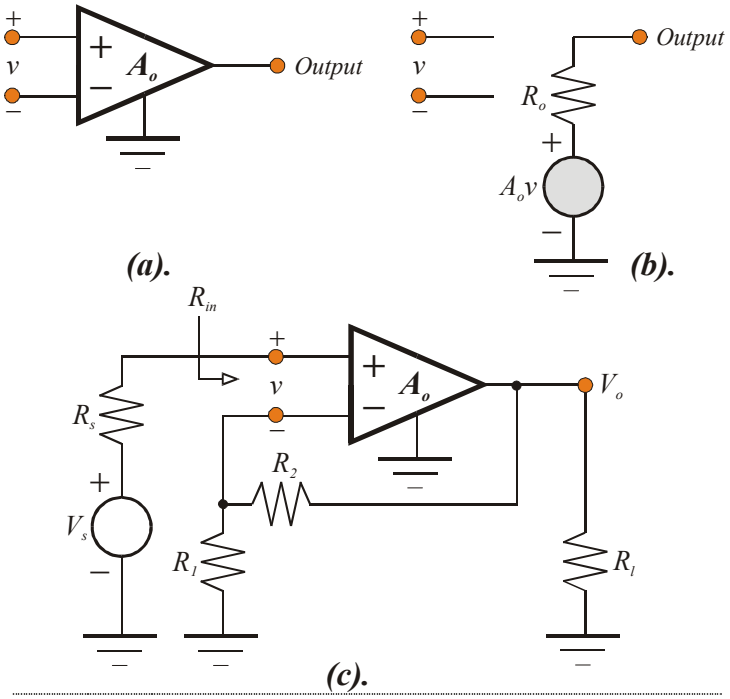


Figure (P1.13)

PROBLEM #1.14

The amplifier addressed in Figures (1.13a) and (1.13b) is utilized in the system offered in Figure (P1.14).

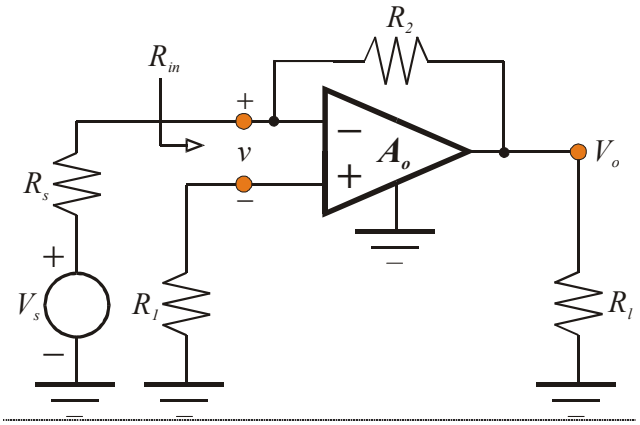


Figure (P1.14)

(a). Derive an expression for the Thévenin voltage gain seen by the terminating load resistance, R_l.

(b). Derive an expression for the Thévenin output resistance seen by the terminating load resistance.

(c). Simplify the expressions determined in the foregoing two parts of this problem for the case of small R_o and large A_o.

(d). What is the driving point input resistance, R_{in}, "seen" by the applied signal source?

(e). Is the system in Figure (P1.14) better suited for voltage amplification, transimpedance amplification, or transconductor action?

PROBLEM #1.15

Figure (P1.15) depicts the schematic diagram of a two-pole lowpass filter. The two amplifiers indicated in the subject schematic representation can be viewed as ideal in the senses of delivering infinitely large input and zero output impedances. Observe that the amplifier providing a voltage gain of A_1 is a non-phase inverting structure, while the amplifier that delivers a voltage gain magnitude of A_2 is a phase inverting unit.

(a). Derive an expression for the voltage transfer function, V_o/V_s, and cast this function in the form,

$$\frac{V_o}{V_s} = \frac{A(0)}{1 + \frac{s}{Q_o\omega_o} + \left(\frac{s}{\omega_o}\right)^2},$$

where $A(0)$ symbolizes the zero frequency gain of the circuit, Q_o is the circuit quality factor, and ω_o represents the undamped natural frequency of the circuit. Provide, in terms of R, C, A_1, and A_2, analytical expressions for $A(0)$, Q_o, and ω_o.

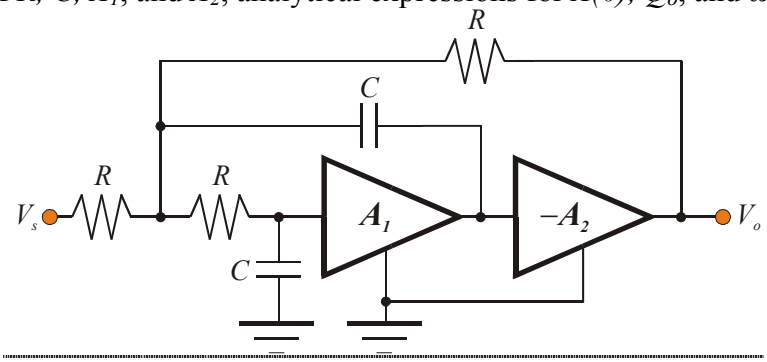


Figure (P1.15)

(b). Under what condition does the circuit become a sinusoidal oscillator? State this condition and give the corresponding oscillation frequency.

(c). What condition must be satisfied to ensure the unconditional stability of the circuit?

(d). If Q_o is the inverse of *root two*, what is the *3-dB* bandwidth of the resultant lowpass filter?

(e). For the condition in (d), give the pole locations of the filter.

PROBLEM #1.16

Wideband analog and high-speed digital integrated circuits necessarily use minimal geometry transistors whose small breakdown voltages preclude their capability to sustain large collector-emitter (or drain-source) voltages over even relatively small time periods. To protect these devices from transient voltage overstress, a second order *LC* filter of the form shown in Figure (P1.16) is often inserted between the *ON/OFF* power line switch and the power supply pad of the integrated circuit. In this circuit, R_l represents the steady state load to which power is to be supplied and is nominally the ratio of the steady state load voltage -to- the steady state load current. Thus, if the desired quiescent pad voltage of an integrated circuit is *3.3 volts* and if this circuit is to draw a quiescent current of *12 mA*, R_l = *3.3/12 mA* = *275 Ω*. The filter itself consists of the inductance, L_s, which includes any parasitic inductance associated with the power supply bus routing on chip, and the capacitance, C_l, which includes parasitic power supply pad capacitance. The

resistance, R_s is generally small and includes the effects of power bus losses and finite inductance quality factor *(Q)*. By the way, the rubberized or plastic-coated "bump" you see in the power line that connects your laptop computer to an energy source is the inductance in Figure (P1.16). The indicated voltage, V_p is the Thévenin energizing voltage for the chip, while the switch, which is closed at *time* $t = 0$, allows the filter input voltage, $v_i(t)$, to emulate the step function, $V_p u(t)$. It is to be understood that the fundamental purpose of the filter is to slow the rate of power delivery from the input port, where $v_i(t)$ is measured, -to- the output port, where voltage $v_o(t)$ is established, so that $v_o(t)$ rises monotonically with time toward its steady state value with little or no voltage overshoot.

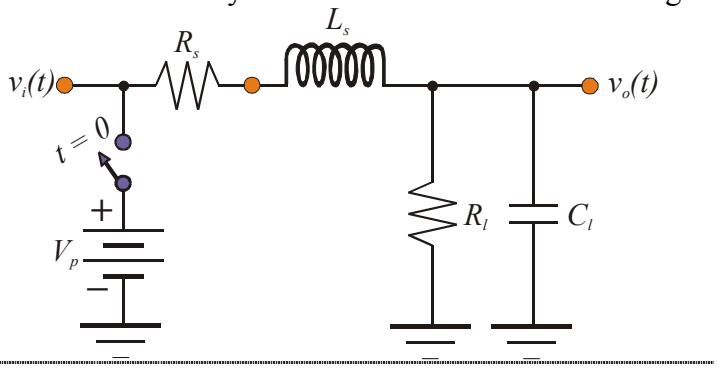


Figure (P1.16)

(a). The filter in Figure (P1.16) is clearly a second order circuit. In view of the discussion provided above, should the circuit poles, whose frequencies might be labeled, p_1 and p_2, be real numbers or complex conjugates? Briefly explain your rationale.

(b). Derive an expression for the transfer function, $H(s) = V_o(s)/V_i(s)$ and in the process, show that the pole frequencies satisfy the relationships,

$$\frac{1}{p_1} + \frac{1}{p_2} = \frac{L_s}{R_l + R_s} + \left(R_s \| R_l\right) C_l$$

and

$$\frac{1}{p_1 p_2} = \left(\frac{R_l}{R_l + R_s}\right) L_s C_l = H(0) L_s C_l \, .$$

(c). Assume that the poles are real and that their frequencies relate as $p_2 = k p_1$, where k is understood to be greater than or equal to one. For $k > 1$, show that the time domain response, normalized to the steady state value of the response, is

$$v_{on}(t) = \frac{v_o(t)}{H(0) V_p} = 1 - \left(\frac{k}{k-1}\right) e^{-p_1 t} + \left(\frac{1}{k-1}\right) e^{-k p_1 t} \, ,$$

while for $k = 1$, confirm that

$$v_{on}(t) = \frac{v_o(t)}{H(0) V_p} = 1 - \left(1 + p_1 t\right) e^{-p_1 t} \, .$$

(d). Plot the normalized responses determined in Part (c) -versus- the normalized time parameter, $t_n = p_1 t$ for $k = 1,\ 1.5,\ 3,$ and 10. What value of k might be desired to ensure the realization of the slowest possible step response for any given real number value of p_1?

(e). Let T_R represent the rise time of the filter; that is, T_R is the time required after the switch is closed for the output response to achieve *90%* of its steady state value. For the optimal value of k (in the sense of a maximally slowed response) determined in Part (d), confirm that $p_1 T_R \approx 3.9$.

(f). Assume now that $R_l >> R_s$ and $L_s >> R_s R_l C_l$. For the optimal operating condition stipulated in Part (e), show that a rise time of T_R is achieved if

$$L_s \approx \frac{T_R\left(R_l + R_s\right)}{1.95}$$

and

$$C_l \approx \frac{T_R}{7.8 R_l}.$$

(g). Assume that a certain integrated circuit is to be energized by a *3.3 volt* battery that is switched on at *time t = 0*. Assume further that the net effective Thévenin source resistance (R_s) is *15 Ω* and that the effective steady state load resistance (R_l) is *1020 Ω*. The latter resistance corresponds nominally to *3.3 volts* delivered to a load drawing *3.23 mA*. A *0 -to- 90%* rise time (T_R) of at least *200 μSEC* is desired to protect the active devices in the given circuit. Design the protection filter and simulate it on SPICE to confirm the stipulated rise time objective.

PROBLEM #1.17

The amplifier depicted in Figure (P1.17) has infinitely large shunt input resistance, zero Thévenin output port resistance, and a finite open loop voltage gain, A_o. The capacitance, C_i, represents the effective shunt input port capacitance and since no other amplifier capacitances are delineated, this capacitance is presumably the dominant energy storage element in the overall circuit. The amplifier is set up to function as an inverting buffer and accordingly, R_f is selected to equal the effective source resistance, R_s.

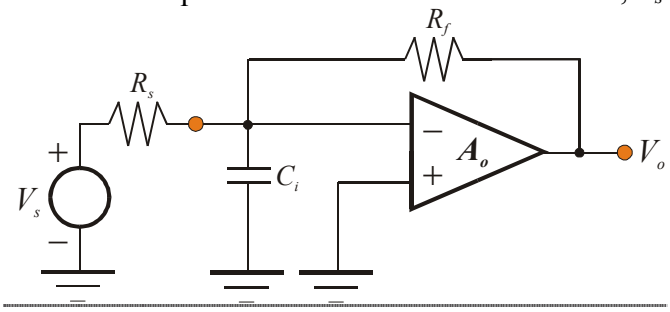


Figure (P1.17)

(a). Derive an expression for the closed loop voltage gain, $A_v(s) = V_o(s)/V_s(s)$.

(b). Derive an expression for the *3-dB* bandwidth, say B, of the circuit.

(c). Derive an expression for the low frequency signal voltage, say V_i, developed across the amplifier input port and show that this voltage tends toward zero as the gain parameter, A_o, tends toward infinity.

(d). Since infinitely large open loop amplifier gains are observed only in academic environments, it is of engineering interest to investigate the response error precipitated by finite gain. To this end, define the error, ε, to be the difference between the magnitude of the input source signal voltage and the magnitude of the resultant response, V_o, under the simplifying condition of $V_s = 1$ *volt*. At low signal frequen-

cies, what general condition must be satisfied by the gain parameter, A_o, if the design requirement is $\varepsilon \leq 2\%$?

PROBLEM #1.18

Numerous signal processing applications, such as transconductance amplifiers, phase detectors, and oscillators, demand current sources and sinks characterized by extremely high resistances at their current output ports. This design requirement is a daunting challenge when frequency response objectives mandate the use of deep submicron MOS technology transistors, which are plagued by relatively small drain-source channel resistances. The circuit in Figure (P1.18a) responds to the foregoing requirement by incorporating a feedback voltage amplifier into a traditional cascode current sink. In this exercise, assume that the amplifier is ideal in the senses of infinitely large input resistance, zero output resistance, and frequency-invariant open loop voltage gain, A_o. The indicated voltage, V_{bias}, is constant in that it derives from a bandgap reference subcircuit or some other form of temperature stable supply.

(a). Describe qualitatively how the use of the presumably ideal amplifier encourages ideal (constant output current) current sink action.

(b). Use the small signal model of Figure (P1.18b) to derive an expression for the indicated output resistance, R_{out}. Do not assume that the model parameters, λ_b, g_m, and r_o, are respectively identical for transistors *M1* and *M2*.

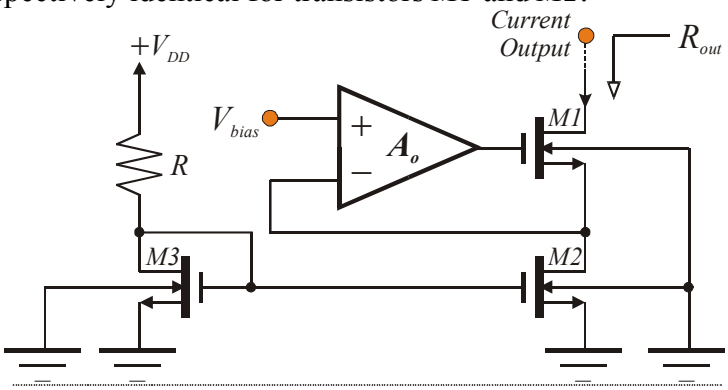


Figure (P1.18a)

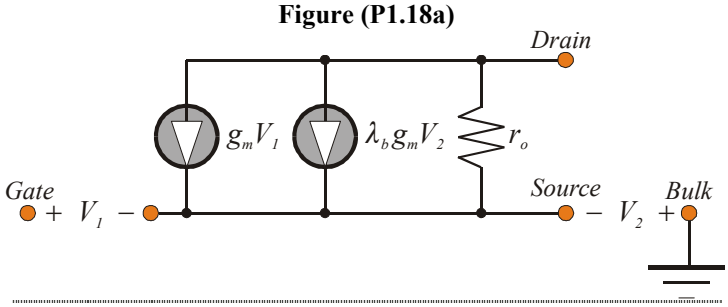


Figure (P1.18b)

PROBLEM #1.19

The circuit abstracted in Figure (1.19) is a gyrator, which has the capability of transforming capacitive load impedances, Z_l, to inductive input impedances, Z_{in}. Conversely, it can also transform inductive loads to driving point capacitive input impedances.

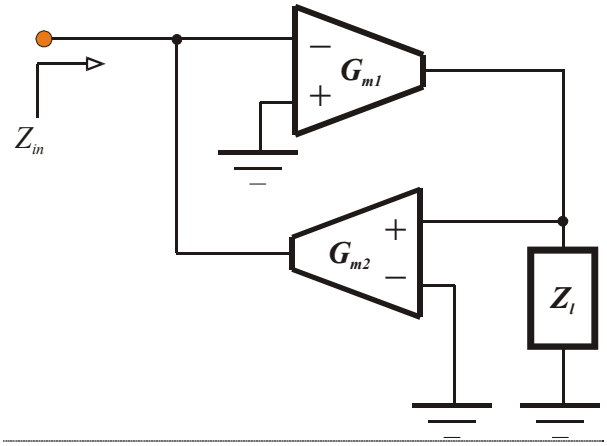


Figure (P1.19)

(a). Assuming ideal transconductors, derive a general expression for the driving point input impedance, Z_{in}.

(b). If the load impedance, Z_l, is the impedance of an inductance, say L, derive an expression for the resultant effective input capacitance, C_{in}.

PROBLEM #1.20

An active realization of a biquadratic filter architecture is offered in Figure (1.20), where all of the utilized transconductor amplifiers are ideal, balanced differential structures. Analyze the filter circuit to confirm that its voltage transfer function, $H(s) = V_o/V_s$, is

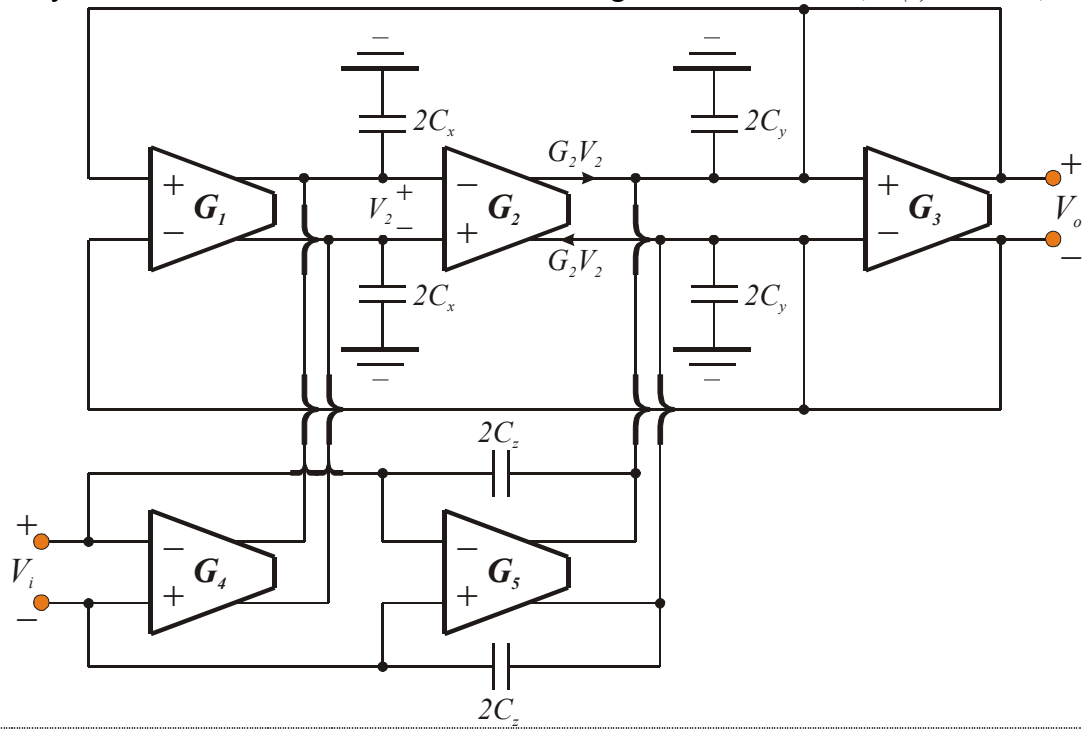


Figure (P1.20)

$$H(s) = \frac{c + bs + as^2}{1 + \frac{s}{Q\omega_n} + \left(\frac{s}{\omega_n}\right)^2}.$$

In particular, confirm that

$$a = \frac{C_x C_z}{G_1 G_2}, \qquad b = \frac{G_5 C_x}{G_1 G_2}, \qquad c = \frac{G_4}{\omega_n C_x},$$

$$\omega_n = \sqrt{\frac{G_1 G_2}{C_x\left(C_y + C_z\right)}},$$

and

$$Q = \sqrt{\left(\frac{G_1 G_2}{G_3^2}\right)\left(\frac{C_y + C_z}{C_x}\right)}.$$

PROBLEM #1.21

The biquadratic filter whose topological structure is abstracted in PROBLEM #1.20 is to be designed to realize a maximally flat, lowpass frequency response exhibiting unity gain at low signal frequencies and a *3-dB* bandwidth of *800 MHz*.

(a). Which transconductor(s) and which capacitor(s) can be removed from the given architecture?

(b). Design the circuit by calculating appropriate values of the remaining transconductances and capacitances. When possible, transconductance values can be equated to simplify the design methodology.

(c). Use SPICE to simulate the steady state frequency response and the time domain unit step response of the designed filter. Examine the resultant *3-dB* bandwidth and compare with the design requirement. Investigate whether any overshoot observed in the step response is in agreement with theoretic predictions.

PROBLEM #1.22

The biquadratic filter whose topological structure appears in Figure (P1.20) is to be designed to realize a bandpass frequency response exhibiting unity maximum gain at a center frequency of *800 MHz*. The *3-dB* bandwidth of the filter is to be *150 MHz*.

(a). Which transconductance(s) and capacitance(s) can be removed from the architecture?

(b). Design the circuit by calculating appropriate values of the remaining transconductances and capacitances. When possible, transconductance values can be equated to simplify the design methodology.

(c). Use SPICE to simulate the steady state frequency response and the time domain unit step response of the designed filter. Examine the resultant *3-dB* bandwidth and compare with the design requirement. Investigate the step response and provide engineering commentary on its time domain form.

PROBLEM #1.23

The biquadratic filter whose topological structure appears in Figure (P1.20) is to be designed to realize a notch at a frequency of *800 MHz*. The quality factor of the notch filter is to be at least five *(Q = 5)*, and the filter is to provide unity gain magnitude at both very low and very high signal frequencies.

(a). Which transconductance(s) and capacitance(s) can be removed from the architecture?

(b). Design the circuit by calculating appropriate values of the remaining transconductances and capacitances. When possible, transconductance values can be equated to

simplify the design methodology.

(c). Use SPICE to simulate the steady state frequency response and the time domain unit step response of the designed filter. Examine the resultant *3-dB* bandwidth and compare with the design requirement. Investigate the step response and provide engineering commentary on its time domain form.

PROBLEM #1.24

Reconsider the lowpass filter designed in PROBLEM #1.21.

(a). Use SPICE to simulate the envelope delay response. What is the very low frequency value of this delay? Does this observation agree with theoretic predictions? Explain any disparity.

(b). Modify the circuit to ensure a maximally flat delay response at a value equal to the low frequency delay value observed in Part (a) of this problem.

(c). Use SPICE to simulate the steady state delay and frequency responses of the modified filter. Do the observed low frequency delay and *3-dB* bandwidth (bandwidth of magnitude response) agree with theoretic predictions? Explain any disparities.