Resume

Mohsin M. Jamali
Professor
Department of Electrical Engineering and Computer Science
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EDUCATION:

Ph.D. Electrical Engineering, 1984
University of Windsor, Windsor, Ontario, Canada

M.Sc. Electrical Engineering, 1979
University of Saskatchewan, Saskatoon, Saskatchewan, Canada

B.Sc. Electrical Engineering, 1975
Aligarh Muslim University, Aligarh, India

EXPERIENCE:

1998- Present Professor
Department of Electrical Engineering and Computer Science, University of Toledo, Toledo

01/2000-08/2000 Graduate Director
Department of Electrical Engineering and Computer Science, University of Toledo, Toledo

1995- 1998 Associate Professor
Department of Electrical Engineering and Computer Science, University of Toledo, Toledo

1990- 1995 Associate Professor
Department of Electrical Engineering, University of Toledo, Toledo, Ohio

1984-1990 Assistant Professor
Department of Electrical Engineering, University of Toledo, Toledo, Ohio

1983-1984 Instructor
School of Computer Science, University of Windsor, Windsor, Ontario, Canada

Other related experience- teaching, industrial, etc.

*Electronic Engineer, Advanced Business Computer Systems Inc., Windsor, Canada.1981-1982
*Consultant, Electronic Concepts & Engineering, Toledo, Summer 1996 & 1997
*Seminar Instructor for 3-day course on Fundamentals of Multiplexing for the Society of Automotive Engineers 1996-2000
*Consultant for NATO Science for Peace program for real time health monitoring of structures. 1999.
*Offered a Web-Course on Advanced Computational Methods, The U. of Toledo, Summer 2000.
*Presented tutorial on intelligent vehicles at the International Conference on Acoustic Speech and Signal Processing, Istanbul, Turkey, June 2000.

Books: Fundamentals of In-Vehicle Networks submitted to the Society of Automotive Engineers. This book covers newtork protocols for vehicles, ITS data bus and other applications.

Keynote Lectures (Invited)

In-Vehicle Networks - International Conference on Robotics, Vision, Information and Signal Processing, Penang, Malaysia July 20-22, 2005.

Embedded Sensor Array Processing -Modern Trends in Electronics and Communications Conference (MTEC-08), Aligarh, India, March 8, 2008

MultiCore System – International Conferece on Multimedia Multimedia, Signal Processing And Communication Technologies **(**IMPACT-2009**),** Aligarh, India, March 16, 2009

Journal publications:

1. M. M. Jamali, P. Bumrungthum, N. Mohankrishnan," A Systolic Array Architecture of Linear Predictive Coding (LPC)" Published in Signal Processing IV, Theories and Applications, by Lacoume, Chehikian, Martin, Malbos, Vol. 2, PP. 907-910. Elsevier Science Publishers B.V. (North-Holland). 1988

2. M. M. Jamali, P. Bumrungthum, N. Mohankrishnan," A Parallel Algorithm for Linear Predictive Coding Analysis (LPC)" Published in Signal Processing IV, Theories and Applications, by Lacoume, Chehikian, Martin, Malbos, Vol. 2, PP. 759-762. Elsevier Science Publishers B.V. (North-Holland). 1988

3. L. P. Eugene, P.J. Fernendes, M. M. Jamali, S.C. Kwatra, J. Budinger "Multicarrier Demodulator Architecture for Onboard Processing Satellites". Journal of Spacecraft and Rockets, Volume 28, Number 5, Sept./Oct. 1991, PP. 580-586.

4 . K. Dezhgosha, M.M. Jamali, S.C. Kwatra, "A VLSI Architecture for Real-Time Image Coding Using A Vector Quantization Based Algorithm," IEEE Transactions on Acoustic, Speech and Signal Processing. Vol. 40, No.1, PP.181-189, January 1992.

5. M. M. Jamali, M. Hussain and G. A. Jullien," Design of a Signal Processing Cell." Abstract published in the Ohio Journal of Science, Vol. 86, No. 2, Page 35.

6. A. Thanawala, S.C. Kwatra, M.M. Jamali, J. Budinger "An Efficient Demultiplexing Algorithm for Non-Contiguous Carriers", Journal of Spacecraft and Rockets, Volume 29, Number 4, July/August 1992, PP. 498-501.

7. A. L. Enriquez, A. H. Eltimsahy, M. M. Jamali,"A Real Time Multiprocessor System for Flexible Controller for Robot Manipulators", IEEE Micro, December 1995, PP. 55-60.

8. M. M. Jamali, R. Tabar, S. C. Kwatra, "SIMD/MIMD Architectures for DOA Computations for Narrowband/Broadbanc Sources," International Journal of Computers and Applications, Volume 21, Number 3, 1999 105-113.

9. M. M. Jamali, " A Comparative Study of Physical Layers of In-Vehicle Multiplexing Systems" SAE 1999 Transactions, Journal of Passenger Cars, Vol-108-6, PP. 2315-2321.

10. M. M. Jamali, William A. Hoyt and Karl W. Swonger, Jr., "Design of a CAN to IEEE 802.11 Wireless LAN Node," SAE 2001 Transactions, Vol. 110, Journal of Passenger Cars: Electronic and Electrical Systems, Section 7, pages 115-121.

11. M. M. Jamali, M. M. Brown, C. C. Sheh, C. Suriyakomal, M. Y. Niamat, " A CAN based Real Time Embedded System for DC Motor Control," SAE 2002 Transactions, Vol. 111-7, Journal of Passenger Cars: Electronic and Electrical Systems, , pages 233-239.

12. M.Y. Niamat D.M. Nemade M.M. Jamali, "Test, Diagnosis, and Fault Simulation of Embedded RAM Modules in SRAM-Based FPGAs." Microelectronics Engineering, Elsevier, March 2006, pp. 194-203.

Other Publications:

1. M. M. Jamali, M. Aref and G. A. Jullien," Algorithm Partitioning and Allocation for a Data Flow Signal Processor." Abstract published in the Ohio Journal of Science, Vol. 86, No. 2, Page 35.

2. M. M. Jamali, G. A. Jullien, W. C. Miller, S. I. Ahmad, "Interactive Programming Environment for a Data Flow Structure." Abstract published in the Ohio Journal of Science, Vol. 85, No. 2, Page 67.

3. M. M. Jamali, N. Mohankrishnan and M. Shridhar,"A Combined Speaker and Digit Recognition System," Abstract published in the Ohio Journal of Science , 1987.

Conference Publications:

1. R. Billinton, G.A. Hamoud, M. M. Jamali,"Reliability Evaluation using Monte Carlo Simulation." presented at the 1979 Canadian Electrical Association Spring meeting in Vancouver and published in their transactions.

2. R. Billinton, M. M. Jamali,"Applications and Comparisons of Generating Capacity Reliability Indices", presented at the International Electrical, Electronic Conference and Exposition in Toronto, Oct. 1979.

3. G. A. Jullien, M. M. Jamali, W.C. Miller," Implementaion of a Spectrum Analyzer Using a Memory Intensive Architecture." Canadian Communication and Energy Conference, Montreal, Oct. 1982.

4. M. M. Jamali, G. A. Jullien, W.C. Miller, S.I. Ahmad, "A Real Time General Purpose Signal Processor." presented at the IEEE 1984 International Conference on Acoustic, Speech and Signal Processing in San Diego.

5. M. M. Jamali, G. A. Jullien, W. C. Miller, S. I. Ahmad, "Software Techniques for Programming a General Purpose Data Flow Signal Processor," presented at the International Conference on Acoustic, Speech and Signal Processing, Tampa, March 1985.

6. M. M. Jamali, G. A. Jullien and S.I. Ahmad,"An Expert System for Partitioning and Allocating Algorithms."Published in the Proceedings of the 1986 International Conference on Systems, Man and Cybernatics, Vol. 2, Pages 1113-1117.

7. M. M. Jamali, M. M. Hussain, G. A. Jullien," A Signal Processing Cell Architecture." Paper presented at the IEEE 1987 International Conference on Acoustic, Speech and Signal Processing.

8. M. M. Jamali, N. Mohankrishnan, G. A. Jullien and M. Shridhar, " Real Time Implementation of a Simultaneous Speaker/Digit Recognition System," Presented at the 1987 Midwest Symposium on Circuits and Systems, Syracuse, New York

9. K. Dezhgosha, S.C. Kwatra, M.M. Jamali," A VQ-based High Quality Image Coding Algorithm ForReal-Time Applications," Presented at the 1988 Midwest Symposium on Circuits and Systems, St. Louis.

10. K. Dezhgosha, M.M. Jamali, S.C. Kwatra, "Real Time VLSI Architecture for a VQ-based High Quality Image Coding Algorithm. Published in the IEEE 1989 International Conference on Acoustic, Speech and Signal Processing Proceedings.

11. K.Dezghosha, M.M. Jamali, S.C. Kwatra, "A Perceptually-Based Heuristic Codebook Design Algorithm,"Published in the 1989 International Symposium on Circuits and Systems Proceedings,PP. 1370-1373.

12. B. D. Goel, M. M. Jamali, S. C. Kwatra, " Real Time Architecturefor Vector Quantization in Residue NumberSystem."Published in the 1989 International Symposium on Circuits and Systems Proceedings PP. 204-207.

13. M.Y. Niamat, R.G. Molyet, M.M. Jamali, K.J. Cios, D.D. Raftopoulos,"Applications of Sytolic Architectures to Motion Analysis Studies" Published in the 1989 IEEE Pacific Rim Conference on Signal Processing. PP. 60-63.

14. P.J. Fernendes, L.P. Eugene, M. M. Jamali, S.C. Kwatra, J. Budinger "A Parallel Pipelined Architecture for A Digital Multicarrier Demodulator". Paper presented at International Communication Satellite Systems Conference, March 1990. pp. 285-294.

15. K. Dezghosha, M.M. Jamali, S.C. Kwatra, "A Codebook Distortion and Comparator (CDC) Chip Architecture For Real-Time Image Coding," Paper published in the 1990 International Symposium on Circuits and Systems. PP. 3034-3037.

16. K. Dezghosha, M.M. Jamali, S.C. Kwatra, "Performance Evaluation of the VQ Based Image Coding Algorithm," Paper published in the 1990 International Symposium on Circuits and Systems. PP.3057-3060.

17. A. Thanawala, S.C. Kwatra, M.M. Jamali, J. Budinger "An Efficient Demultiplexing Algorithm for Non-Contiguous Carriers", IEEE International Telecommunications Symposium ITS'90 pp. 0373-0376.

18. P. Fernandes, S. C. Kwatra, M.M. Jamali, J. Budinger, "A Reconfigurable Transmultiplexor Architecture," Paper presented at the IEEE 1991 International Conference on Acoustic, Speech and Signal Processing.

19. S.C. Kwatra, M.M. Jamali,"A Reconfigurable Multicarier Demodulator Architecture", presented at NASA Space Technology Conference, Cleveland Ohio, Nov. 1991.

20. A. H. Djouadi, M. M. Jamali, S.C. Kwatra," A Parallel QR Architecture for the Symmetrical Tridiagonal Eigenvalue Problem," Asilomar Conference on Signals, Systems and Computers, Pacific Grove, October 1992. PP. 591-595.

21. R. Sheelvant, M.M. Jamali, A. H. Djouadi, S.C. Kwatra,"A Parallel Architecture for MUSIC Algorithm," International Conference on Digital Signal Processing Applications and Technology, Boston November 1992, PP. 778-796.

22. R. Tabar, M. M. Jamali, S.C. Kwatra, A.H. Djouadi," A Generalized Architecture for DOA Estimation for Wideband/Narrowband Sources," Proceedings of the SPIE's International Society for Optical Engineering , Architecture, Hardware, and Forward-Looking Infrared Issues in Automatic Target Recognition, pp. 336-346, April 1993, .

23. D. Wagner, S. C. Kwatra, M.M. Jamali,"A Single Chip High Data Rate QPSK Demodulator," Proceedings of the 1993 International Symposium on Circuits and Systems. pp. 2031-2034.

24. M. M. Jamali, S. C. Kwatra,"Design of Special Purpose Parallel Hardware for Real Time Applications," Proceedings of the 1993 National Aerospace and Electronic conference, Vol. 2. pp. 54-60.

25. R. Tabar, M. M. Jamali, S.C. Kwatra," An Architecture for DOA Estimation for Broadband Sources," Occean 93 conference proceedings, Vol. PP 253-256.

26. C. S. Lee, E.D. Smith, S. C. Kwatra, M. M. Jamali, A. G. Eldin," Embedded CMOS SRAM for an ASIC Implementation of a Satellite Communications Transmultiplexer", Presented at the 36th Midwest Symposium on Circuits and Systems.

27. M. Pakkurti, A. G. Eldin, S. C. Kwatra, M. M. Jamali,"Automated Synthesis and Verification of Configurable DRAM blocks for ASIC's", Presented at the Fifth Annual NASA Symposium on VLSI Design.

28. A. L. Enriquez, A. H. Eltimsahy and M. M. Jamali, " Design and Implementation of A Flexible Controller for Robot Manipulators," 1994 Midwest Symposium on Circuits and Systems.

29. M. M. Jamali, S. Ravindranath, S. C. Kwatra, A. G. Eldin, " ASIC Design of A Genralized Covariance Matrix Processor for DOA Algorithms," 1994 International Symposium on Circuits and Systems.

30. M.Y. Niamat, P.C. Mohanty, M. M. Jamali,"Novel Systolic Array Architecture for theComputation of the Similarity Matrix," Presented at the 1994 IASTED Modelling and Simulation Conference, Pittsburg, PA, May 1994.

31. M.Y. Niamat, M. M. Jamali, P.C. Mohanty,"Design of a Mesh-Type Systolic Array Architecture for the Fast Computation of the Single Linkage Algorithm," 1994 International Symposium on Circuits and Systems.

32. C. A. Carty, M. M. Jamali, A. G. Eldin, S. C. Kwatra, " A High Speed 800 Channel Digital Interpolator Network," 1995 International Symposium on Circuits and Systems.
PP. 85-88.

33.Y. Liang, M. M. Jamali, S. C. Kwatra, M. Alam, " A Multiprocessor Architecture for Generalized DOA Algorithms ," Published in Occean 95 Conference Proceedings.

35. M.M. Jamali, S.C. Kwatra, D. H. Shetty, " Module Generation Based VLSI Implementation of a Demultiplexer for Satellite Communications," 1996 International Symposium on Circuits and Systems. PP. 364-367.

36. M.M. Jamali, S.C. Kwatra, " VLSI Implementation of On board Processing Subsystems for Satellite Channels, Presented at the 1996 Midwest Symposium on Circuits and Systems.

37. M. Y. Niamat, D. Bitter, M. M. Jamali," FPGA Implementation of Hierarchical Clustering Algorithms" 1998 International Symposium on Circuits and Systems. (International)

38. M. M. Jamali, " A Comparative tudy of Physical Layers of In-Vehicle Multiplexing Systems" Presented at the 1999 SAE International Congress and Exposition.

39. Khalid S. AL-Olimat, Adel A. Ghandakly, Mohsin M. Jamali, "Adaptive Air-Fuel Ratio Control Of a SI Engine Using Fuzzy Logic Parameter Evaluations," Presented at the 2000 SAE International Congress and Exposition.

40. M. M. Jamali, M. Y. Niamat, "Incorporating DSP Applications in Vehicles", Presented at 2000 IEEE Workshop on Signal Processing Systems.

41. M. M. Jamali, William A. Hoyt and Karl W. Swonger, Jr., "Design of a CAN to IEEE 802.11 Wireless LAN Node," Presented at the 2001 SAE International Congress, Detroit, Michigan.

42. Mohsin M. Jamali, Mark M. Brown, C. C. Sheh, C. Suriyakamol, M. Y. Niamat, "A CAN Based Real-time Embedded System for DC Motor Control ," Presented at the 2002 SAE International Congress, Detroit, Michigan.

43. M. Y. Niamat, Rajesh Nambiar, M. M. Jamali," A BIST scheme for testing the interconnect of SRAM based FPGAs," Presented 45th IEEE Midwest Symposium on Circuits and Systems, Tulsa, OK, August 2002.

44. Mark M Brown and Mohsin M. Jamali, "Detection And Tracking Of Multiple Targets Within A Three-Dimensional Medium," Presented at the Asilomar Conference on Signals, Systems and Computers, November 2004.

45. Reza Jamasebi and Mohsin M. Jamali, "Authentication and Secure Communication for In-Vehicle Networks ," Presented at the 2005 SAE World Congress, Detroit, MI.

46. M. Y. Niamat, A. S. Ravinuthala, M. M. Jamali and S. R. Vemuru,"BIST for Embedded SRAMs in System on Chips," Presented at the ESA 2005.

47. Arnab Shaw, M. M. Jamali and Nathan Wilkins," Toward Bandwidth Invariance of Spatial Processing in the Non-Cooperative Receiver," Presented at the IEEE Workshop on Sensor Array and Multichannel Processing (SAM-2006), Waltham, Massachusetts, July 2006.

48. Mohsin M. Jamali, Abdel Affo, Nathan Wilkins, Philip D. Mumford, Ken Hahn, "DSP Based Implementation of Direction of Arrival for Wideband Sources," Presented at the IEEE 2007 Radar Conference.

49. M. Y. Niamat, Arunjit Sahni and M. M. Jamali," A Built in Self Test Scheme for Automatic Interconnect Fault Diagnosis in Multiple and Single FPGA Systems," Proceedings of the 50th IEEE MWSCAS 07 Conference, pp. 229 - 232, Aug. 5 -8, 2007 Montreal, Canada.

50. Ahmad Rizvi and Mohsin M. Jamali, " FPGA Implementation of Frequency Estimation Using Power Method and MUSIC Algorithm" Presented at the MTEC-08, India, March 2008

51. Mohsin M. Jamali, " Embedded Sensor Array Processing" Presented at the MTEC-08, India, March 2008

52. Mohsin M. Jamali and Benjamin J. Tran, "FPGA Based Sensory/Actuation Embedded System," Presented at the 2008 IEEE National Aerospace Conference (NAECON), Dayton, OH, July 2008

53. Mohsin Jamali, Joseph Downey, Joseph Tipping , Nathan Wilikins, Christopher R. Rehm, "Development of a FPGA-based High Speed FFT Processor for Wideband Direction of Arrival Applications," Presented at the 2009 IEEE Radar Conference.

54. Todd E. Schmuland, Mathew B. Longbrake, Peter E. Buxa, Mohsin M. Jamali," Automatic VHDL Generation Software Tool for Parameterized FPGA Based FFT Architectures," Presented at the 2010 IEEE National Aerospace Conference (NAECON), Dayton, OH, July 2010

55. Todd E. Schmuland, Mohsin M. Jamali, Mathew B. Longbrake, Peter E. Buxa, ," Parallel Implementation of the Wideband DOA Algorithm on the IBM Cell BE Processor," Presented at the 2010 IEEE Radar Conference

56. Mohsin M. Jamali, Ameen M. Jamali, " The Future of High Performance Real Time Computation and its Utilization in Diagnostic Medicine, Imaging, and Surgical Procedures," Poster presentation at the College of Medicine Research Day, The University of Toledo, March 27, 2010.

Reports:
Mohsin M. Jamali, 'Computational Requirement Analysis of Wide-band DOA algorithms" DSPH-10, Report submitted to U. S. Air Force Research Laboratory, Wright Patterson Air Force Base, Dayton, (Under contract administered by Mac-Aulay Brown, Dayton, OH), May 2007.

Externally funded grants:

1. Principal Investigator- Dr. A. R. Thorbjornsen
Co-Investigators, E.D. Smith, C.B. Kim, M.M. Jamali
" Engineering Research Equipment Grant for VLSI System Design Workstation and Dedicated Computer," NSF Grant No. ECS-8604663, $ 60,000, April 1986.

2. Principal Investigator- Dr. A. R. Thorbjornsen
Co-Investigators, E.D. Smith, C.B. Kim, M.M. Jamali
"Educational Use of the DARPA/NSF Silicon Brokerage Service (MOSIS)," Grant $ 20,600, October 1986.

3. Principal Investigator- Dr. S. C. Kwatra, Co-Investigator, M. M. Jamali,
"Digital Signal Processing Systems," Motorola Inc. $17450 including $2450 from UT matching funds, June 1988.

4. Principal Investigator- Dr. S. C. Kwatra, Co-Investigator, M. M. Jamali
"Digital Modem Development," NASA Grant NAG3-865, $60,380, 15 months, September 1988.

5. Principal Investigator- Dr. S. C. Kwatra, Co-Investigator, M. M. Jamali
"Development of Demultiplexing System," NASA grant NAG3-799, $ 48,646 one year, January 1989.

6. Principal Investigator- Dr. S. C. Kwatra, Co-Investigator, M. M. Jamali
Department of Elect. Engineering, The University of Toledo, "Signal Processing Worksystems," Comdisco Systems Inc. $29500 including $2400 from UT matching funds, Feb. 1989.

7. Principal Investigator- Dr. S. C. Kwatra, Co-Investigator, M. M. Jamali
"Digital Implementation of the Multicarrier demodulator. " NASA Grant NAG3-865, $61,324, 15 months, December 1989.

8. Principal Investigator- Dr. S. C. Kwatra, Co-Investigator, M. M. Jamali
"A Digitally Implemented Multicarrier demodulator. " NASA Grant NAG3-799, $55,857, 12 months, December 1990.

9. Principal Investigator- Dr. S. C. Kwatra, Co-Investigator, M. M. Jamali
"A Digitally Implemented Multicarrier demodulator. " NASA Grant NAG3-799, $45000

10. Principal Investigator- M. M. Jamali, Co-Investigator, S. C. Kwatra
"Development of Parallel Architectures for Sensor Array Processing Algorithms." Office of Naval Research (ONR) Grant N00014-91-J-1011, $ 93,750 December 1990.

11. Principal Investigator- M. M. Jamali, Co-Investigator, S. C. Kwatra
"Development of Parallel Architectures for Sensor Array Processing Algorithms." Office of Naval Research (ONR) Grant N00014-91-J-1011, $ 99,045, October 1991.

12. Principal Investigator- Dr. S. C. Kwatra, Co-Investigators, M. M. Jamali, A. G. Eldin
Department of Electrical Engineering, The University of Toledo, "A Digitally Implemented Multicarrier demodulator. " NASA Grant NAG3-799, $45000

13. Principal Investigator- M. M. Jamali, Co-Investigator- J. Klep
"Development System for Digital Systems Design ", Intel Corporation, $ 18,415, Feb. 1994.

14. Principal Investigator- Dr. S. C. Kwatra, Co-Investigators, M. M. Jamali, A. G. Eldin
"A Digitally Implemented Multicarrier demodulator. " NASA Grant NAG3-799, $55,383, December 1994.

15. Principal Investigator- M. M. Jamali
"PLC Programming Software," Allen-Bradley Inc.$ 15600.00 1994

16. Principal Investigator-M. M. Jamali
“Computer Integrated Manufacturing Software,” Microtek Controls. Total Sponsor $ 47,500. 1997

17. Principal Investigator-M. M. Jamali
"Multiplexing Network Development System ," Advanced Vehicle Technology. Total Sponsor $ 1350. 1998.

18. C0-Investigator-M. M. Jamali
"Intelligent Transportation System Research,", College of Engineering, U. of Toledo, $ 50,000, 1998

19. Principal Investigator- M. M. Jamali, Co-Investigator, Tom. Stuart
"Network Analysis Systems," Dearborn Groups. Total Sponsor $ 3495. January 2001.

20. Kohler International Faculty Travel Grant for Keynote Lecture on In-Vehicle Networks at the International Conference on Robotics, Vision, Information and Signal Processing, Penang, Malaysia July 20-22, 2005. Awarded $ 500.

21. Awarded US Air Force Summer Research Fellowship for work on advanced digital receiver at Air Force Research Laboratories Wright Patterson Air Force Base, Sensor Directorate. $ 23000, Summer 2005

22. Principal Investigator- M. M. Jamali
" Bandwidth Invariant Spatial Processing", AFRL/SN (Air Force Research Laboratories, Wright Patterson Air Force Base, Sensor Directorate)- Mac Aulay Brown (Dayton) Contract, May 2006, $ 25390.

23. Principal Investigator- M. M. Jamali
PLC Laboratory upgrade, OBOR instructional grant, $ 30,000, major redevelopment of laboratory equipment. July 2006

24. Lab Equipment for EECS 4170 and EECS 4150, OBOR instructional grant, $ 9,290 with Tom Stuart (PI). July 2006

25. US Air Force Summer Research Fellowship for work on FPGA based Embedded Systems at Air Force Research Laboratories Wright Patterson Air Force Base, Air Vehicle Directorate. $ 23000. Summer 2007

26. US Air Force Summer Research Fellowship for work on FPGA based Embedded Systems at Air Force Research Laboratories Wright Patterson Air Force Base, Air Vehicle Directorate. $ 23000. Summer 2007

27. Mohsin M. Jamali (PI), Gursel Serpen (Co-PI), Kami Makki (Co-PI), Lawrence Miller (Co-PI), "Enhancing efficiency in OMMC manufacturing process," Proposal submitted to OMMC, Toledo, September 2007, $ 267,199 (Pending)

28. Mohsin M. Jamali (PI), "Fast Fourier Transform FPGA/ASIC Architecture Simulator/Generator ", Funded by AFRL/DAGSI Program, April 2009. $ 83,363

29. M. M. Jamali (PI) Development of Radar/IR Based Embedded System, Proposal Submitted to DOE/BGSU Subcontract, May 2009, $ 46867, (Funded)

30. M. M. Jamali (PI) Development of Radar/IR/Sensor Array Based Embedded System, Proposal Submitted to DOE/BGSU Subcontract, May 2009, $ 489232, (Funded)

31. Mohsin M. Jamali (PI), "Fast Fourier Transform FPGA/ASIC Architecture Simulator/Generator, " Funded by AFRL/DAGSI Program, March 2010. $ 85, 872

Grant proposals submitted:

1. Principal Investigator, M. M. Jamali " Development of a Data Flow Computer and Its Knowledge Base System," NSF 84-53, $60,000, November 1984, two years.

2. Principal Investigator, M. M. Jamali " Development ofa Knowledge Base System for a General Purpose SignalProcessor," Grant No. NSF 83-57, ($51,171 including$16,702 from UT Matching funds), October 1985.

3. Principal Investigator, M. M. Jamali " Hardware Sim- ulation of a simultaneous Speaker Identification and Digit Recognition System," Faculty Research Award and Fellowship Program, University of Toledo, $7,400, November 1986.

4. Principal Investigator, M. M. Jamali " Hardware Simulation of a simultaneous Speaker Identificationand Digit Recognition System," Grant NSF 86-66, $59,918, January 1987.

5. Principal Investigator, " Development of Real-Time Hardware for Image Coding Using Vector Quantization," Ohio Board of Regents Research Challenge Program, $34,294, October 1987.

6. Principal Investigator- M. M. Jamali, Co-Investigator, S. C. Kwatra
"Development of computer architectures for mathematical modules used in sensor array processing Algorithms." Proposal submitted to ONR October 1991.

7. Principal Investigator- M. M. Jamali,
Co-Investigator, Drs. Smith, Eldin, Jovanovic and Kwatra.
"VLSI/ASIC Laboratory", Proposal submitted to NSF, November 1991.

8. Principal Investigator- M. M. Jamali, Co-Investigator, Dr. S. C. Kwatra.
"Development of Parallel Architectures for Mathematical Modules", Proposal submitted to NSF, March 1992.

9. Principal Investigator- M. M. Jamali, Co-Investigator, S. C. Kwatra
" Laboratory Enhancement rquest for VLSI Implementation of Sensor Array Processing Algorithms." Proposal submitted to ONR July 1992.

10. Principal Investigator- M. M. Jamali, Co-Investigator, S. C. Kwatra
"Development of Parallel Architectures for Sensor Array Processing Algorithms." Proposal submitted to ONR October 1992.

11. Principal Investigator- M. M. Jamali,
Co-Investigator, Drs. Smith, Eldin, Jovanovic and Kwatra.
"VLSI/ASIC Laboratory", Proposal submitted to NSF, November 1992.

12. Principal Investigator- M. M. Jamali, J. Klepp
"Intel development systems for digital systems designs laboratory", Proposal submitted to Intel, December 1992.

13. Principal Investigator- M. M. Jamali, Co-Investigator, S. C. Kwatra
"Development of Sonar system with real time computation of DOA estimation" Proposal submitted to ONR December 1992.

14. Principal Investigator- M. M. Jamali
"Automotive Electronics Engineering ", Submitted to NSF, November 1993.

15. Principal Investigator- M. M. Jamali
"Automotive Electronics Diagnostic System ", Submitted to OBOR, Feb. 1994.

16. Principal Investigator- M. M. Jamali
"Development of parallel real time architectures", submitted to NSF. 1994

17. Principal Investigator- M. M. Jamali
"Development of Integrated Automotive Electronic Systems," Submitted to URAFP. 1995.

18. Co- Investigator- M. M. Jamali
"Inroporation of adaptive control techniques into PLC technology", submitted to NSF. 1995.

19. Principal Investigator- M. M. Jamali
"Automotive Electronic research ", submitted to NSF. 1995.

20. Principal Investigator- M. M. Jamali
"Course development for automotive electronics ", submitted to NSF, 1995.

21. Principal Investigator- M. M. Jamali
“Development of Parallel Architectures”, submitted to FRAF, Feb. 1996.

22. Principal Investigator- M. M. Jamali
“Automotive Electronics Diagnostic System”, submitted to OBOR, Feb. 1996.

23. Principal Investigator- M. M. Jamali
"Computer Integrated Manufacturing Software," Submitted to Gray Matter Systems.

24. Principal Investigator- M. M. Jamali
Automotive Diagnostic Systems Study, Honda Corporation $ 25000 October 1998 (Not-funded)

25. Principal Investigator- M. M. Jamali
"Development of Diagnostic Software for Emission Control." Submitted to Environmental Protection Agency $ 249,981, June 1999.

26. Principal Investigator- M. M. Jamali, Development of In-Vehicle Network Test-bed proposal submitted to NSF, $ 296,815, May 2002

27. Principal Investigator- M. M. Jamali, Wired and Wireless Embedded Network Test-bed proposal submitted to DARPA/IXO, $ 414,235, May 2002

28. Abdul-Majeed Azad (PI), Mohsin M. Jamali (Co-PI) Design and Development of Microchemical Sensor Arrays with Nanofirillar Surface Features, Submitted to NSF $637,961, 3 years, Feb. 2004

29. Mohsin M. Jamali (PI)**, "**Interactive Teaching and Re-development of Advanced Computational Methods -EECS 6380" Summer Faculty Teaching Fellowship Program, Center for Teaching and Learning, The University of Toledo, March 2004 and March 2005.

30. Mohsin M. Jamali (PI) Programmable Logic Controller Laboratory Development , Submitted to NSF, $ 75000, 3 years, June 2004

31. Abdul-Majeed Azad (PI), Mohsin M. Jamali (Co-PI) "Development of a Miniaturized fast responding solid-state hydrogen safety sensor,:" Submitted to NASA, $ 584882, December 2004.
32. Abdul-Majeed Azad (PI), Mohsin M. Jamali (Co-PI) (Co-PI)- "Development of Potentiometric Microchemical sensors with nanofeatured surfaces,:" Submitted to NSF, $ 663,778, February 2005

33. Mohsin M. Jamali (PI)
Development of FPGA or DSP based hardware for digital receiver for UAV applications – White paper submitted to U.S. Army AATD, AMSRD-AMR-AA-I (Allen Walker), Fort Eu stis, VA, November 2005

34. J. Kim (PI) Co-PIs: M. Alam, M. M. Jamali, and W. Li
"Advanced Communication and Networking (CAN)," Submitted to University of Toledo, for the identification of a research area for new enhancement, November 2005.

35. Mohsin M. Jamali (PI), Submitted proposal to Summer Research Fellowship to Air Force Office of Reseach, November 2005.

36. Mohsin M. Jamali (PI) Submitted proposal to Summer Research Fellowship to Air Vehicle Directorate, AFRL, Wright Patterson Air Force Base, November 2005.

37. Digital Receiver Development – Research Summary submitted to Ohio Third Frontier program. May 2006.

38. Mohsin M. Jamali (PI), Comparative study of digital beamforming algorithms and development of parallel architectures submitted to AFRL/DAGSI Program, Dayton, OH, January 2007. $ 55950, Declined

39. Mohsin M. Jamali (PI), "Spatial audio displays for distributed team collaboration", submitted to AFRL/DAGSI Program, January 2008. $ 40084

40. Mohsin M. Jamali (PI), "Implementation of Radar Signal Processing Algorithms on IBM Cell Processor", submitted to AFRL/DAGSI Program, January 2008. $ 40084

41. Mohsin M. Jamali (PI), "Development of An Integrated Location and Physiology Monitoring and Processing System", submitted to AFRL/DAGSI Program, January 2008. $ 40084

42. Mohsin M. Jamali (PI), FPGA Based Adaptive Control Embedded System for Flight Surface Control proposal submitted to AFRL/RBCC- Wright Patterson Air Force Base, August 2008, $ 17000.

43. Mohsin M. Jamali (PI), "Multicore Based Wideband Digital Beamforming Architecture", submitted to AFRL/DAGSI Program, January 2009. $ 48,510

44. Mohsin M. Jamali (PI), "Heterogeneous Multi-core High Performance Computing Test-bed for Real-Time Sensor Array Signal Processing," Submitted to the Deparment of Energy, Office of Advanced Scientific Computing Research, March 2010, $ 639,563.

Professional societies -

Institute of Electrical and Electronics Engineers, Senior Member
Society of Automotive Engineers. Member
Technical committee member(IEEE Society of Circuits and Systems)
(a). Digital signal processing. (b). VLSI Applications
Member of SAE Vehicle Multiplexing Standard Development Committee
Member of SAE Vehicle Diagnostics Standard Development Committee
Vice-President Computer Science & Mathematics Section, Ohio Academy of Science. 1987
Chairman - SAE Vincent Bendix Automotive Electronics Engineering Award Committee 2002-Present
Chairman- SAE Vehicle Muliplexing Standard Development Sub-Committee for review of In-Vehicle Network Security, 2004.
Advisor for local IEEE Student Chapter, 2005-2007
Member at Large local IEEE Chapter, 2008-Present

Papers reviewed

Have reviewed papers for
IEEE Transactions of Acoustics, Speech and Signal Processing.

IEEE Computer magazine.
Midwest Symposium on Circuits and Systems.
International Journal of Computer Aided VLSI Design
IEEE Transactions of Signal Processing.
International Symposium for Circuits and Systems.
Journal of VLSI Signal Processing
Society of Automotive Engineers
Society of Automotive Engineers, In-Vehicle Networks, 1998-Present

New courses developed and taught:
Computer Architecture & Parallel Processing
Multiprocessor Architecture
Special Purpose Computer Architectures
Special Topics on Computer Arithmetic
Digital Logic Laboratory
Digital VLSI Design (VLSI Team).
Special Topics on the Digital Signal Processing Hardware
Programmable Logic Controllers- Covers process control using PLCs/SLCs 1994
Automotive Electronics-Covers engine control, in-vehicle networks, 1994
Digital Design- Covers VHDL and ASIC design. 1998
Real Time Embedded Systems (1998)
Array Signal Processing (Fall 2006, 2007)
Advance Digital Signal Processing

New Laboratories Developed
Digital Logic Laboratory (1987)
Microprocessor Systems Design Laboratory (1992)
Programmable Logic Controller Based System Laboratory (1994)
Real Time Embedded Systems Laboratory (1998)
Digital Design (VHDL) Laboratory (1998)

Courses taught:
Digital Systems Design
Digital Computer Design
Mini/Micro Computers & Applications.
Systems Analysis.
Microcomputer Systems I
Digital Design
Computer Organization and Assembly Language
Assembly Language
Electric Circuits
Signal Analysis
Advanced Computational Methods using MATLAB
Digital Signal Processing
Advance Computer Architecture

Graduate students supervision:

Doctoral
K. Dezhgosha, "Development of a Real Time Hardware for Image Coding Algorithms," 1989

Doctoral (Foreign Examiner)
1. Zia Ahmad Abbasi, "Discrete Coded Waveforms for Signal Processing in Radar," Department of Electronics Engineering, Aligarh Muslim University, 1997.

2. Ateeq Ahmad Khan," Modelling and Characterization of IC Fabrication Processes," Department of Electronics Engineering, Aligarh Muslim University, 1999.

3. Shamimul Qamar, " Capacity and Quality of Service for CDMA Communication Network with Diversity & Handoff", Indian Institute of Technology (IIT) Roorkee, 2007

4. Mahesh Chandra," Speech Recognition Using Wavelet Transform," Department of Electronics Engineering, Aligarh Muslim University, India, 2008.

5. Ajai Kumar Jain," Performance Trade Off in Quality of Service of High Speed Networks," Department of Instrumentation and Control Engineering, National Institute of Technology, Jalandhar, India, 2008.

6. Mohammad Ahmad Ansari, " Context Based Image Compression with Transform Coding", Indian Institute of Technology (IIT) Roorkee, 2009

7. Manoj Kumar, "Evaluation of Quality of Service Parameters and Performance of Wireless Ad Hoc Networks", Indian Institute of Technology (IIT) Roorkee, 2010

Current Ph. D. Students

Majid Wadood, "Development of GPU Based Architectures for DOA Algorithms," in progress
Todd Schmuland Working with FPGA Simulator
Kamel Fahmy, Development of Adaptive Flight Control Systems, in progress

Current MS Students

Xiaoru Wang,"FPGA Based Embedded Hardware for Discrete Self Tuning Regulator for Flight Control Systems," in progress

Lai Wei,"FPGA Based Embedded Hardware for Discrete Model Reference Adaptive Flight Control System," in progress

Priyadarsini Komatineni, “Development of Radar/IR Real Time Remote Sensor Systems,” in progress

Selin Bastas,”Development of Microphone Based Array DOA/Beamforming Based Sound Recognition System,” in progress

Harsha Avinoori developing bird radar in progress

Nishatha Nagarajan working on NEXRAD/Marine Radar in progress

Vamshi Gummala working on MIMO/IR based systems in progress

Masters Thesis

1. M. M. Hussain, "A Signal Processing Cell Architecture," 1987.
2. P. Bumrungthum, "A Systolic Array Architecture for Linear Predictive Coding," 1987.
3. Raja Tabar "Wideband Sensor Array Processing Architecture using Time Domain Approach" December 1993.
4. P. Mohanty "Systolic Architecture for Clustering Algorithm" 1993.
5. R. Suria "Wideband Sensor Array Processor Architecture using Frequency Domain Architecture" August 1994.
6. Clark Carty "An Architecture for Interpolator, 1994.
7. Yikai Linag "Multiprocessor Architecture for QR Algorithm" 1995.
8. Doug Bitter " A VLSI design for pattern recognition algorithms using FPGAs." 1999.
9. Mark Brown- Multiple target detection and tracking in three dimensional medium, 2001
10. Ahmad Rizvi – Algorithms and Architectures for Subspace Frequency Estimation- July 2004
11. Javed Rizvi – FPGA Implementation of MUSIC algorithm, April 2004
12. Felipe Arredondo- Development of FPGA based architecture for DOA algorithms in progress.
13. Abdel Affo- Development of DSP based architecture for DOA algorithms, August 2006
14. Todd Schmuland- IBM Cell Processor Based System for Wideband DOA Algorithms, 2010

MS Projects

1. Amitava Bhattacharyya, “Exploring Security Systems for ITS/Vehicle Communications” 1999.
2. Saranagati Chatterjee, “ Exploring Bridges and Gateways”, 1999.
3. Huan Gao, “Exploring Smart and Java Cards”, 1999.
4. Dinish Sinnasamy, “ Security schemes for In-Vehicle Networks”, 1999.
5. Satish Ayyaswami, “Investigation of Control Algorithms for Anti Lock Brake System” 1999.
6. Rizwan Husain, “Gateway Design” 1999.
7. Mubeen Ahmad, “Reconfigurable computing” 1999.
8. Sudheer Averineni, “Reconfigurable Computing for Vector Quantization”, 2000.
9. Raghuraman Ganesan, “Reconfigurable Sensor Array Processing Hardware”, 2000.
10. Joseph Deeb, “Bluetooth Wireless Interface Node Design”, 2000.
11. Abhuday Pradhan, “Just in Time Power Aware Architectures”, 2000.
12. Prahlad Goggi, “Development of Multicast Protocols Part I”, 2000.
13. Harshal Pimpalkhute, “Development of Multicast Protocols Part II”, 2000.

14. W. Hoyt, “Design of a CAN to IEEE 802.11 Wireless LAN Node,” 2000.
15. S. Shetty,”Simulation of Multicast Protocols”2000
16. C. Sheh,”Reconfigurable FPGAs for Sensor Array Processing Algorithms” 2001.
17. W. Bush,”Design of Gateways/Bridges for In-Vehicle Networks,” 2001.
18. Deepa Sarathy, Analysis of Macrodiversity Scheme for 3G Wireless Systems and VHDL Implementation of CDMA Matched Filter, December 2001.
19. S. Janagama,”FPGA Implementation of Cellular Phone Location Algorithm,” 2001
20. Charlie Suriyakamol,”Development of a Bluetooth Node for In-Vehicle Network,” 2001
21. Nicolas Hadjisavvas – Study of network routing algorithms, 2004
22. Yongquan Chai – Development and simulation of engine control algorithm, 2004
23. Ivon Popov –Development of adaptive cruise control algorithm, in progress

Co-Advisor for the following MS students
1. B. D. Goel, " A Design of Systolic Architecture for Real Time Vec. Quantization in RNS," 1988
2. A. Thanawala, "A Design of Digital Demultipexor," 1989.
3. P. Fernandes, "A Pipelined Transmultiplexor Architecture" 1990.
4. L. P. Eugene "A Parallel Architecture for a Digital Demodulator" 1990.
5. C. Gottschak "An ASIC Design of Transmultiplexer Architecture," 1992.
6. M. Bexten " ASIC design for a Multicarrier Demodulator using Standard Cell Approach," 1992.
7. Dave Wagner "A Single Chip QPSK Demodulator" 1992.
8. C. S. Lee "ASIC Design of Data Stage Module for Digital Transmultiplexor" 1992.
9. A. L. Enriquez, " Implementation of A Flexible Controller for Robot Manipulators," 1992.
10. Dinraj Shetty, A VLSI design of the transmultiplexor.1995
11. Subhash Chintameni, VLSI design of a multicarrier demodulator. 1995
12. M. Maruthapan, A Design of ROM Generator, 1995.
13. M. Pakkurti, A CAD system for the memory.
14. Motheeswara Salla- Design of a Built-In- Self Test Scheme for Xilinx Virtex FPGA May 2002
15. Dinesh Nemade- Testing Embedded RAM Modules in SRAM-based FPGAs 2002
16. Aditya Srinivas Ravinuthala- A Built-IN- Self Test Scheme for Testing Embedded Memories in System-on-Chips July 28, 2004

MS Independent Study

Terrell Williams- Digital Design using VHDL
Chiang Chung Sheh- Synthesis Tools for FPGAs
Amit Deshmukh -Network Security
Sachin Shetty -Investigation of Multicast Protocols for wireless networks, 2001
Charlie Suriyakamol - Comparative Study of various protocols
Chiang Chung Sheh- Synthesis Tools for FPGA May 2001
Mubeen Ahmed- Internet Reconfigurable Computing, 2000

Work with undergraduate students (Partial List)
Chiang Chung Sheh- Systems on Chips BS Independent Study, 1999.
K.Low, C. Sheh, T. Strimpel- Development of SDLC language for Radar Applicaitons
Molham Bali- Development of reconfigurable hardware for DOA applications.

Edward MacCanon, Yong Wee Tay, James Roberts- Design of an In-Vehicle Node with CAN and IEEE 1394b Network Interface December 2000

Senior Design Projects
K. Barth, R. Getter-Senior Design Project on development of MP3 hardware/software system 1999.
Chiang Chung Sheh, Kok Hwe Low and Todd Strimpel- Electronic System Design Using System Level Design Language December 1999.
Joe Schilens, Andy Talicska, Jason Crispen- Automotive Rain Sensor & Window Control 2003
Shawn Tiell, Andy Marckel-Angle Head Grinder December 2003
Curtis Unik and Ben Wierwille- Adaptive Cruise Control, June 2004
Stephen Steen, Cost Reduced Fault Code Interface, April 2006

Fall 2004
Josh Nixon, Brad Waybright, Adam Huelskamp and Josh Ross- Drive-by-wire model car, Fall 2004
Mustapha Barakat, Sheetal Shah, Benjamin Tran, Michael Wesgate- Automatic Coin Dispenser,
Spring 2005

- Tim Bensor, Josh Kessler, James Jones, Temperature-Controlled, Secure Beverage Management System
- Tom Garnes, Aaron Thomas- VHDL Implemented MUSIC Algorithm
- Andy Moebius, Brian Nally, Matt Sortor, Wireless Communication Between TI Calculators
- Rachna Patel, Libbe Speck, FPGA Optical Feedback with Human Interface

Fall 2005
4- Senior Design Projects

Spring 2006
Stephen Steen, Cost Reduced Fault Code Interface

Fall 2007
Brandon Burrow, Aron Friszman, Kevin Grady, James O'Neill, Todd Ostendorf, Casey Theman- PLC Food Processing System
Spring 2008
Joseph Downey and Joseph Tipping, "Development of a FPGA-based High Speed FFT Processor for Wideband Direction of Arrival Applications.
Fall 2009
Ben Swift, James Velleroy, John Wagner,"Data Acquistion for Avian Observation near Wind Turbines,"

Served on Committees:
Under-graduate Curriculum Committee 84-86, 2008-Present
Graduate Curriculum Committee 1986-1987. 2007-Present
Chairman of Computer Curriculum Sub-Committee 1985-1995
University Microcomputer Advisory Committee 1984-1985
College Computer Advisory Committee
College System Committee

Library Representative
Awards Committee
Chairman, Logic and Computers Sub-Curriculum Committee.
Computer Systems Focus Group
Control and Manufacturing Focus Froup.
Department Personnel Committee 1997-2000, 2001-2006
Chairman, Department Personnel Committee, 1998-2000, 2003-2006
Graduate Director 01/2000-2001
University Research Task Force 2000-2001
Member EECS Chair Search Committee 2000-2001, 2005-2007
Chairman Faculty Search Committee 2000, 2002-2003, 2007-2008
Chair ABET Assessment sub-committee Outcome # 6, 2003-Present
Member CSE Curriculum Committee, 2000-Present
Member CSE retention committee, 2003-2004
Member College Diversity Committee, 2003-2004, 2009
Member Engineering College Academic Personnel Committee, 2009-2012
Member-at-Large, IEEE Toledo Section, 2009-2012
Focus Group Leader, Communication and Signal Processing (CSP) 2007-Present

Continuing education seminars/workshops(attended)

Robotics and its Applications , University of Michigan, Ann Arbor, 1985
Computer Vision and Image Processing, University of Michigan, Ann Arbor, 1986
Attended IEEE Satellite seminars on Applications of Artificial Intelligence 02/26/86
Participated in the Reliability Engineering Design Workshop at the Wright Patterson Air Force Base during June 15, 1987 to July 10, 1987.
Attended NSF VLSI Educational Conference 1991.
Attended IEEE workshop on Computer Arithmetic 1993.
Digital Signal Processing Hardware Design , NSF Workshop, Darthmouth, MA, July 1998.
RS Logic Workshop, Rockwell Software, Cleveland, Ohio, December 1998.
FLEXRay Workshop, FLEXRay Consortioum, Dearborn, MI, March 2003.
Tutorial on Sensor Networks, ICASP 2004, Montreal, April 2004
Tutorial on Space Time Adaptive Processing, IEEE 2006 Radar Conference in Stoney Point, NY, April 2006
XILINX DSP design using FPGA course (2 days) May, 2006
XILINX FPGA design course (2 days) June, 2006