7 Combinational Logic Design (SSN Decoder)

In Part I, this experiment challenges the student to design a unique logic circuit, and construct it via gate selections from a limited set of 74XX gates. Circuit inputs are **BCD** encoded. In Part II, this experiment has the student implement the Part I design using VHDL and programmable logic. *Part I has Altera Maxplus prelab requirements!!!*

I. Design Description

You are to design a circuit which has four inputs, A, B, C, and D, and four outputs, F_1, F_2, F_3, and F_4. The four inputs represent the binary numbers 0 through 15 with A the MSB and D the LSB. The three output functions are defined below:

A. F_1 is to be a logic 1 if the input is equal to one of the first three numbers of your social security number. Otherwise, F_1 is to be a logic 0.

B. F_2 is to be a logic 1 if the input is equal to one of the middle two numbers of your social security number. Otherwise, F_2 is to be a logic 0.

C. F_3 is to be a logic 1 if the input is equal to one of the remaining four numbers of your social security number. Otherwise, F_3 is to be a logic 0.

D. F_4 is to be a logic 1 if the input is equal to any one of the numbers in your social security number. Otherwise, F_4 is to be a logic 0.

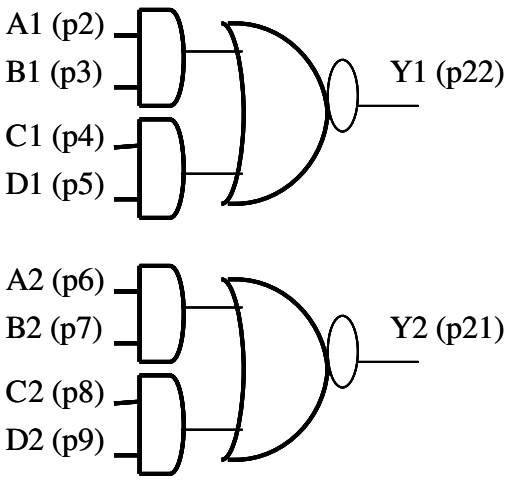
II. Implementation (Part I, First Week)

Design the logic circuit so that it can be implemented using only one of each of the following chips: 7400, 7402, 7404, 7408, 7410, 7432, 7451, and 7486. Draw the logic diagram for your design using only the chips mentioned above.
The following link:

http://www.ece.msstate.edu/~reese/EE3714/multfunc/index.htm

contains additional discussion about the 74XX implementation of this lab including a sample solution.

Your parts kit does not contain a 7451. The TA will program one of your PLDs with the 7451 function; the pinout is shown below.



III. Testing (Part I)

Connect your design from Part II using DS-1 for input A, DS-2 for input B, DS-3 for input C, DS-4 for input D, DI-1 for F_1 , DI-2 for F_2, DI-3 for F_3, and DI-4 for F_4. Have the instructor verify the operation of your circuit. It is allowed to get final checkoff of your 74XX implementation in the 2nd week of this lab.

IV. Implementation (Part II, Second Week)

You are to implement your SSN decoder design using VHDL and a 22V10 Programmable Logic Device. The following link:

- http://www.ece.msstate.edu/~reese/EE3714/vhdl2pld/index.htm

contains information on how to implement boolean equations using VHDL and has a sample solution. In order to compile your VHDL, and produce a JEDEC file, you must follow this link:

- http://www.ece.msstate.edu/~reese/EE3714/webcad/ssncomblab.htm

V. Testing (Part II)

Have the TA program your PLD for you. You must have a printout of the successful VHLD compilation/simulation when you enter the lab the 2nd week, or the TA will no program your PLD. Connect up your 22V10 PLD and verify its correct functionality for the TA.

VI. Report

You are to write ONE report that includes both parts of this lab assignment. Include in your report the step-by-step procedure used to design and build the required 74XX logic circuit. This must include the development of the functional expressions, their manipulation to meet limited logic availability, plus the implementation and test approach. Also include your VHDL code, and a printout of the WWW page that contains the results of the VHDL compilation and simulation.

Each PART of this lab counts as a normal lab grade (each 100 points).

PreLab Data Sheet

1. Part I. (Due at beginning of lab the FIRST WEEK). You MUST have the schematics and F1,F2,F3,F4 K-MAPS for your 74XX implementation ready for TA checkoff at the beginning of the lab period in the FIRST WEEK. Since each solution is unique, the TA can only check that you have made a good faith effort at getting a correct solution. You must have a minimized SOP form for F4 from a K-map even if you are implementing F4 as F1 + F2 + F3.

The WWW page has a ZIP archive that contains an Altera Maxplus Schematic + Waveform files for the sample solution discussed in the notes (SSN:458 70 2198). Look as this schematic/simulation and be sure you understand how it works. Feel free to use this as starting point for your own solution. You must demo the schematic/simulation for your solution via screenshots or laptop PC to the TA at the beginning of the lab period.

TA CHECKOFF (KMAPS) _____

TA CHECKOFF (MAXPLUS) _____

2. Part II (Due at beginning of lab the SECOND WEEK). You must have a printout of your VHDL code plus a printout of your completed VHDL simulation/JEDEC report page. You must demonstrate to the the TA that the VHDL simulation results matches the expected results for your SSN. If your results are incorrect, then you will not be allowed to use the PLD programmer. The EQUATIONS used in your VHDL code for F1,F2,F3,F4 **must be the minimized SOP equations** from your K-maps.

TA CHECKOFF (VHDL) _____

Lab Data Sheet

1. (Part I) Verify the functionality of F1, F2, F3, F4 to the TA. You have a two week period to get this lab, and the next lab (VHDL implementation of the SSN Decoder) working. You can get both checked off in the 2nd week if you desire; however, DO NOT WAIT until the 2nd week to start working on both labs or you will not finish.

Function F1: TA Checkoff _____

Function F2: TA Checkoff _____

Function F3: TA Checkoff _____

Function F4: TA Checkoff _____

2. (Part II) Verify the functionality of F1, F2, F3, F4 implemented via the 22V10 to the TA..

Function F1: TA Checkoff _____

Function F2: TA Checkoff _____

Function F3: TA Checkoff _____

Function F4: TA Checkoff _____