ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

Designers Manual for SMFL Standard CMOS

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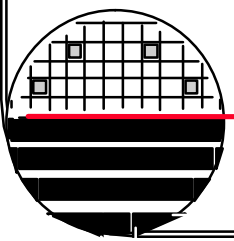
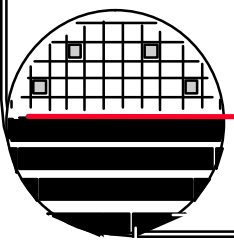
OUTLINE



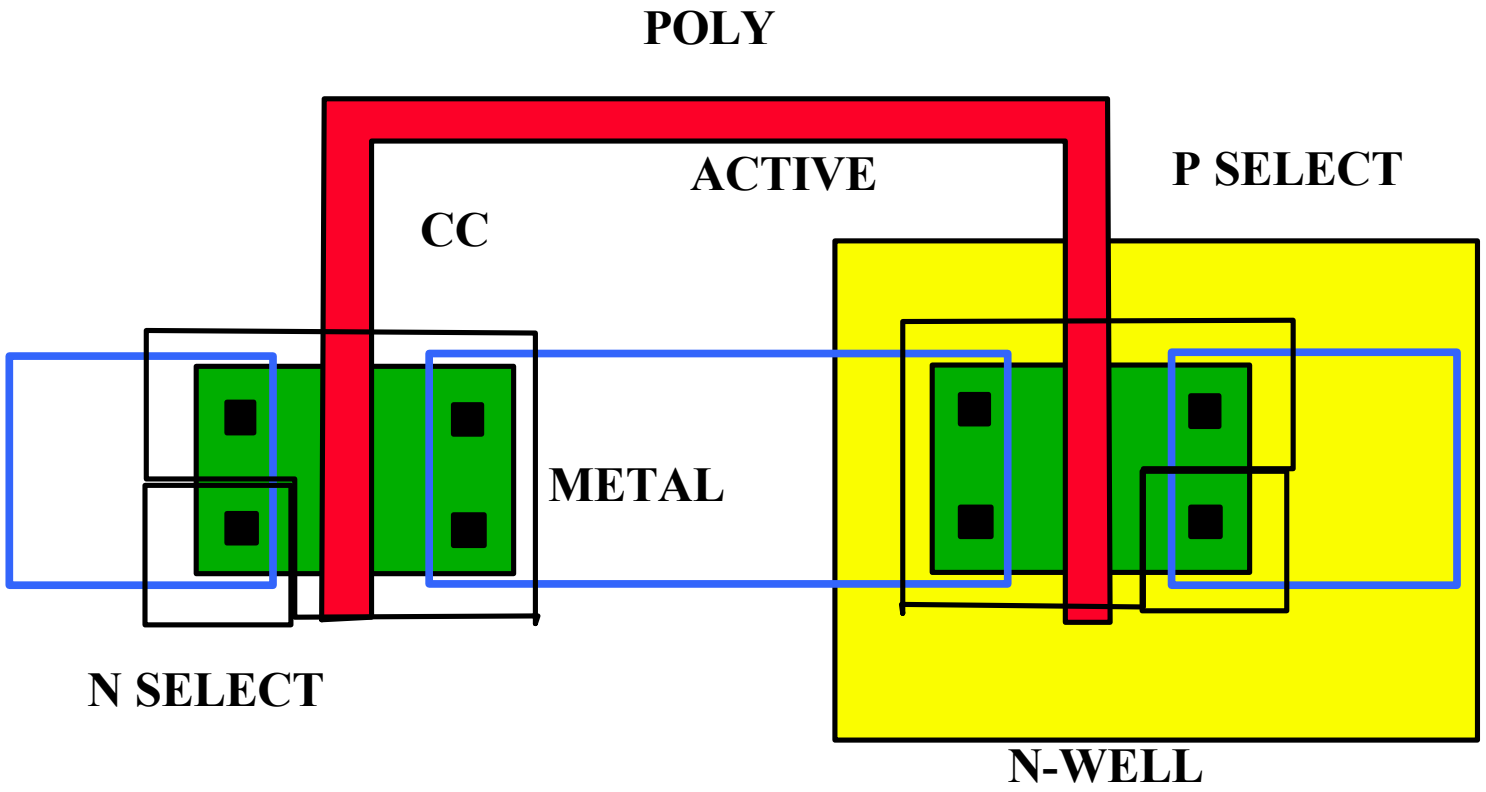
INTRODUCTION

RIT is supporting three different CMOS process technologies. The older p-well CMOS has been phased out. The SMFL-CMOS process is used for standard 5 Volt Digital and Analog integrated circuits. This is the technology of choice for teaching circuit design and fabricating CMOS circuits at RIT. The SUB-CMOS and ADV-CMOS processes are intended to introduce our students to process technology that is close to industry state-of-the-art. These processes are used to build test structures and develop new process technologies at RIT.

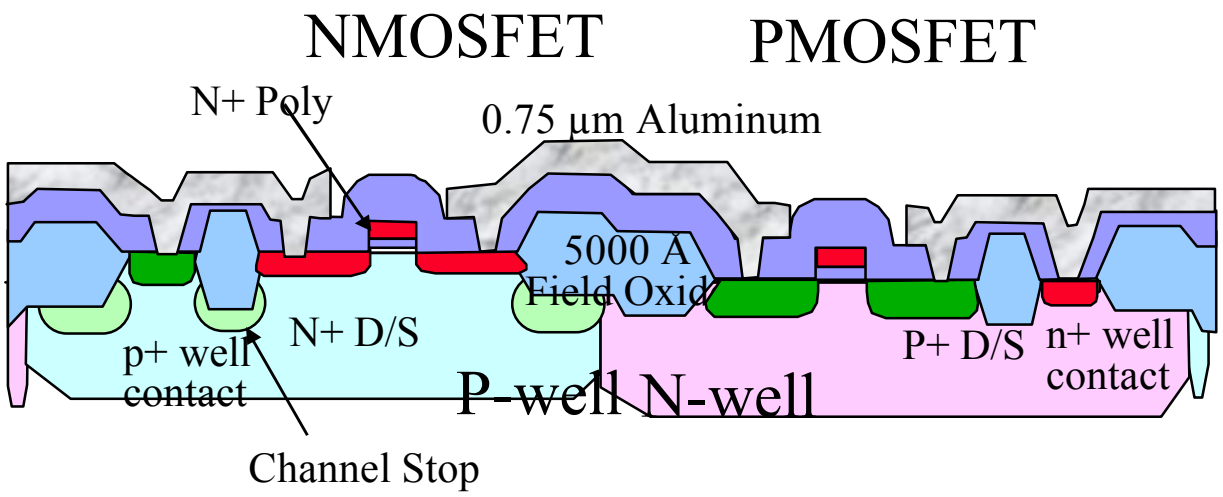
RIT p-well CMOS	$\lambda = 4\ \mu m$	Lmin = 8 µm
RIT SMFL-CMOS	$\lambda = 1\ \mu m$	Lmin = 2 µm
RIT Subµ-CMOS	$\lambda = 0.5\ \mu m$	Lmin = 1.0 µm
RIT Advanced-CMOS	$\lambda = 0.25\ \mu m$	Lmin = 0.5 µm

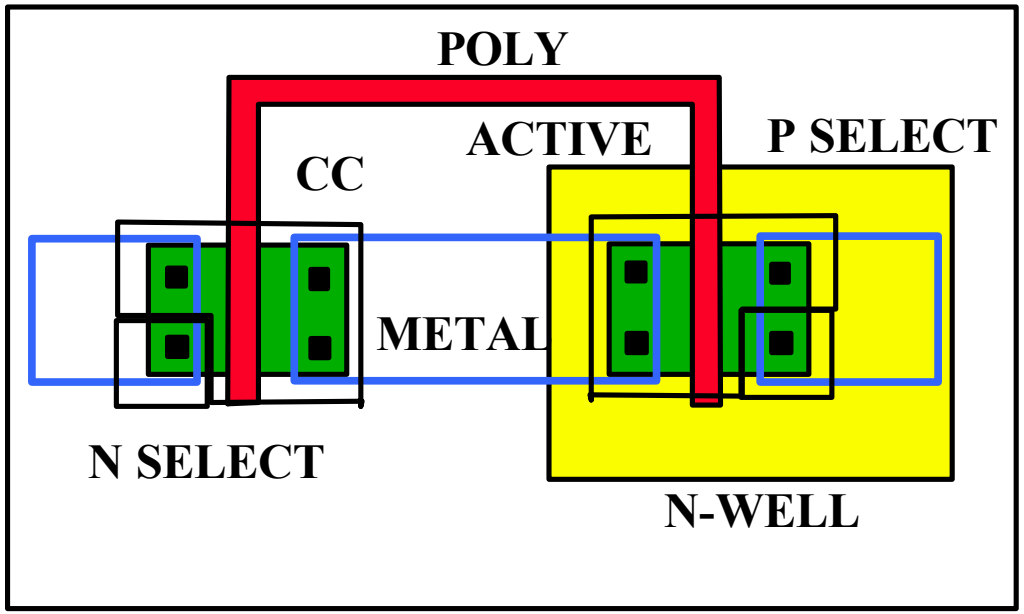


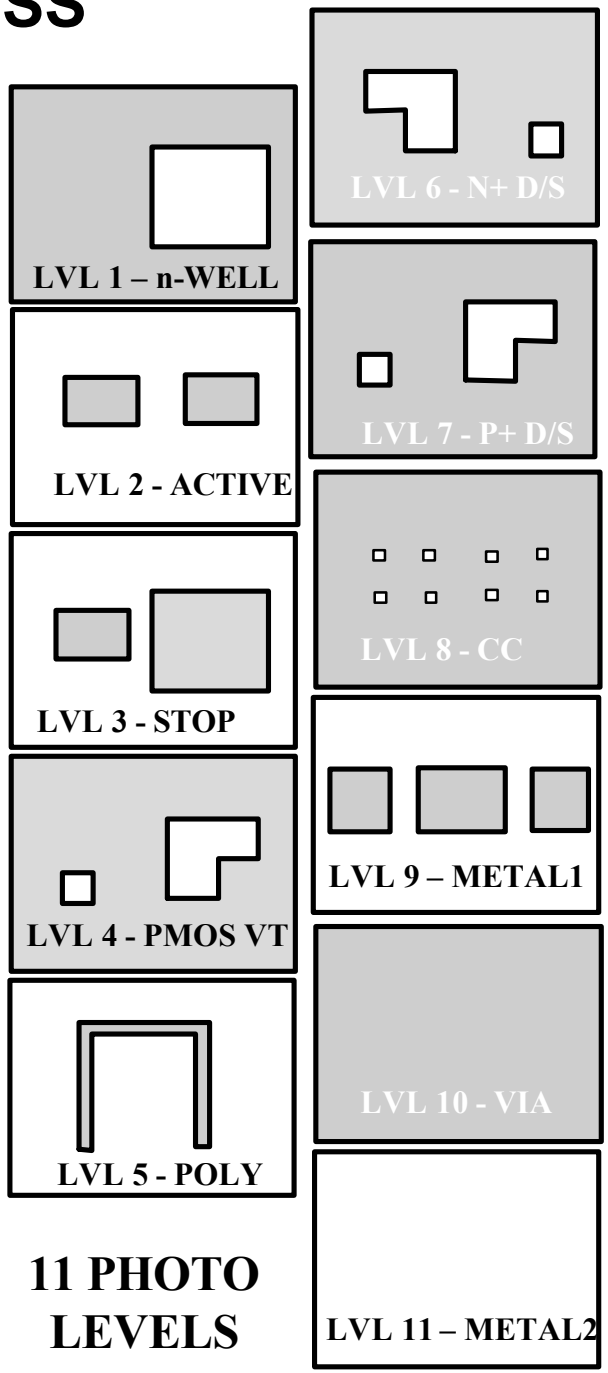
DESIGN LAYER NAMES



RIT SMFL-CMOS PROCESS



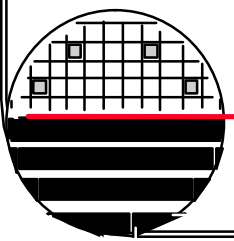




SMFL-CMOS PROCESS

SMFL-CMOS, twin-well CMOS process, two level Metal

1. ID01 scribe
2. DE01 4 pt probe
3. CL01
4. OX05--- pad oxide
5. CV02- 1500 Å
6. PH03 –1- n well,
7. ET29 nitride etch
8. IM01 – n-well
9. ET07 strip resist
10. CL01
11. OX04 – well oxide
12. ET19 strip nitride
13. IM01 – p-well
14. OX06 – well drive
15. ET06 etch all oxide
16. OX05 – pad oxide
17. CV02 - 1500 Å
18. PH03 – 2 - Active
19. ET29 etch nitride
20. ET07 strip resist
21. PH03 – 3 - p-well stop
22. IM01- stop
23. ET07 strip resist
24. CL01
25. OX04 - field
26. ET19 strip nitride
27. ET06 etch pad oxide
28. OX04 - Kooi
29. PH03 – 4 - PMOS Vt Adjust
30. IM01 - Vt
31. ET07 strip resisit
32. ET06 etch Kooi Oxide
33. CL01
34. OX06 - gate
35. CV01 dep poply
36. DI04 - dope poly Si
37. ET06 etch spin on dopant
38. DE01 four pt probe
39. PH03 – 5 – poly, open
40. ET08 poly etch
41. ET07 strip resist
42. PH03 – 6 - N+D/S
43. IM01 – N+D/S
44. ET07 strip resist
45. PH03 – 7 P+ D/S
46. IM01 – P+ D/S
47. ET07 strip resist
48. CL01
49. OX08 – poly reox
50. CV03 – LTO
51. OX08 DS anneal
52. PH03 – 8 CC
53. ET10 etch CC
54. ET07 strip resist
55. CL01
56. ME01 Dep Metal1
57. PH03 -9- metal1
58. ET05 etch metal
59. ET07 strip resist
60. CV03 – LTO
61. PH03 – 10 VIA
62. ET10 etch VIA
63. ET07 strip resist
64. CL01
65. ME01 Dep Metal2
66. PH03 -11- metal2
67. ET05 etch metal2
68. ET07 strip resist
69. SI01 SINTER
70. TE01 Test 1 van der pauw
71. TE02 Test 2 transistors
72. TE03 Test 3 inverters
73. TE04 Test 4 Vt wafer map



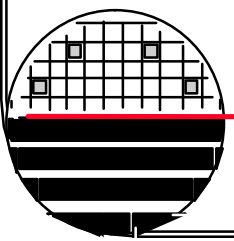
PROCESS PARAMETERS

Poly Thickness = 0.35 μm
Oxide Thickness Between Poly and Metal One = 0.5 μm
Metal One Thickness = 0.75 μm
Oxide Thickness Between Metal One and Metal Two = 0.5 μm
Metal Two Thickness = 1.0 μm

Capacitance ~ 6.9 nF/cm^2

Maximum Current Density ~ 1 $Amp/\mu m^2$

Minimum Width ~ 3 Lambda

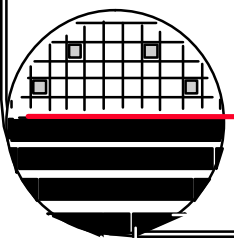


MOSIS LAMBDA BASED DESIGN RULES

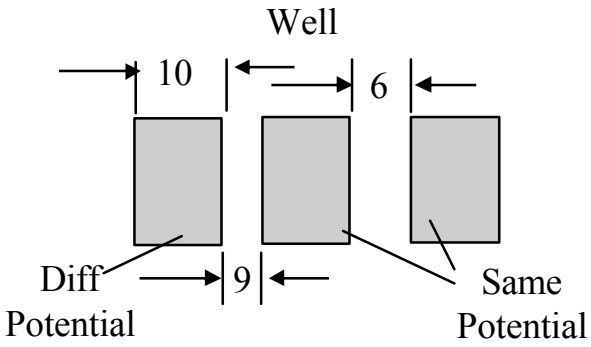
The design rules may change from foundry to foundry or for different technologies. So to make the design rules generic the sizes, separations and overlap are given in terms of numbers of lambda (λ). The actual size is found by multiplying the number by the value for lambda.

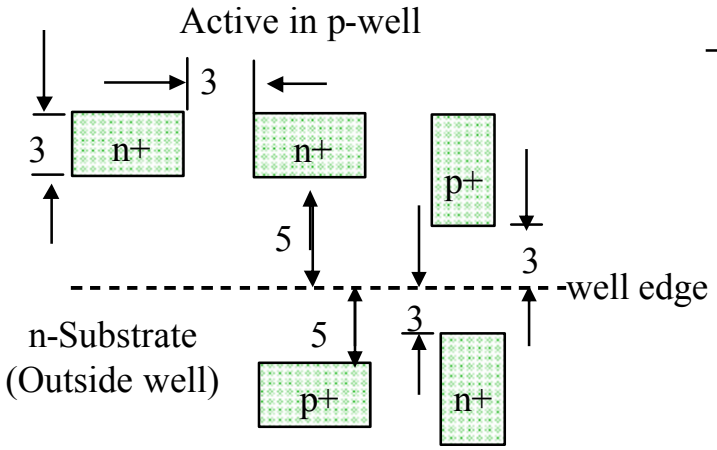
For example:

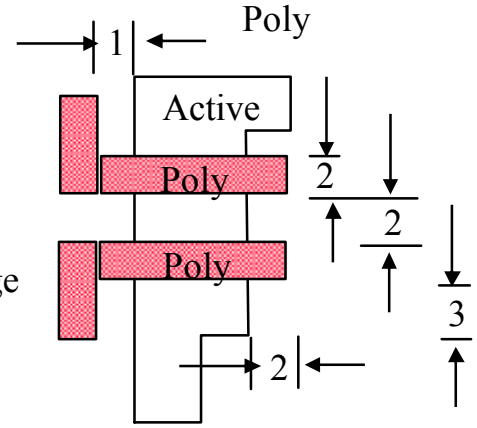
RIT PMOS process λ = 10 μm and minimum metal width is 3 λ so that gives a minimum metal width of 30 μm. The RIT CMOS process (single well) has λ = 4 μm and the minimum metal width is also 3 λ so minimum metal is 12 μm but if we send our CMOS designs out to industry λ might be 0.8 μm so the minimum metal of 3 λ corresponds to 2.4 μm. In all cases the design rule is the minimum metal width = 3 λ

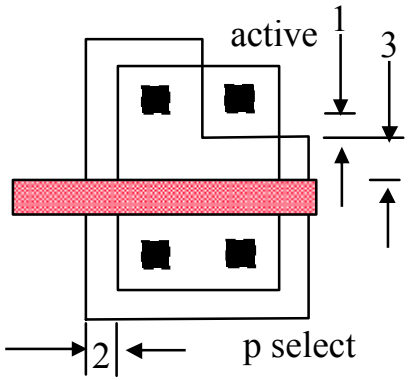


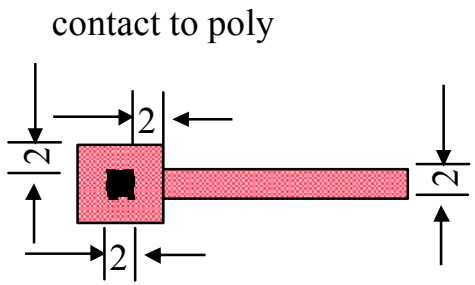
MOSIS LAMBDA BASED DESIGN RULES

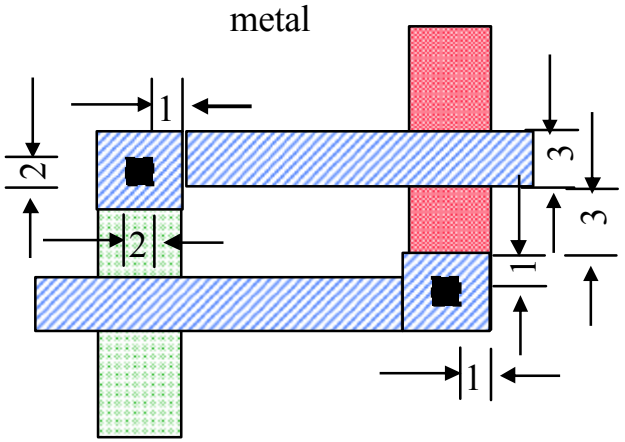






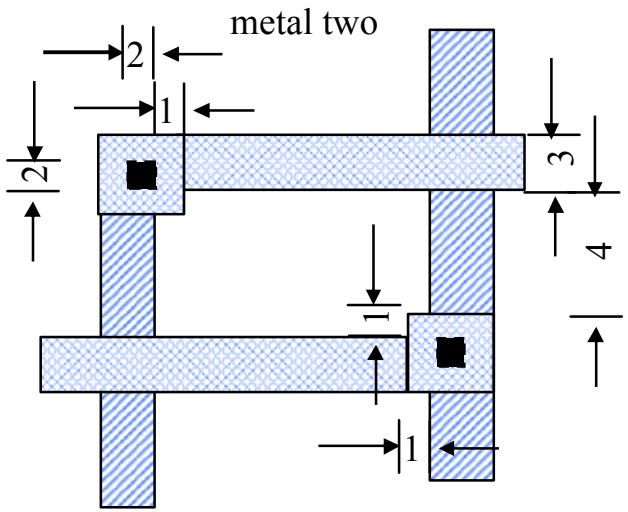






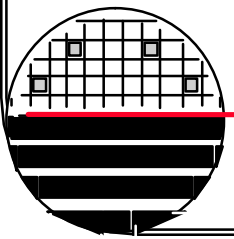
If λ = 4 μm then contact is 8 μm x 8 μm

MOSIS LAMBDA BASED DESIGN RULES



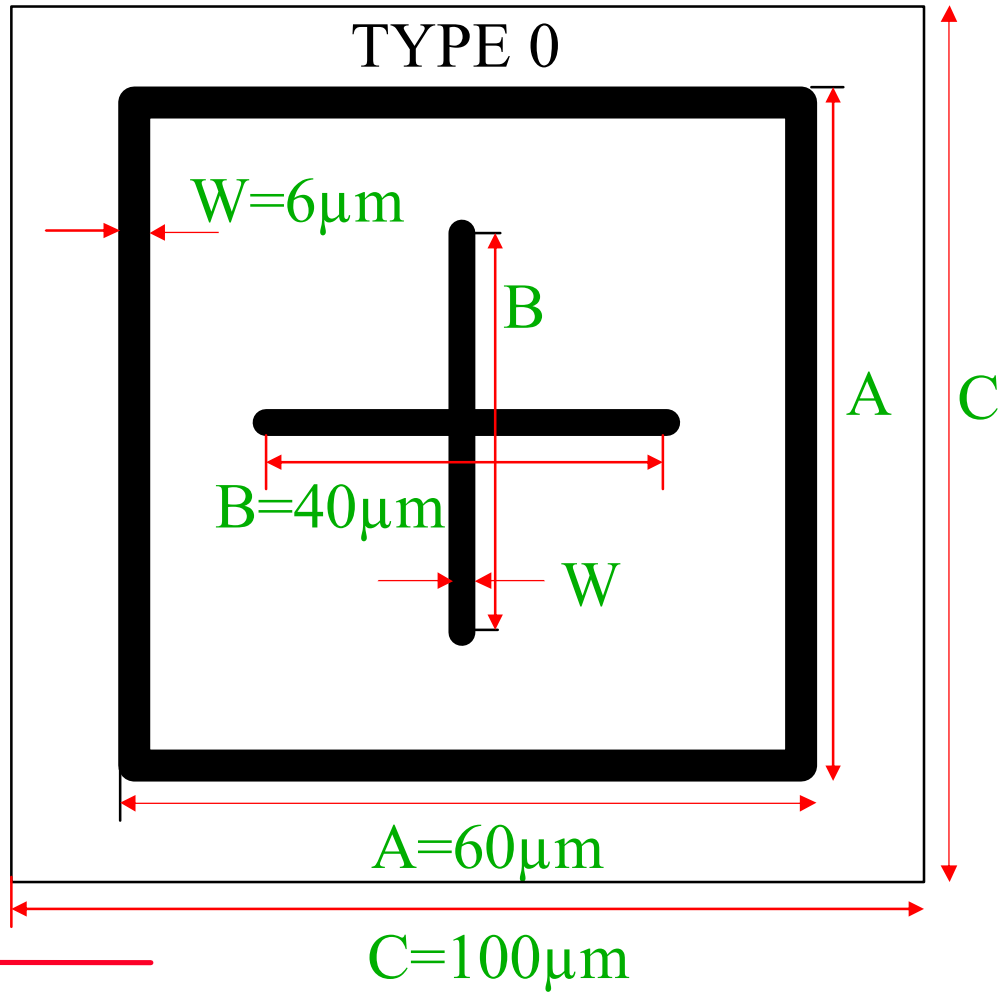
MOSIS DESIGN RULES

Click Here to See MOSIS Design Rules

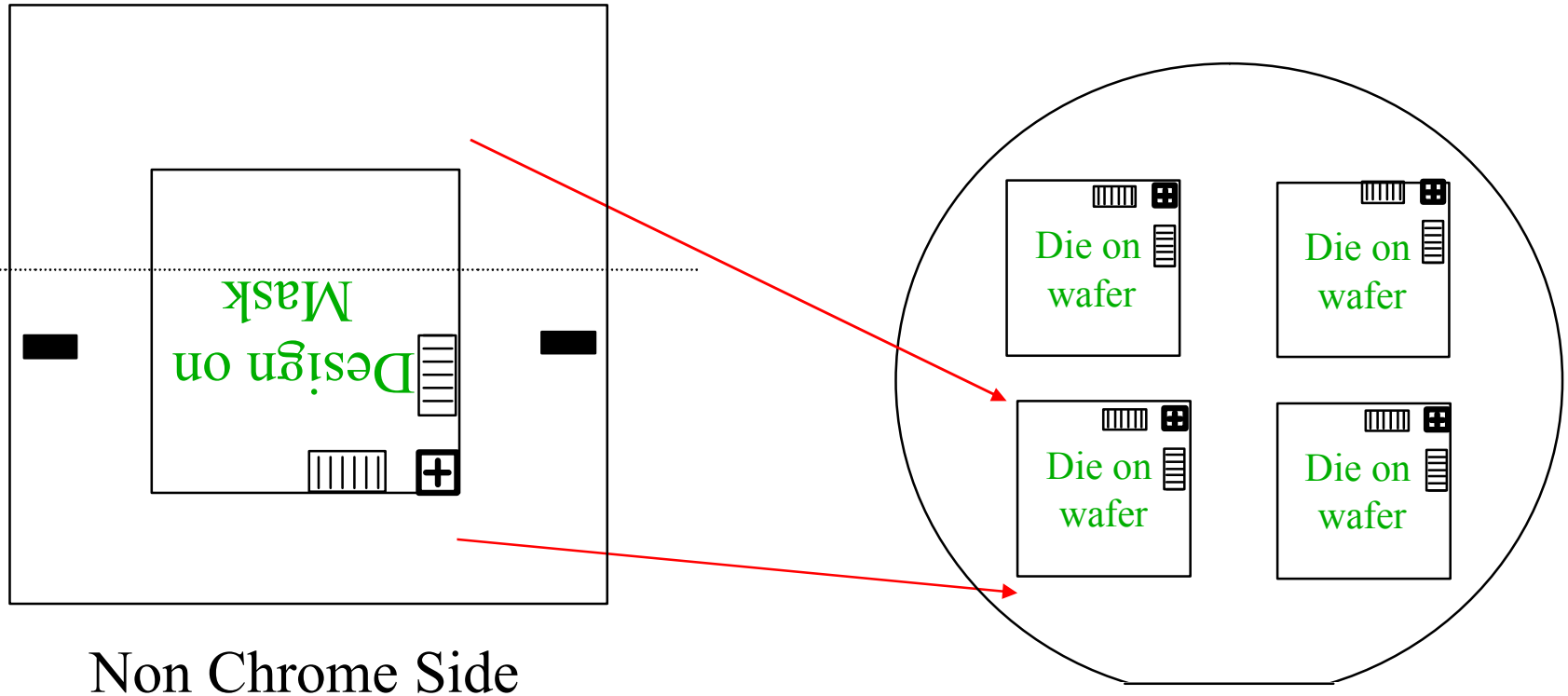


TV PRE ALIGNMENT (TVPA) MARKS

- The TVPA Marks are placed by the designer on design
- TVPA Marks may be copied from the RITPUB directory
- Dimensions are given for sizes on the wafer
- TVPA Marks are used to adjust for rotation (theta)
- On 6” wafers TVPA marks should be placed on the wafer > 90mm apart, on the front half of the wafer



WAFER AUTO ALIGNMENT MARKS for HeNe OR B^2

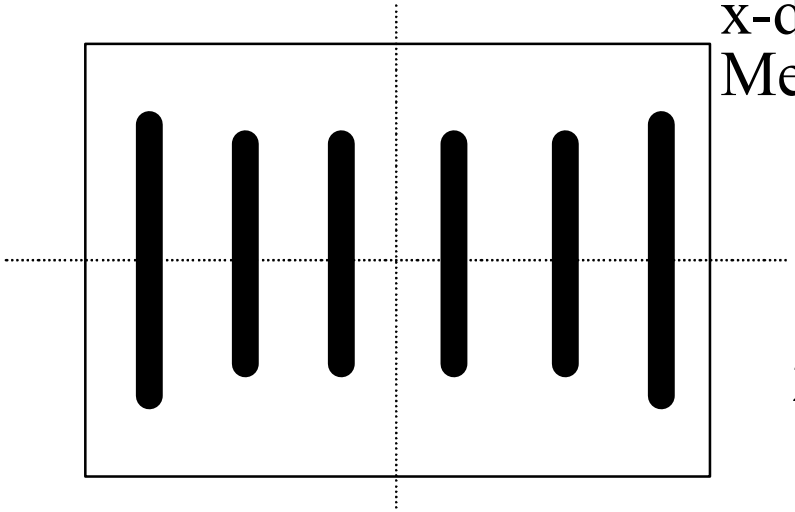


Non Chrome Side

HeNe means marks are illuminated with HeNe Laser
B^2 means broadband (white) light illumination

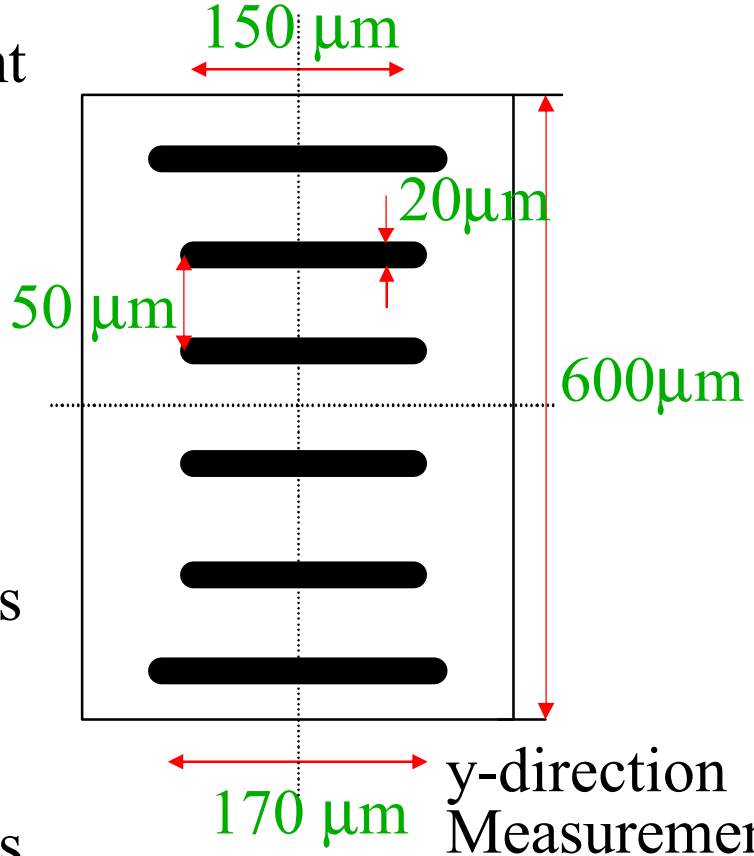
Need 4 die on the wafer with HeNe or B^2 marks for auto alignment. (actually 2-8 die)

WAFER AUTO ALIGNMENT MARKS for HeNe OR B^2



x-direction
Measurement

Type
20P-4F



y-direction
Measurement

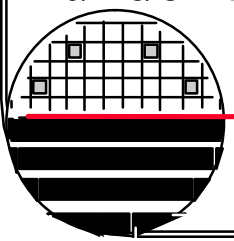
Dimensions are for Sizes on the Reticle. Need both x and y patterns and locations of center for each. These marks are normally in the streets around the edge of the chip. These marks are called multi-marks.

HeNe means marks are illuminated with HeNe Laser
B^2 means broadband (white) light illumination

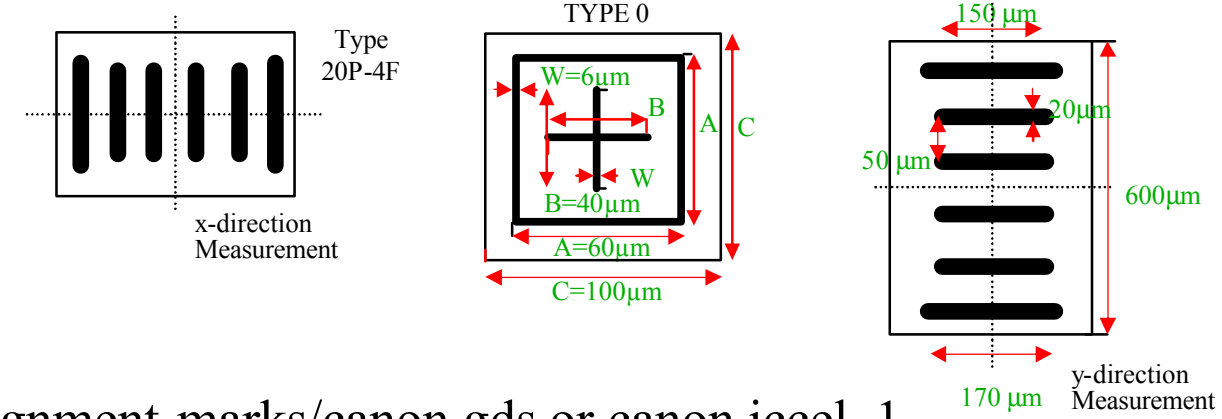
HeNe or B^2 AA USING B-SCOPE AND C-SCOPE

The B and C scopes are alignment microscopes mounted to the right and back of the lens. These scopes have patterns that match the multi-marks (HeNe or B^2 marks) on the wafer and a light intensity detector to determine the alignment signal.

Knowing the location of the y-direction multi-mark on the die, the stage is moved to place the mark under the B-scope (13.0 mm in x-direction). The stage is adjusted slightly in y to give correct alignment signal. The necessary adjustment is recorded. The stage moves the x-direction multi-mark under the C-scope (13.1 mm in y-direction). The stage is adjusted slightly to give correct alignment. The necessary adjustment is recorded. The stepper then calculates the stage position to center the die under the optical column. The stage moves the die under the optical column. The die is exposed.

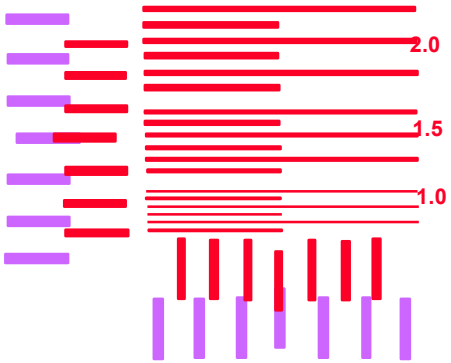


CANON ALIGNMENT, RESOLUTION AND OVERLAY STRUCTURES



Filename
/tools/ritpub/alignment-marks/canon.gds or canon.iccel_1

/tools/ritpub/resolution-overlay/canon.gds or canon.iccel_1



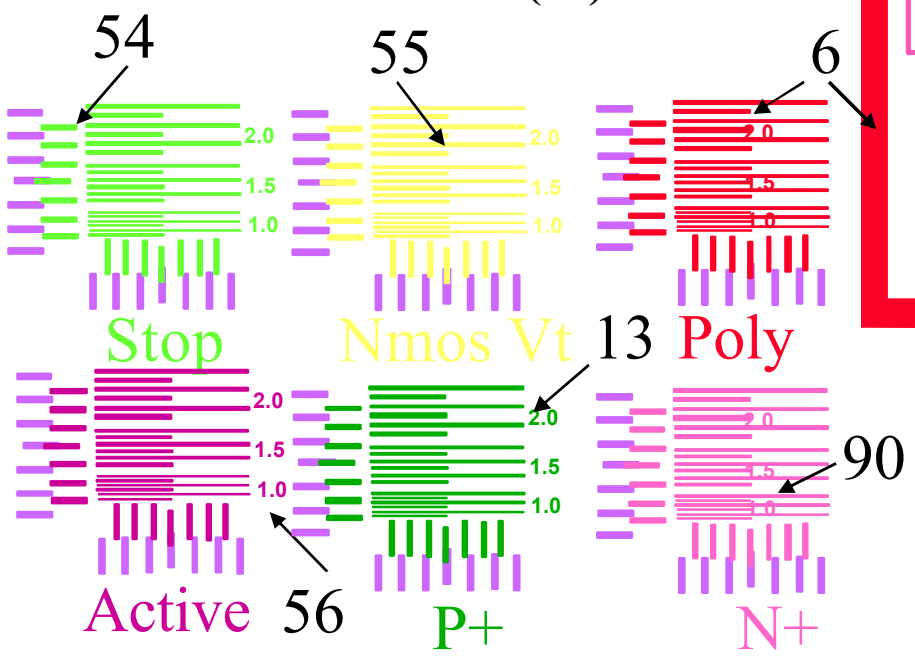
USE OF OTHER LAYERS TO SEPARATE RESOLUTION AND OVERLAY FOR EACH MASK

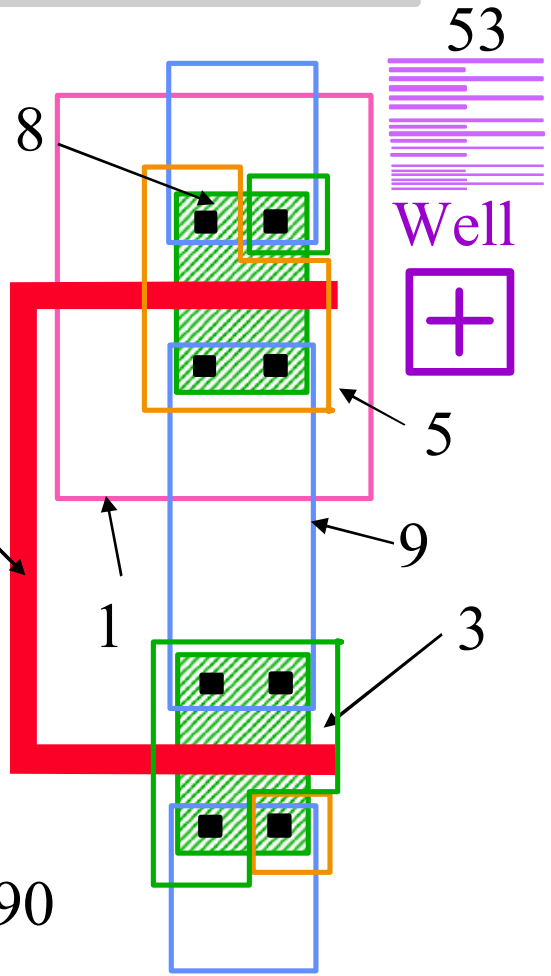
9 Design Layers

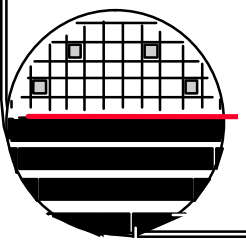
- N-WELL (1)
- ACTIVE (3)
- POLY (6)
- P-SELECT (7)
- CC (8)
- METAL 1 (9)
- N-SELECT
- VIA
- METAL 2

Other Design Layers

- P+ Resolution (13)
- Well Resolution (53)
- Stop Resolution (54)
- Vt Resolution (55)
- Active Resolution (56)
- N+ Resolution (90)







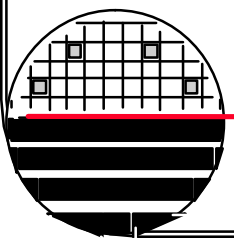
PATTERN GENERATION AND DATA PREP

1. Using Mentor Graphics Design Tools, layout the device layers and save in mentor format. Mentor- ICGraph files (filename.iccel), all layers, polygons with up to 200 vertices

2. Convert the layout information to GDSII file format. GDS2- CALMA files (old IC design tool) (filename.gds), all layers, polygons

3. The GDSII format is then transferred to the CATS system for fracturing (conversion to MEBES format), and other data manipulations such as rotate, mirror, size, bias, and boolean combinations. MEBES- files for electron beam maskmaking tool, each file one layer, trapezoids only

4. Save the file on magnetic tape to transfer to the MEBES.



CONVERSION FROM .ICCEL TO .GDS FORMAT

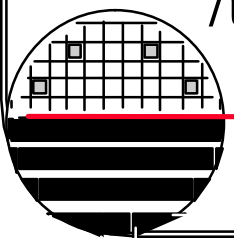
GENERATION OF GDS FILE ON HP COMPUTER SYSTEM:

1. Type: pwd for design pathname and record:
   example: **/home/stu2/sxs8853/senior**
2. Type: **iclink -co -so -i /pathname/designname -d -g filename.gds**

note: design name and filename can be the same.

3. Obtain individual plots for each mask level, label them, and attach to the order form.
4. Copy .gds file to dropbox for maskmaking at RIT
   cp <design name>.gds /dropbox/masks
5. Set protection on file so the file can be accessed

/usr/bin/chmod 644 /dropbox/masks/<design name>.gds



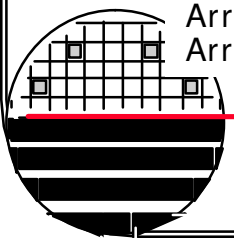
MASK ORDER

Customer Information

Name
Company
Department
Street Address
City, State and Zip Code
Phone Number
( ) -
Project Code
E-mail Address
Order Date
Order Due Date

Mask Information

Design Name	.gds			
Number of Design Layers in Layout				
Number of Mask Levels				
Cell Layout Size	X:	µm	Y:	µm
Alignment Key (Center of Die is Origin)	X:	µm	Y:	µM
Fracture Resolution	0.5µm	Other		
Scale Factor	1X	4X	5X	
Mirror135	Yes	None	Other	
Rotation	zero	90	Other	
Plate Size	5” x 5” x 0.090” – Email for other sizes			
Number of Levels on Plate				
Array	None			
Array with	rows and		columns	



MASK ORDER

Mask Level Name	Mask Level #	Design Layer Name	Design Layer #	Boolean Function	Field Type
Nwell	1	n_well.l	1	1 ORed 53	Dark
Active	2	active._area.i	3		Clear
Stop	3			1 ORed 3	Clear
PMOS VT	4	poly.l	6		Dark
Poly	5	?			Clear
N+DS	6	?			Dark
P+DS	7	?			Dark
CC	8	contact_a.l	8		Dark
Metal One	9	metal1.l	9		Clear
Via	10	pad.l	15		Dark
Metal Two	11	?			Clear

MASK BOX LABELS

Rochester Institute of Technology
Microelectronic Engineering

Dr. Fuller's MASK

SMFL-CMOS Testchip for Canon Stepper

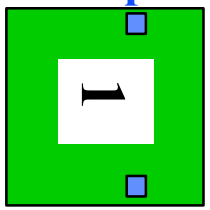


Plate 1 of 7

Reticle ID	Level #	Stepper Job Name
Nwell	1	F033SMFLTEST_NWELL

Alignment Key: On this reticle at locations given below
Alignment Mark Locations:
TV Pre Align PA X=2.23 Y=1.37 Rows = 12
Fine B X=1.87 Y=1.159 Col = 10
C X=1.66 Y=1.37
Step Size X =13.5 mm Y = 10.5 mm
Date: 3-17-04 Owner:Dr. Fuller
IC Graph Filename: smflcmos031704.gds
IC Graph File Location: /home/usr/lff
Mask ID: NWELL

Rochester Institute of Technology
Microelectronic Engineering

Dr. Fuller's MASK

SMFL-CMOS Testchip for Canon Stepper

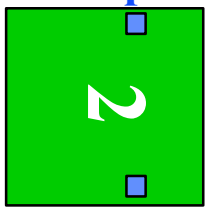


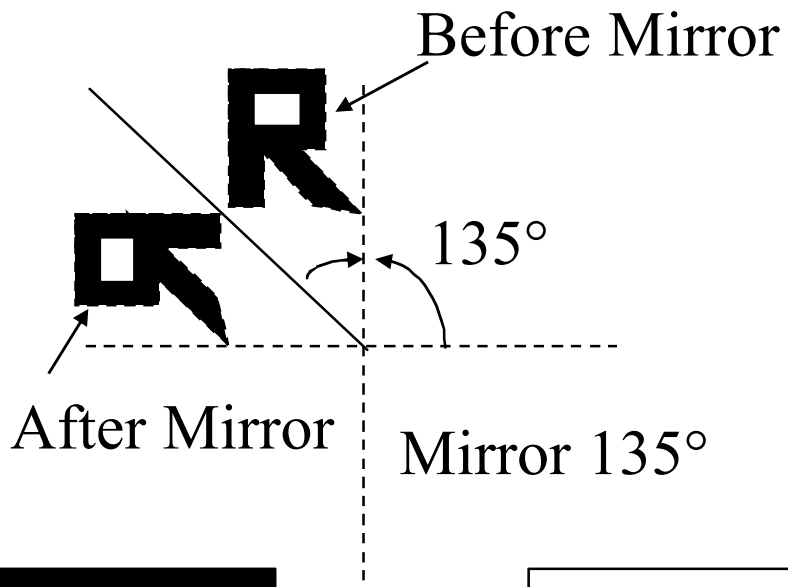
Plate 2 of 7

Reticle ID	Level #	Stepper Job Name
Active	2	F033SMFLTEST_ACT

Alignment Key: On this reticle at locations given below
Alignment Mark Locations:
TV Pre Align PA X=2.23 Y=1.37 Rows = 12
Fine B X=1.87 Y=1.159 Col = 10
C X=1.66 Y=1.37
Step Size X =13.5 mm Y = 10.5 mm
Date: 3-17-04 Owner:Dr. Fuller
IC Graph Filename: smflcmos031704.gds
IC Graph File Location: /home/usr/lff
Mask ID: ACTIVE

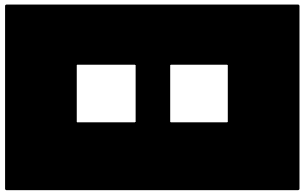
Rochester Institute of Technology
Microelectronic Engineering

DATA PREP USING CATS

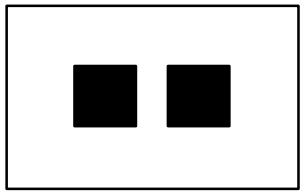


Input File: GDS2- CALMA files (old IC design tool) (filename.gds), all layers, polygons

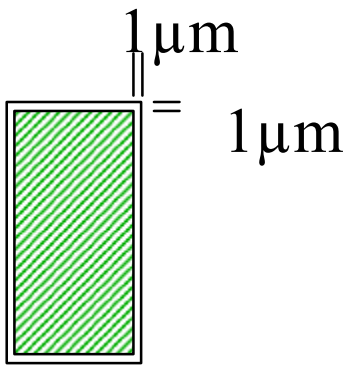
Output File: MEBES- files for electron beam maskmaking tool, each file one layer, trapezoids only



Dark Field: Black is chrome, White is Quartz.



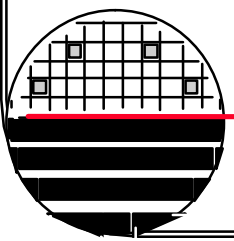
Light Field: Black is chrome, White is Quartz.



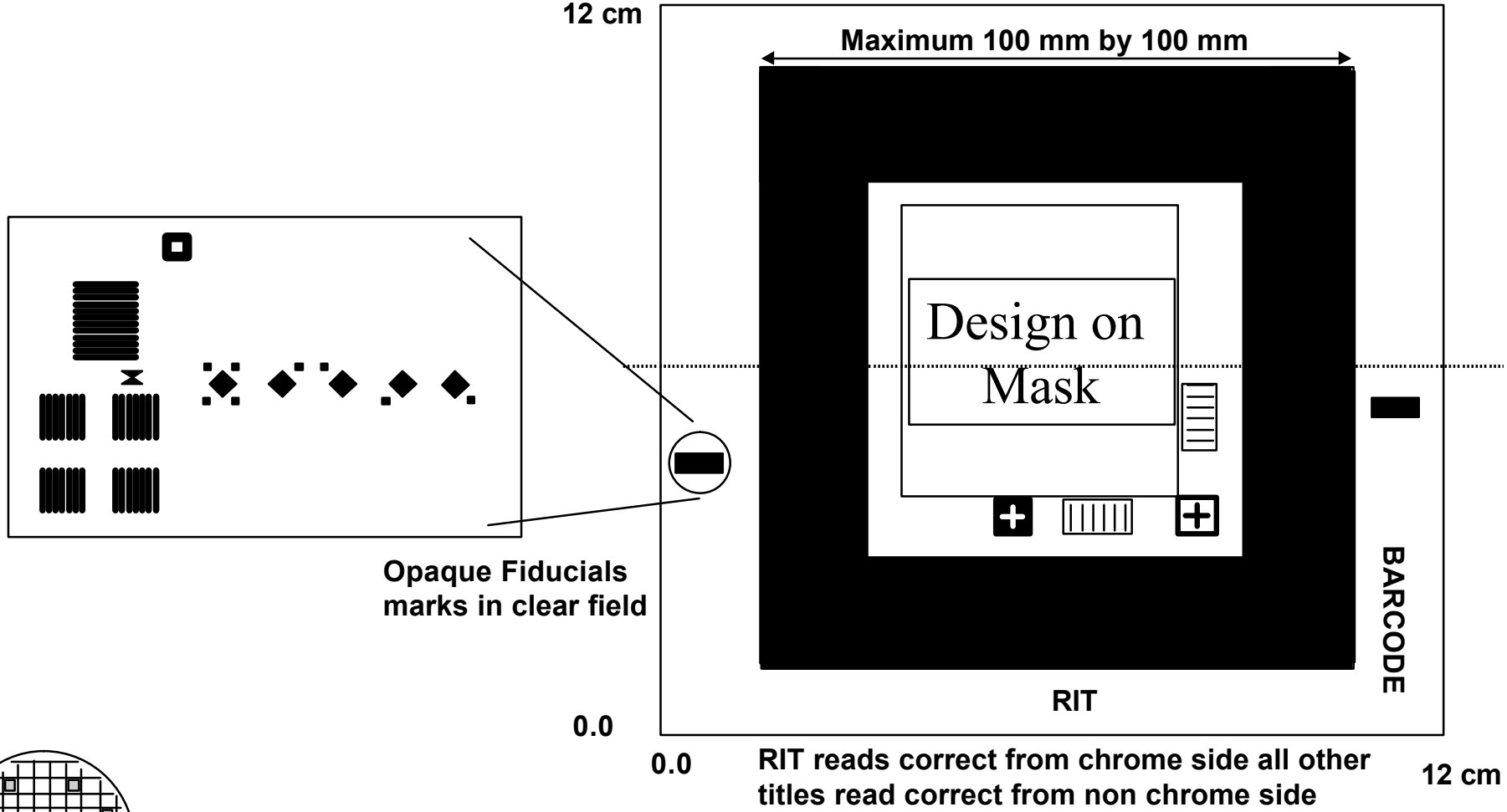
BIAS +1µm

SAVE IN MEBES FORMAT

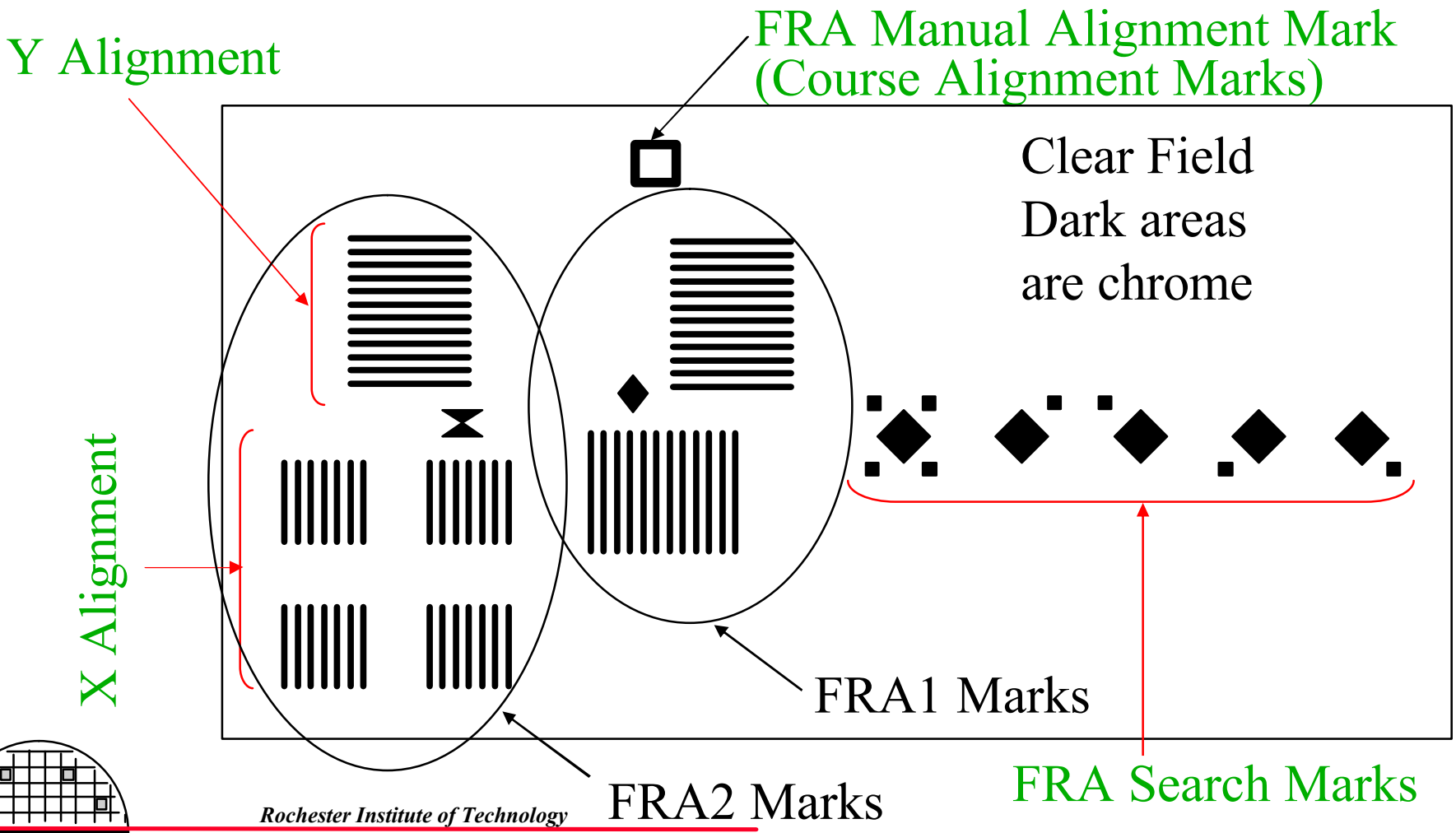
MEBES format - files for electron beam maskmaking tool,
each file one layer
trapezoids only



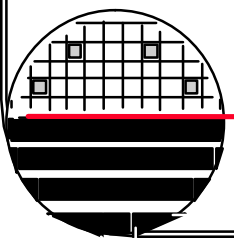
CANON RETICLE AND FIDUCIAL MARKS



FINE RETICAL ALIGNMENT (FRA) FIDUCIAL MARKS



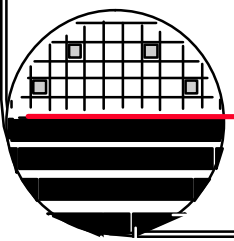
STEPPER JOBS



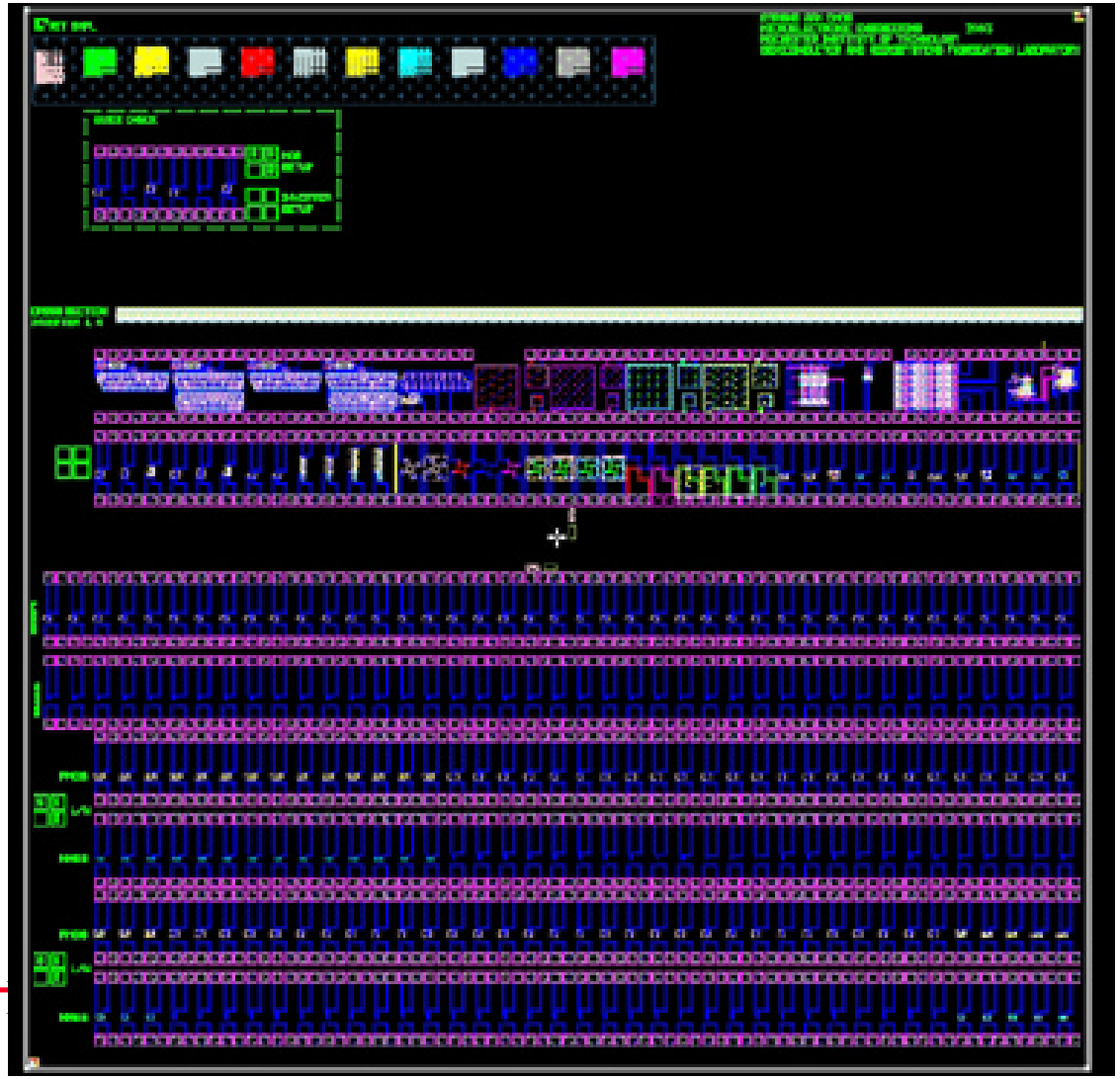
TEST CHIP

Set Cell Process /class/eecc630/SCNA20

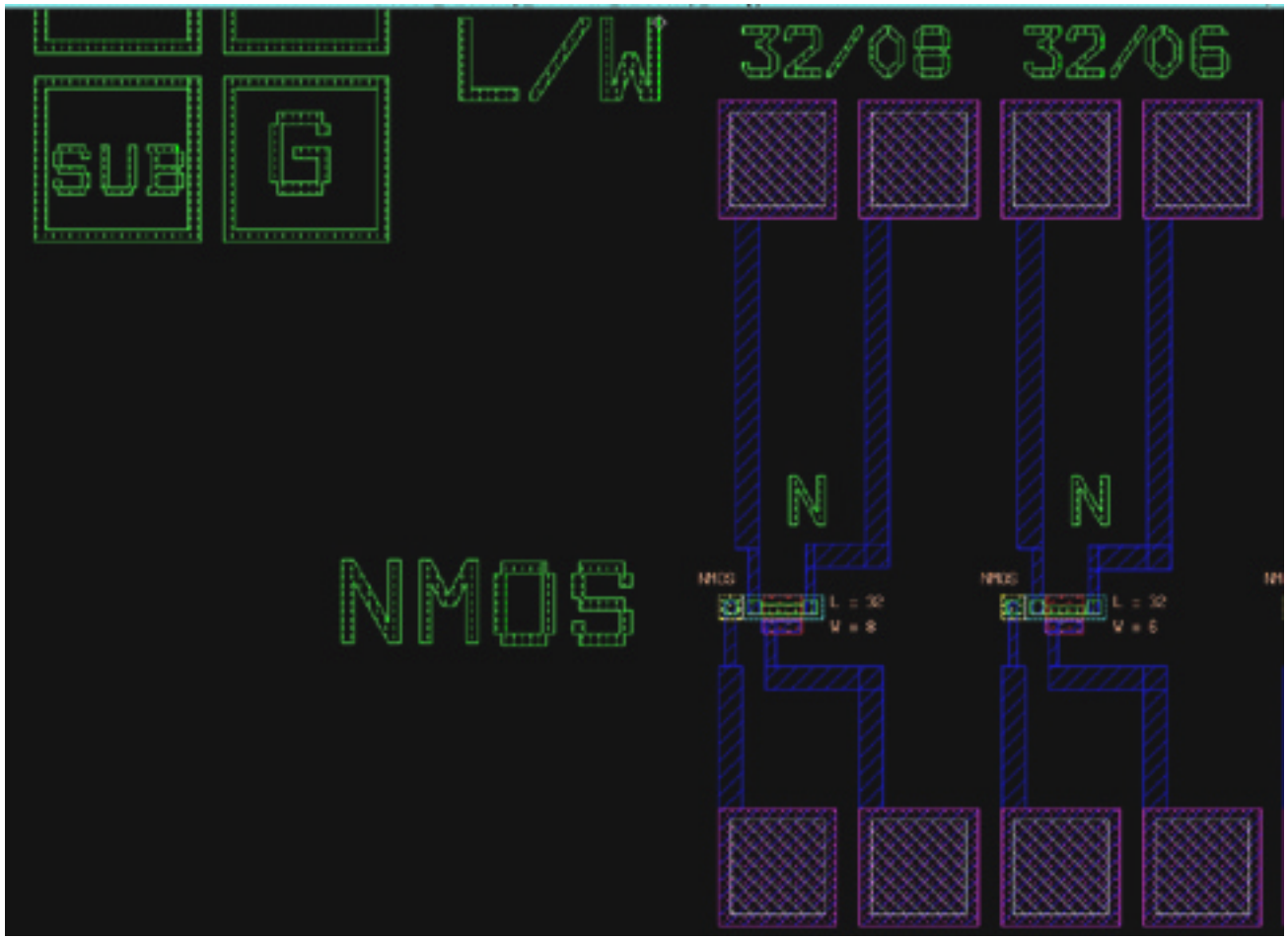
/dropbox/SA_TESTchip_V14
Translate > Read GDSII



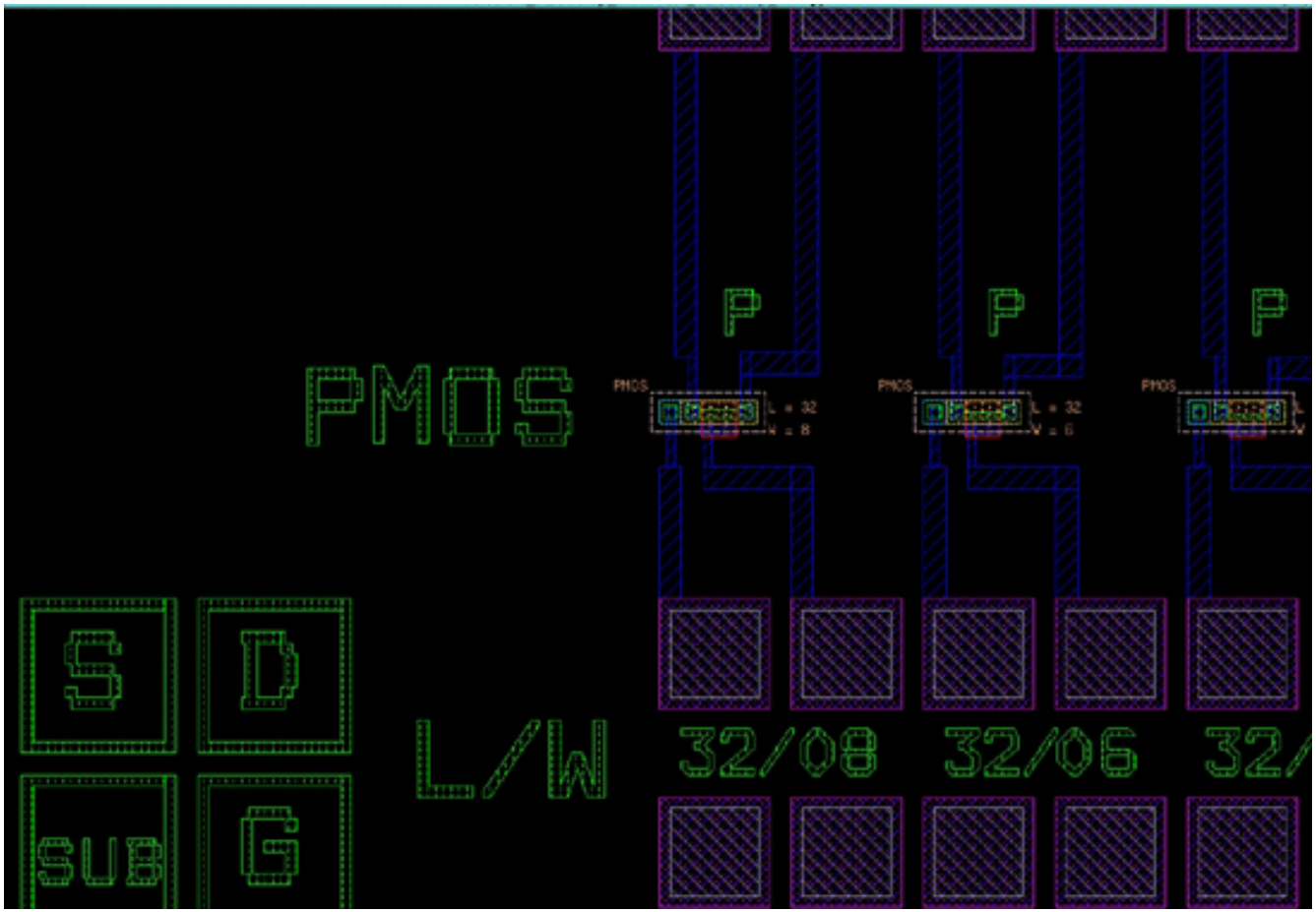
TEST CHIP



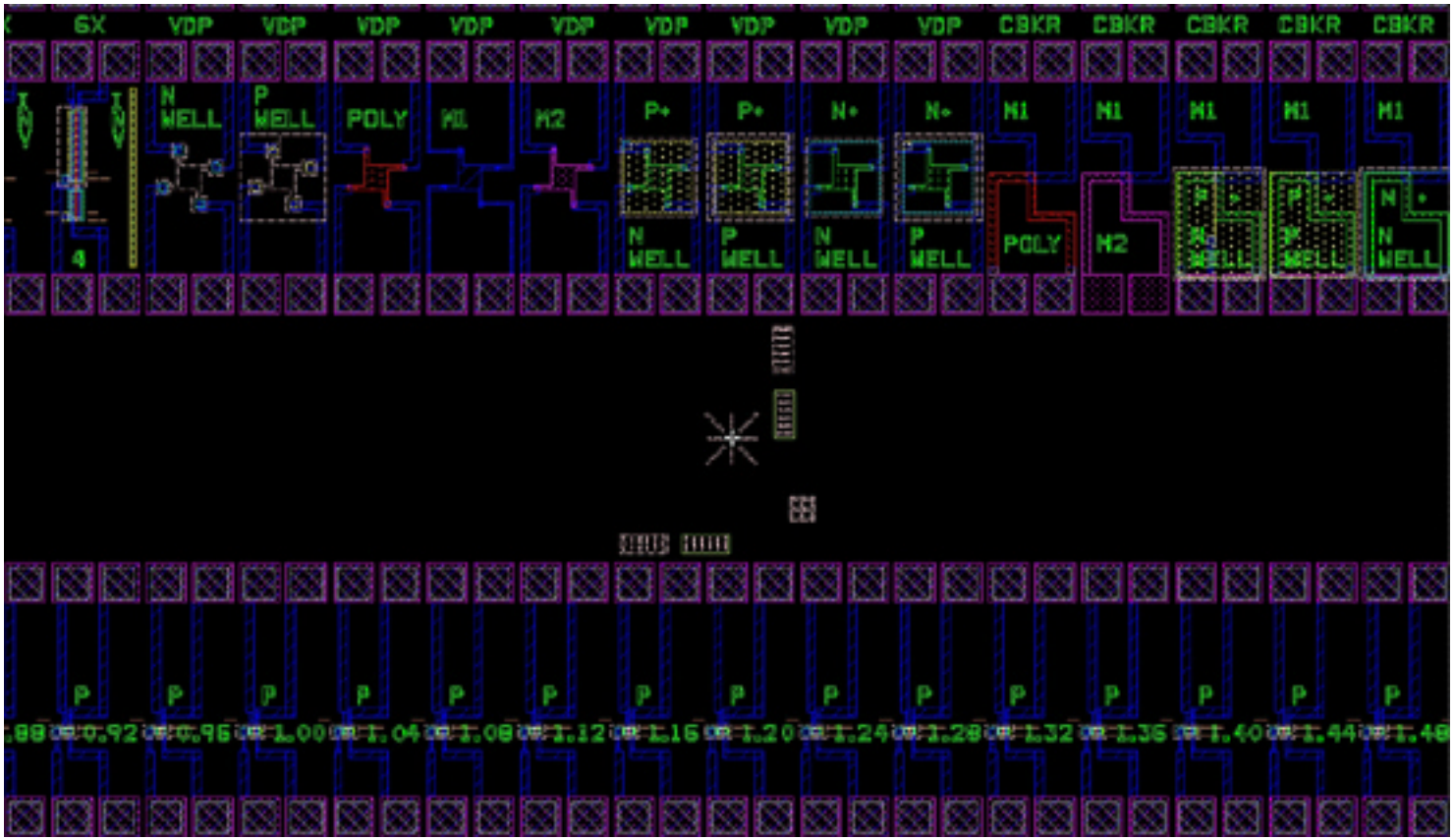
TEST CHIP



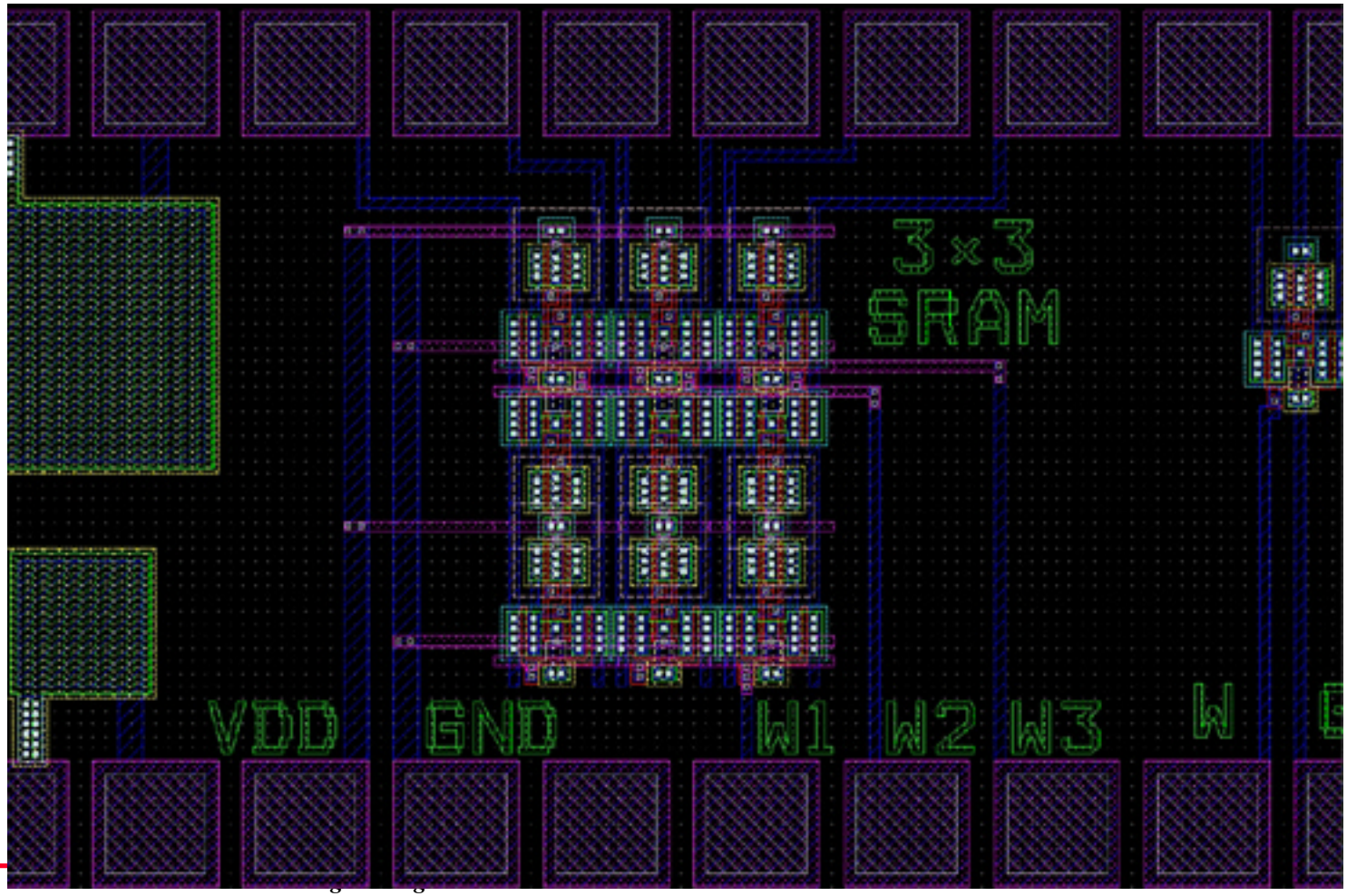
TEST CHIP



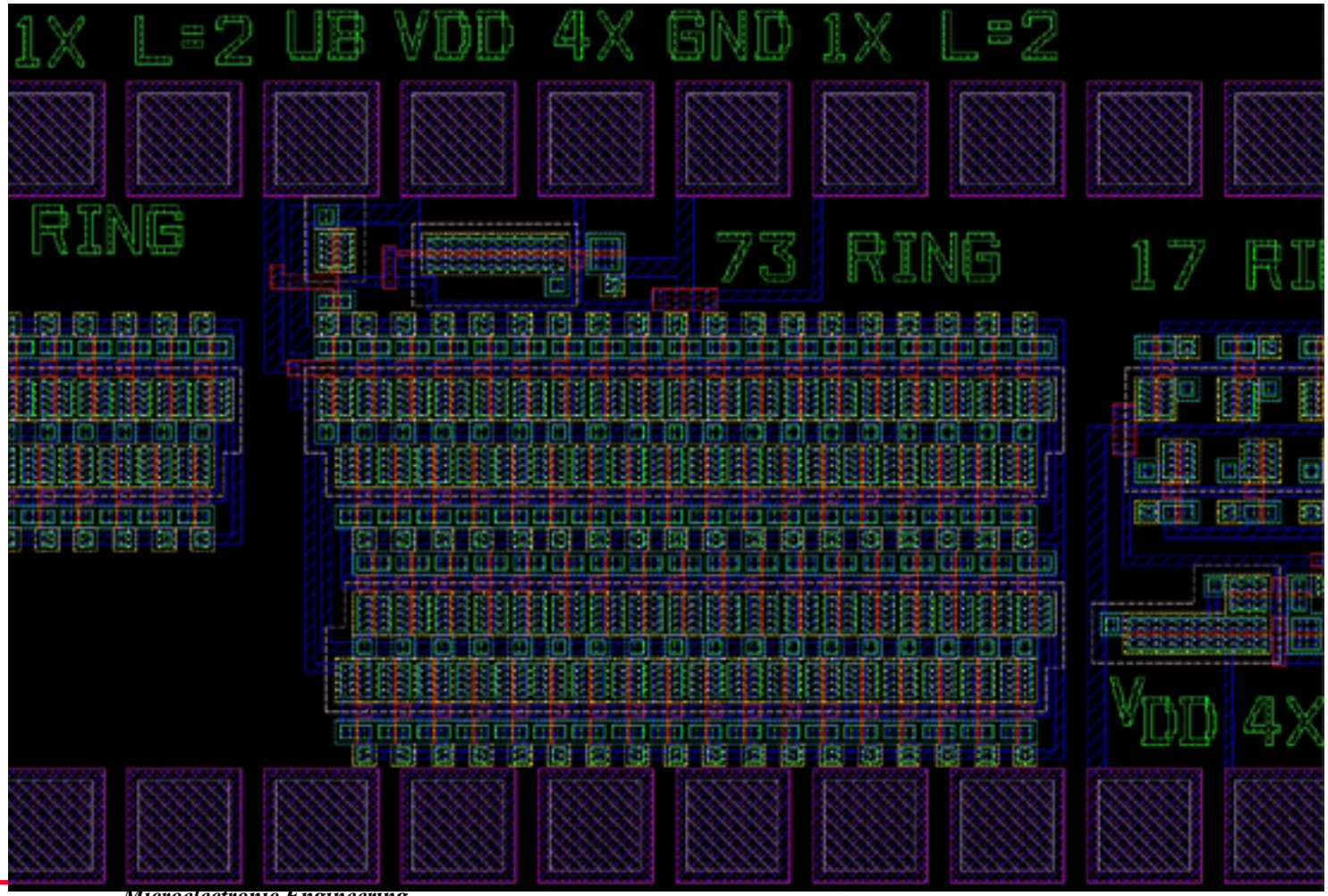
TEST CHIP

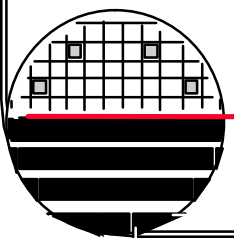

6X
VDP
CBKR
N WELL
P WELL
POLY
M1
M2
P+
N+
P
1.00
1.04
1.08
1.12
1.16
1.20
1.24
1.28
1.32
1.36
1.40
1.44

TEST CHIP



TEST CHIP

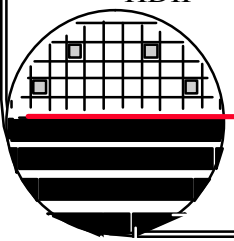




Microelectronic Engineering

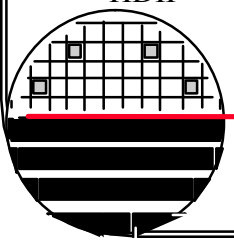
NMOS NOMINAL BSIM3 (V3.1) SPICE PARAMETERS

```
.model nch nmos ( LEVEL   = 11
+  VERSION = 3.1    TNOM    = 27     TOX     = 3.10E-8     XJ     = 9.0E-7       NCH     = 8.2E16       VTH0    = 1.026
+  K1      = 1.724      K2      = -0.1212      K3      = 0      K3B     = 0           W0      = 2.5E-6       NLX     = 4.80E-9
+  DVT0W   = 0          DVT1W   = 0          DVT2W   = -0.032      DVT0    = 0.1466       DVT1    = 0.038       DVT2    = 0.1394
+  U0      = 687.22       UA      = 2.34E-9       UB      = -1.85E-18       UC      = -1.29E-11       VSAT    = 1.64E5       A0      = 0.4453
+  AGS     = 0          B0      = 0          B1      = 0          KETA    = -0.0569       A1      = 0          A2      = 1
+  RDSW    = 376.89       PRWG    = 0          PRWB    = 0          WR      = 1          WINT    = 2.58E-8       LINT    = 1.86E-8
+  XL      = 0          XW      = 0          DWG     = 0          DWB     = 0          VOFF    = -0.1056       NFACTOR = 0.8025
+  CIT     = 0          CDSC    = -2.59E-5       CDSCD   = 0          CDSCB   = 0          ETA0    = 0          ETAB    = 0
+  DSUB    = 0.0117     PCLM    = 0.6184       PDIBLC1 = 0.0251       PDIBLC2 = 0.00202       PDIBLCB = 0       DROUT   = 0.0772
+  PSCBE1  = 2.77E9       PSCBE2  = 3.11E-8       PVAG    = 0       DELTA   = 0.01       MOBMOD  = 1          PRT     = 0
+  UTE     = -1.5       KT1     = 0          KT1L    = 0       KT2     = 0          UA1     = 4.30E-9       UB1     = -7.60E-18
+  UC1     = -5.6E-11       AT      = 3.3E4       WL      = 0       WLN     = 1          WW      = 0          WWN     = 1
+  WWL     = 0          LL      = 0          LLN     = 1       LW      = 0          LWN     = 1          LWL     = 0
+  CAPMOD  = 2          XPART   = 0       CGDO    = 1.99E-10       CGSO    = 1.99E-10       CGBO    = 0       CJ      = 4.233802E-4
+  PB      = 0.9899238      MJ      = 0.4495859      CJSW    = 3.825632E-10       PBSW    = 0.1082556       MJSW    = 0.1083618
+  PVTH0   = 0.0212852      PRDSW   = -16.1546703       PK2     = 0.0253069       WKETA   = 0.0188633       LKETA   = 0.0204965
+  HDIF    = hdifn)
```



PMOS NOMINAL BSIM3 (V3.1) SPICE PARAMETERS

```
.model pch pmos (       LEVEL   = 11
+  VERSION = 3.1     TNOM    = 27     TOX     = 3.10E-8     XJ      = 8.80E-7      NCH     = 3.10E16      VTH0    = -1.166
+  K1      = 0.3029  K2      = 0.1055  K3      = 0           K3B     = 0            W0      = 2.50E-6      NLX     = 2.01E-8
+  DVT0W   = 0       DVT1W   = 0       DVT2W   = -0.032      DVT0    = 2            DVT1    = 0.5049       DVT2    = -0.0193
+  U0      = 232.53  UA      = 4.00E-9 UB      = -2.26E-18   UC      = -6.80E-11    VSAT    = 4.40E4       A0      = 0.6045
+  AGS     = 0       B0      = 0       B1      = 0           KETA    = -0.0385      A1      = 0            A2      = 1
+  RDSW    = 1.23E3  PRWG    = 0       PRWB    = 0           WR      = 1            WINT    = 1.67E-8      LINT    = 6.50E-8
+  XL      = 0       XW      = 0       DWG     = 0           DWB     = 0            VOFF    = -0.0619      NFACTOR = 1.454
+  CIT     = 0       CDSC    = -4.30E-4  CDSCD   = 0         CDSCB   = 0            ETA0    = 0            ETAB    = 0
+  DSUB    = 0.2522  PCLM    = 5.046   PDIBLC1 = 0          PDIBLC2 = 1.00E-5      PDIBLCB = 0            DROUT   = 0.2522
+  PSCBE1  = 2.80E9  PSCBE2  = 2.98E-8 PVAG    = 0         DELTA   = 0.01         MOBMOD  = 1            PRT     = 0
+  UTE     = -1.5    KT1     = 0       KT1L    = 0         KT2     = 0            UA1     = 4.30E-9      UB1     = -7.60E-18
+  UC1     = -5.6E-11  AT    = 3.3E4   WL      = 0         WLN     = 1            WW      = 0            WWN     = 1
+  WWL     = 0       LL      = 0       LLN     = 1         LW      = 0            LWN     = 1            LWL     = 0
+  CAPMOD  = 2       XPART   = 0       CGDO    = 2.4E-10   CGSO    = 2.4E-10      CGBO    = 0            CJ      = 7.273568E-4
+  PB      = 0.9665597  MJ     = 0.4959837  CJSW    = 3.114708E-10  PBSW    = 0.99  MJSW    = 0.2653654  PVTH0   = 9.420541E-3
+  PRDSW   = -231.2571566  PK2  = 1.396684E-3  WKETA  = 1.862966E-3  LKETA   = 5.728589E-3
+  HDIF    = hdifp   )
```



HOT SPICE MODELS

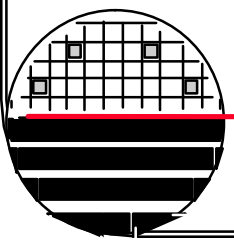
All parameters the same except those listed are changed to give more transistor current:

.model **hot** nmos (LEVEL = 11 VERSION = 3.1

TOX = 2.70E-8 **VTH0**= 0.926 **U0** = 750 **RDSW** = 330)

.model **hot** pmos (LEVEL = 11 VERSION = 3.1

TOX = 2.70E-8 **VTH0**= -1.066 **U0** = 250 **RDSW** = 1.00E3)



COLD SPICE MODEL

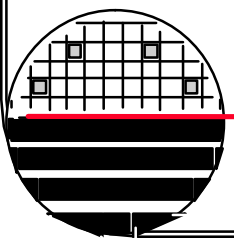
All parameters the same except those listed are changed to give less transistor current:

.model **cold** nmos (LEVEL = 11 VERSION = 3.1

TOX = 3.50E-8 **VTH0**= 1.126 **U0** = 620 **RDSW** = 410)

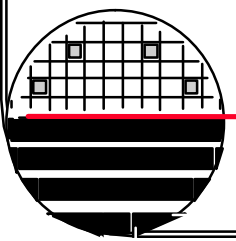
.model **cold** pmos (LEVEL = 11 VERSION = 3.1

TOX = 3.50E-8 **VTH0**= -1.266 **U0** = 200 **RDSW** = 1.45E3)



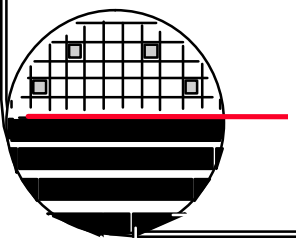
NMOS COLD

```
.model nch nmos (                                    LEVEL   = 11
+    VERSION = 3.1          TNOM    = 27             TOX     = 3.70E-8
+    XJ      = 8.6E-7       NCH     = 8.6E16         VTH0    = 1.282
+    K1      = 1.63         K2      = 0.0167         K3      = 0
+    K3B     = 0            W0      = 2.5E-6         NLX     = 8.80E-9
+    DVT0W   = 0            DVT1W   = 0              DVT2W   = -0.032
+    DVT0    = 0.1007       DVT1    = 0.0455         DVT2    = -0.1657
+    U0      = 701.12       UA      = 2.21E-9        UB      = -1.29E-18
+    UC      = -4.80E-11    VSAT    = 7.20E4         A0      = 0.342
+    AGS     = 0            B0      = 0              B1      = 0
+    KETA    = -0.0308      A1      = 0              A2      = 1
+    RDSW    = 1.13E3       PRWG    = 0              PRWB    = 0
+    WR      = 1            WINT    = 9.90E-8        LINT    = 1.25E-7
+    XL      = 0            XW      = 0              DWG     = 0
+    DWB     = 0            VOFF    = -0.1015        NFACTOR = 0.7948
+    CIT     = 0            CDSC    = -1.01E-5       CDSCD   = 0
+    CDSCB   = 0            ETA0    = 0              ETAB    = 0
+    DSUB    = 6.80E-4      PCLM    = 0.5599         PDIBLC1 = 0.00541
+    PDIBLC2 = 0.0021       PDIBLCB = 0              DROUT   = 0.0355
+    PSCBE1  = 2.59E9       PSCBE2  = 2.80E-8        PVAG    = 0
+    DELTA   = 0.01         MOBMOD  = 1              PRT     = 0
+    UTE     = -1.5         KT1     = 0              KT1L    = 0
+    KT2     = 0            UA1     = 4.30E-9        UB1     = -7.60E-18
+    UC1     = -5.6E-11     AT      = 3.3E4          WL      = 0
+    WLN     = 1            WW      = 0              WWN     = 1
+    WWL     = 0            LL      = 0              LLN     = 1
+    LW      = 0            LWN     = 1              LWL     = 0
+    CAPMOD  = 2            XPART   = 0              CGDO    = 1.99E-10
+    CGSO    = 1.99E-10     CGBO    = 0              CJ      = 4.233802E-4
+    PB      = 0.9899238    MJ      = 0.4495859      CJSW    = 3.825632E-10
+    PBSW    = 0.1082556    MJSW    = 0.1083618      PVTH0   = 0.0212852
+    PRDSW   = -16.1546703  PK2     = 0.0253069      WKETA   = 0.0188633
+    LKETA   = 0.0204965
+    HDIF    = hdifn        )
```



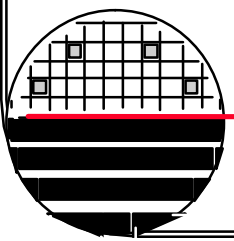
PMOS COLD

```
.model pch pmos (                                    LEVEL   = 11
+   VERSION = 3.1           TNOM    = 27             TOX     = 3.40E-8
+   XJ      = 9.00E-7       NCH     = 2.60E16        VTH0    = -1.461
+   K1      = 0.0766        K2      = 0.2287         K3      = 0
+   K3B     = 0             W0      = 2.50E-6        NLX     = 4.40E-8
+   DVT0W   = 0             DVT1W   = 0              DVT2W   = -0.032
+   DVT0    = 0.16          DVT1    = 0.1091         DVT2    = -0.6009
+   U0      = 214.32        UA      = 3.30E-9        UB      = -1.37E-18
+   UC      = -6.90E-11     VSAT    = 1.94E4         A0      = 0.1
+   AGS     = 0             B0      = 0              B1      = 0
+   KETA    = -0.0489       A1      = 0              A2      = 1
+   RDSW    = 481.9         PRWG    = 0              PRWB    = 0
+   WR      = 1             WINT    = 6.10E-8        LINT    = 1.28E-7
+   XL      = 0             XW      = 0              DWG     = 0
+   DWB     = 0             VOFF    = -0.0564        NFACTOR = 0.5158
+   CIT     = 0             CDSC    = 9.70E-6        CDSCD   = 0
+   CDSCB   = 0             ETA0    = 0              ETAB    = 0
+   DSUB    = 0.00745       PCLM    = 14.255         PDIBLC1 = 0
+   PDIBLC2 = 0.00149       PDIBLCB = 0              DROUT   = 0.1091
+   PSCBE1  = 2.64E9        PSCBE2  = 2.79E-8        PVAG    = 0
+   DELTA   = 0.01          MOBMOD  = 1              PRT     = 0
+   UTE     = -1.5          KT1     = 0              KT1L    = 0
+   KT2     = 0             UA1     = 4.30E-9        UB1     = -7.60E-18
+   UC1     = -5.6E-11      AT      = 3.3E4          WL      = 0
+   WLN     = 1             WW      = 0              WWN     = 1
+   WWL     = 0             LL      = 0              LLN     = 1
+   LW      = 0             LWN     = 1              LWL     = 0
+   CAPMOD  = 2             XPART   = 0              CGDO    = 2.4E-10
+   CGSO    = 2.4E-10       CGBO    = 0              CJ      = 7.273568E-4
+   PB      = 0.9665597     MJ      = 0.4959837      CJSW    = 3.114708E-10
+   PBSW    = 0.99          MJSW    = 0.2653654      PVTH0   = 9.420541E-3
+   PRDSW   = -231.2571566  PK2     = 1.396684E-3    WKETA   = 1.862966E-3
+   LKETA   = 5.728589E-3
+  HDIF    = hdifp   )
```



NMOS HOT

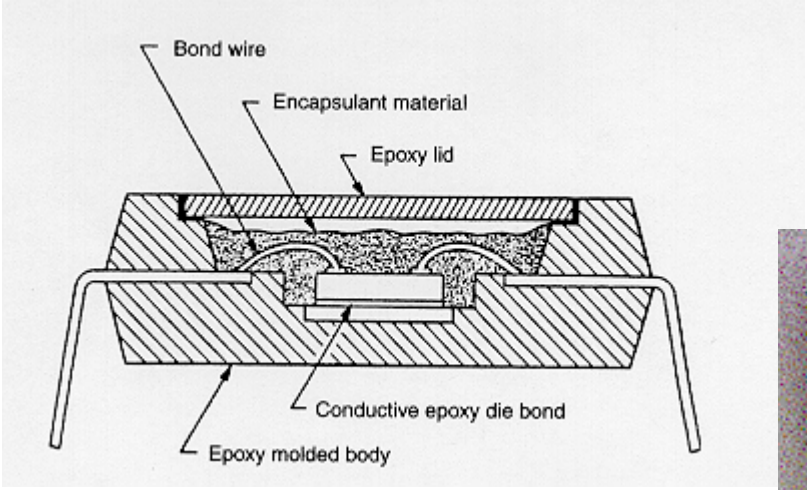
```
.model nch nmos (                                    LEVEL   = 11
+    VERSION = 3.1          TNOM    = 27              TOX     = 2.99E-8
+    XJ      = 1.0E-6       NCH     = 6.5E16          VTH0    = 0.8411
+    K1      = 1.117        K2      = 0.0138          K3      = 0
+    K3B     = 0            W0      = 2.5E-6          NLX     = 2.12E-8
+    DVT0W   = 0            DVT1W   = 0               DVT2W   = -0.032
+    DVT0    = 0.1692       DVT1    = 0.042           DVT2    = -0.1482
+    U0      = 790.78       UA      = 2.55E-9         UB      = -4.50E-18
+    UC      = -1.62E-10    VSAT    = 1.46E5          A0      = 0.5306
+    AGS     = 0            B0      = 0               B1      = 0
+    KETA    = -0.0465      A1      = 0               A2      = 1
+    RDSW    = 182.48       PRWG    = 0               PRWB    = 0
+    WR      = 1            WINT    = 2.23E-8         LINT    = -1.53E-8
+    XL      = 0            XW      = 0               DWG     = 0
+    DWB     = 0            VOFF    = -0.0958         NFACTOR = 0.7539
+    CIT     = 0            CDSC    = -2.92E-5        CDSCD   = 0
+    CDSCB   = 0            ETA0    = 0               ETAB    = 0
+    DSUB    = 0.0112       PCLM    = 1.762           PDIBLC1 = 0.0211
+    PDIBLC2 = 0.00248      PDIBLCB = 0               DROUT   = 0.066
+    PSCBE1  = 8.40E9       PSCBE2  = 3.20E-8         PVAG    = 0
+    DELTA   = 0.01         MOBMOD  = 1               PRT     = 0
+    UTE     = -1.5         KT1     = 0               KT1L    = 0
+    KT2     = 0            UA1     = 4.30E-9         UB1     = -7.60E-18
+    UC1     = -5.6E-11     AT      = 3.3E4           WL      = 0
+    WLN     = 1            WW      = 0               WWN     = 1
+    WWL     = 0            LL      = 0               LLN     = 1
+    LW      = 0            LWN     = 1               LWL     = 0
+    CAPMOD  = 2            XPART   = 0               CGDO    = 1.99E-10
+    CGSO    = 1.99E-10     CGBO    = 0               CJ      = 4.233802E-4
+    PB      = 0.9899238    MJ      = 0.4495859       CJSW    = 3.825632E-10
+    PBSW    = 0.1082556    MJSW    = 0.1083618       PVTH0   = 0.0212852
+    PRDSW   = -16.1546703  PK2     = 0.0253069       WKETA   = 0.0188633
+    LKETA   = 0.0204965
+    HDIF    = hdifn       )
```

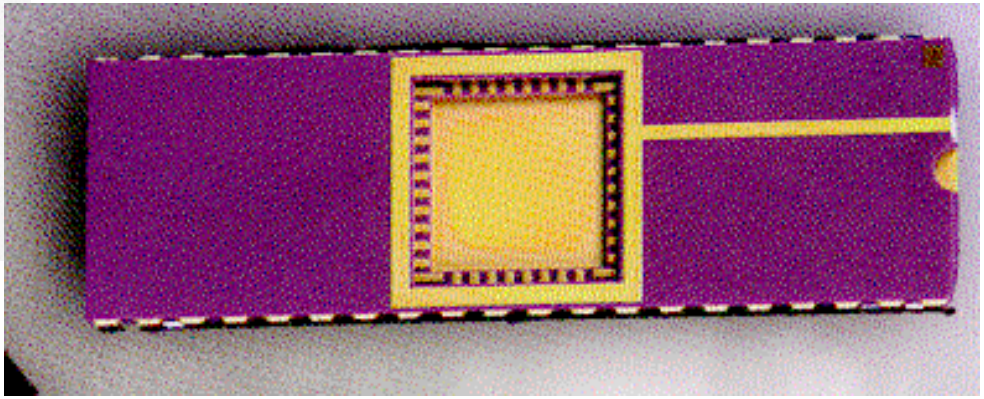


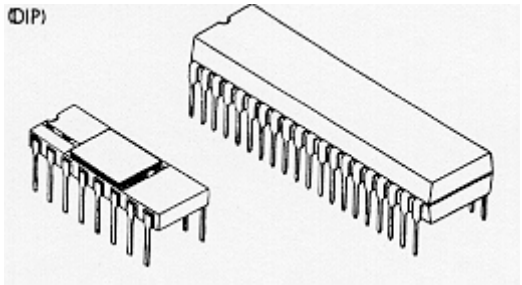
PMOS HOT

```
.model pch pmos (                                    LEVEL   = 11
+    VERSION = 3.1          TNOM    = 27              TOX     = 3.20E-8
+    XJ      = 9.50E-7      NCH     = 3.50E16         VTH0    = -0.8576
+    K1      = 0.5848       K2      = -0.00369        K3      = 0
+    K3B     = 0            W0      = 2.50E-6         NLX     = 2.19E-8
+    DVT0W   = 0            DVT1W   = 0               DVT2W   = -0.032
+    DVT0    = 2            DVT1    = 0.3564          DVT2    = 0.0283
+    U0      = 258.34       UA      = 5.00E-9         UB      = -2.31E-18
+    UC      = -1.07E-10    VSAT    = 1.96E4          A0      = 0.1
+    AGS     = 0            B0      = 0               B1      = 0
+    KETA    = -0.0533      A1      = 0               A2      = 1
+    RDSW    = 369.91       PRWG    = 0               PRWB    = 0
+    WR      = 1            WINT    = 6.80E-8         LINT    = 1.42E-7
+    XL      = 0            XW      = 0               DWG     = 0
+    DWB     = 0            VOFF    = -0.045          NFACTOR = 0.6032
+    CIT     = 0            CDSC    = -6.40E-4        CDSCD   = 0
+    CDSCB   = 0            ETA0    = 0               ETAB    = 0
+    DSUB    = 0.3564       PCLM    = 4.446           PDIBLC1 = 0
+    PDIBLC2 = 0.00209      PDIBLCB = 0               DROUT   = 0.3564
+    PSCBE1  = 2.65E9       PSCBE2  = 2.75E-8         PVAG    = 0
+    DELTA   = 0.01         MOBMOD  = 1               PRT     = 0
+    UTE     = -1.5         KT1     = 0               KT1L    = 0
+    KT2     = 0            UA1     = 4.30E-9         UB1     = -7.60E-18
+    UC1     = -5.6E-11     AT      = 3.3E4           WL      = 0
+    WLN     = 1            WW      = 0               WWN     = 1
+    WWL     = 0            LL      = 0               LLN     = 1
+    LW      = 0            LWN     = 1               LWL     = 0
+    CAPMOD  = 2            XPART   = 0               CGDO    = 2.4E-10
+    CGSO    = 2.4E-10      CGBO    = 0               CJ      = 7.273568E-4
+    PB      = 0.9665597    MJ      = 0.4959837       CJSW    = 3.114708E-10
+    PBSW    = 0.99         MJSW    = 0.2653654       PVTH0   = 9.420541E-3
+    PRDSW   = -231.2571566 PK2     = 1.396684E-3     WKETA   = 1.862966E-3
+    LKETA   = 5.728589E-3
+    HDIF    = hdifp    )
```

PACKAGE





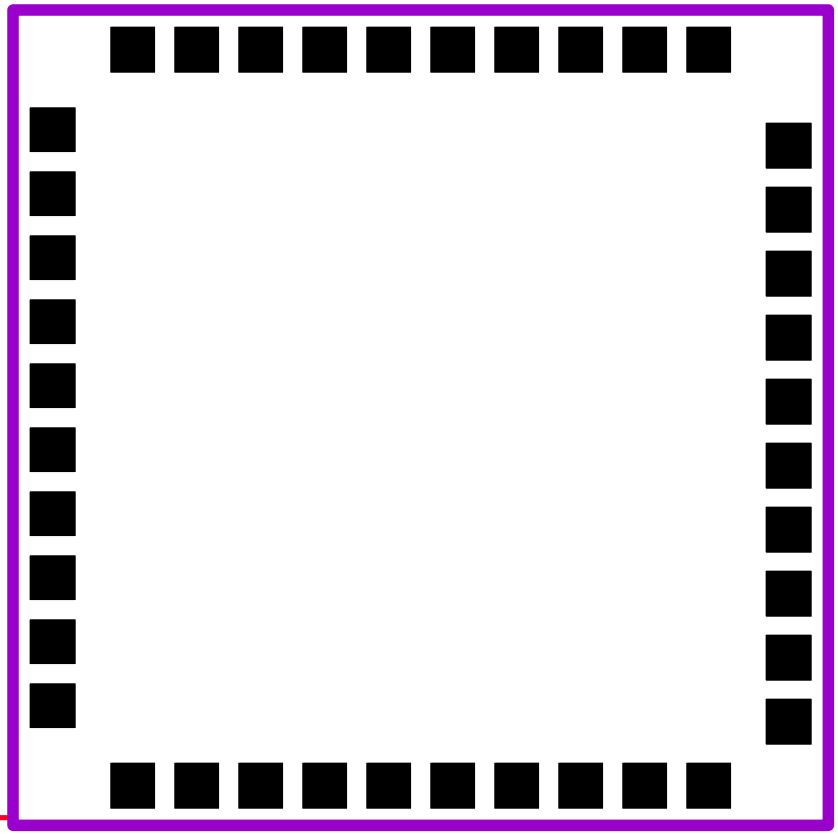


0.10 inch adjacent pin spacing
0.6 inch row spacing

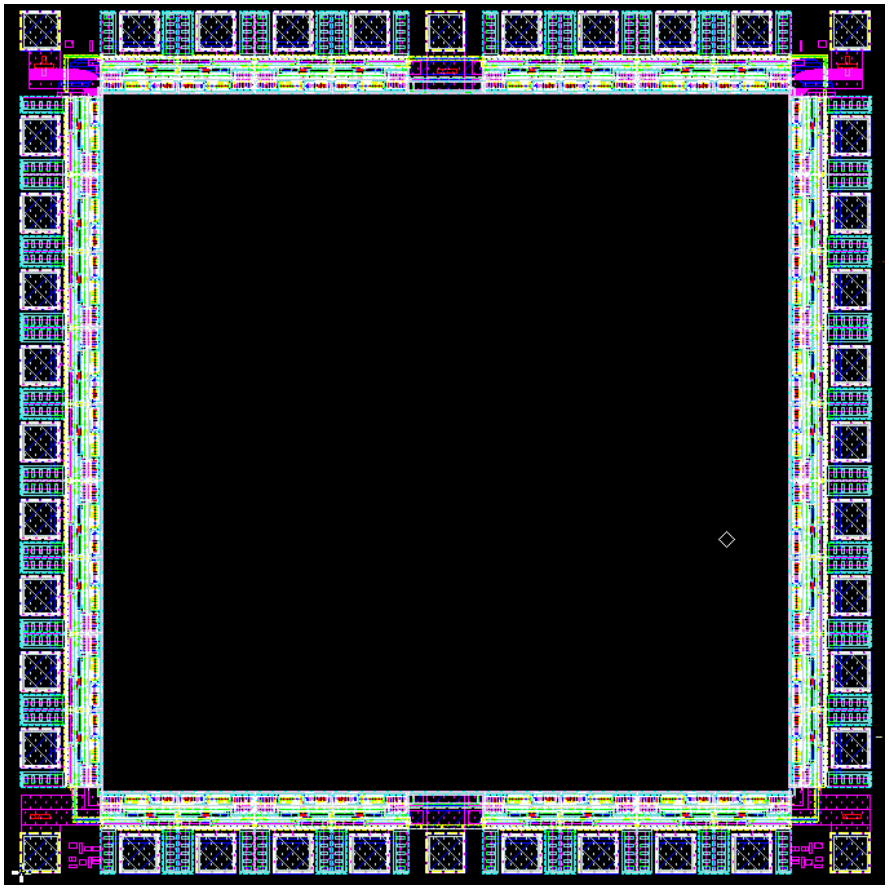
CHIP SIZE AND BOND PAD LOCATIONS

Maximum Chip Size for this Package = 6 mm X 6 mm

Pads on chip should be 10 on each side evenly spaces but not smaller than 100 µm by 100 µm bond pad. Leave plenty of room near the corners

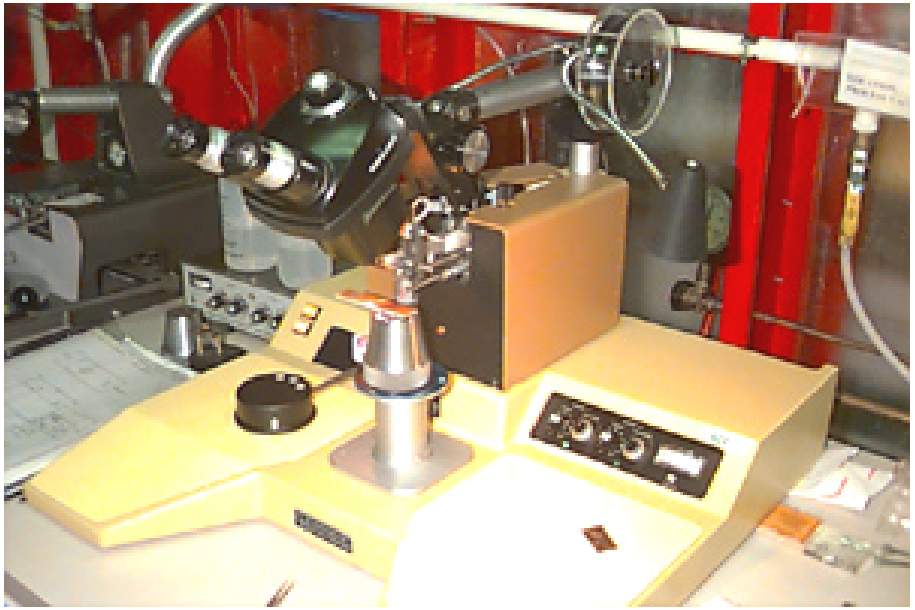


MOSIS TINYCHIP PAD FRAME



/users/class/eecc630/pads/40pc22x22_stuffed/40pc22x22_stuffed
/users/class/eecc630/pads/scna20-pads.doc

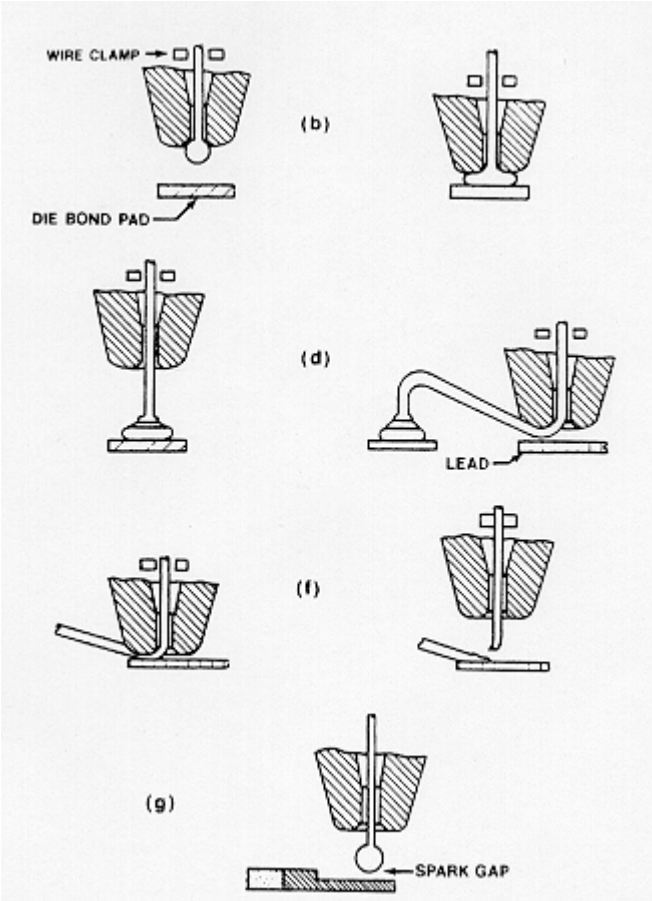
WIRE BONDING

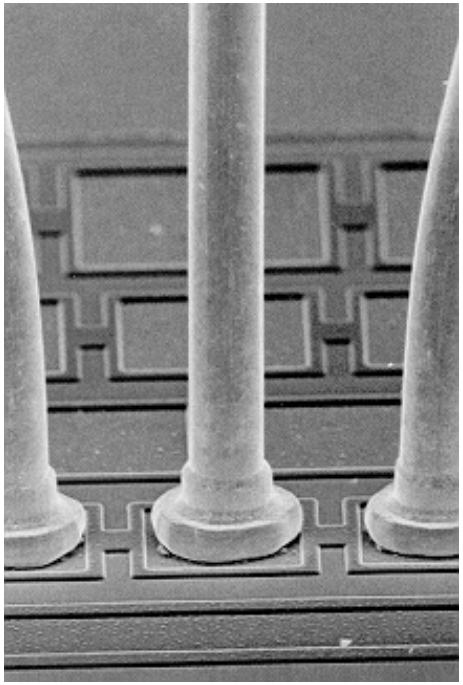


WIRE BONDING

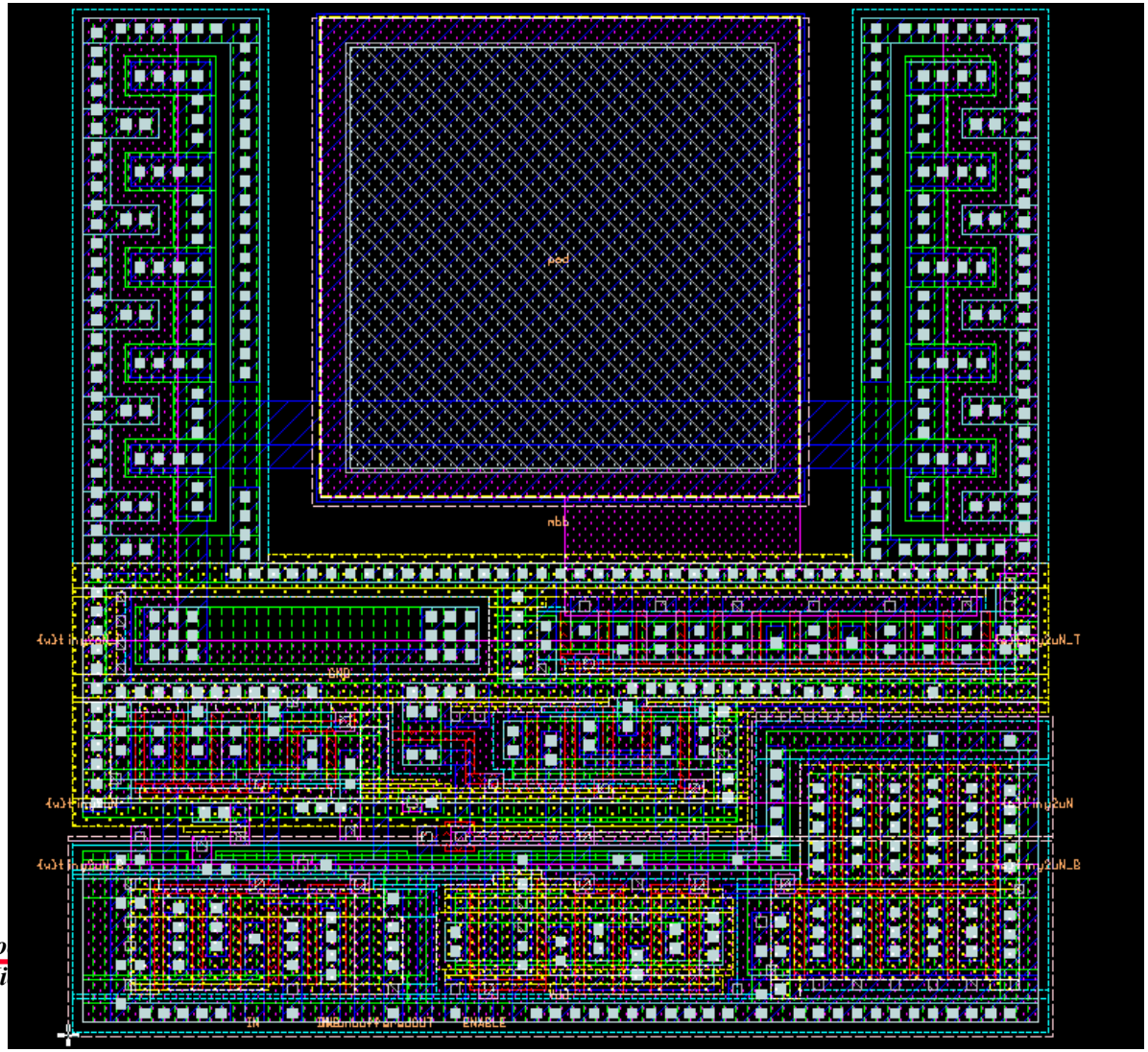
Large diameter gold wire (10 mil) can be ultrasonically bonded to aluminum pads on chips and then can be soldered into a circuit

Smaller diameter aluminum wire (3 mil) can be ultrasonically bonded to aluminum chip pads and then to packages

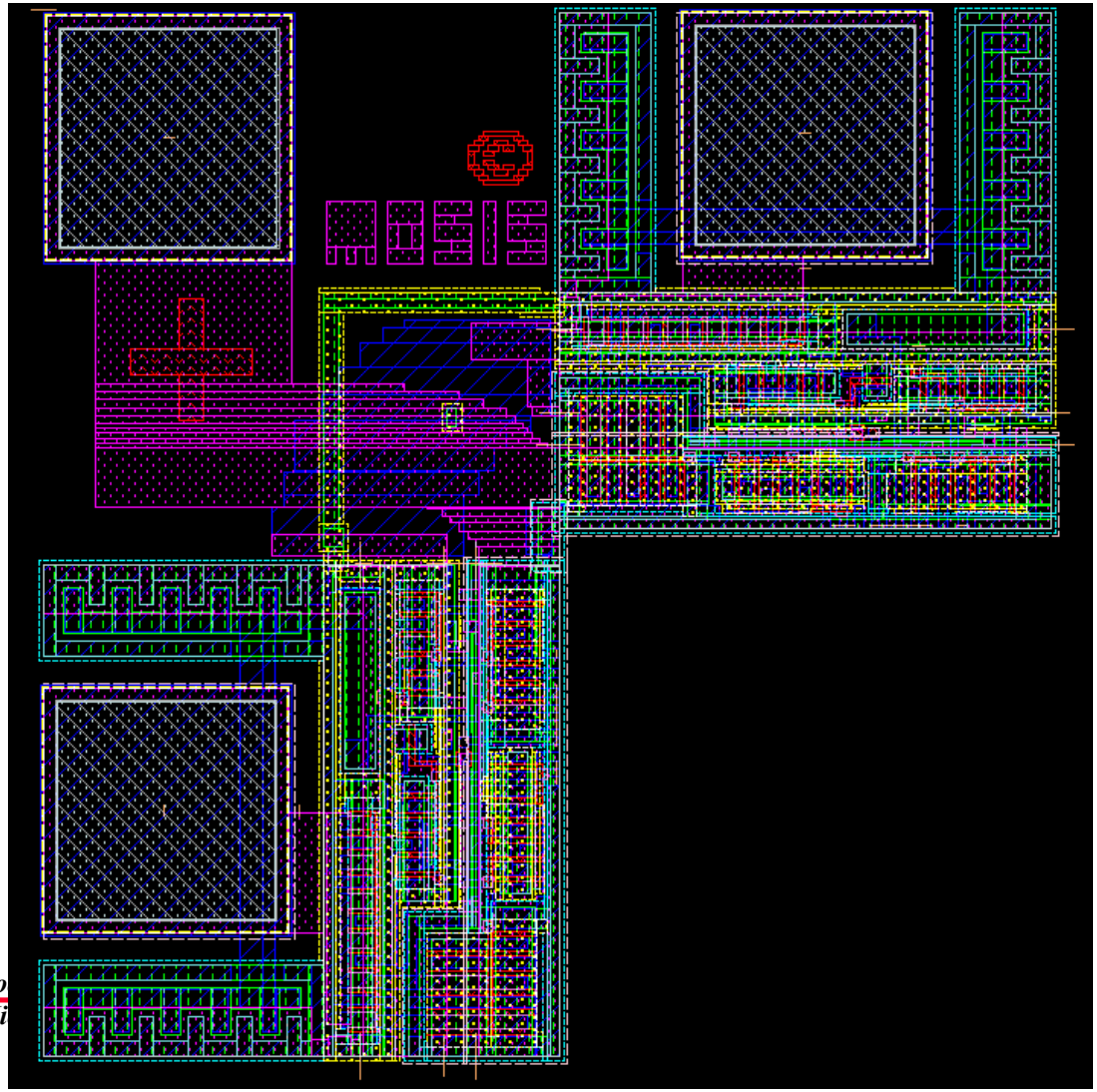




MOSIS I/O PAD CELL



MOSIS +V AND I/O PAD CELLS



TINY CHIP PAD SET

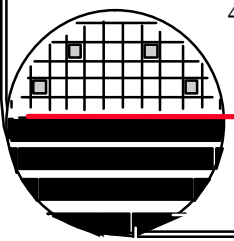
These pads have been validated by the MOSIS System of USC/ISI. Any modification of these pads by the user is done solely at the user's risk. Modified pads are not to be referred to as "MOSIS Pads" unless prior agreement is obtained from USC/ISI.
MOSIS really intends that you use the complete (stuffed) digital or analog pad frames without modification. The individual pads and pad frame subcells are supplied only as a courtesy to those who want to build and verify their own custom pad frames. These pads were not designed to be interchangeable within the pad frame, rather, they were optimized for power and size, and require intricate editing and verification in different arrangements.); TINYCHIP PADS SET, SCN (N-WELL) 2.0 MICRON

1. INTRODUCTION

This 2 micron SCN (N-well) TinyChip pads set was designed with the MOSIS scalable CMOS design rules (Rev 6) at a lambda of 1.0 micron. To use these pads, get the newest Magic technology file (dated on or after than 1/19/93). All pads are laid out on a lambda grid and are designed for use with the 40PC22X22 Standard Frame.

2. CONTENTS OF THE DIGITAL PADS SET

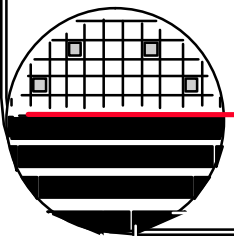
blank.CIF	blank with only bonding metals
gnd.CIF	internal GND power supply - not connected to pad GND
vdd.CIF	internal Vdd power supply - not connected to pad Vdd
in.CIF	input pad - a derivative from I/O pad
io.CIF	input/output pad
out.CIF	output pad - a derivative from I/O pad
cg.CIF	GND Bottom Left corner pad
CG_r.CIF	GND Bottom Right corner pad
cv.CIF	Vdd Top Left corner pad
cv_r.CIF	Vdd Top Right corner pad
40pc22x22_stuffed.CIF	contains a complete io pad ring layout in size 220x2250 um



TINY CHIP PAD SET

DESCRIPTION:
The single most important pad in this pad set is the IO pad. From this tri-state I/O pad we derived the IN pad and the OUT pad. A circuit diagram for this tri-state I/O pad is given below. Connecting ENABLE to GND will turn this I/O pad into an input pad. Connecting ENABLE to Vdd will result an output pad.

ESD protection is done with
(1) Thick-Field Oxide transistor of size W/L= 600/3 microns,
(2) 150 ohms N_diffusion resistor/diode, and
(3) Tri-state output drivers as pair of diode clamps.



TINY CHIP PAD SET

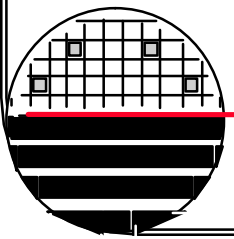
These pads should fit into the standard frame 40PC22x22 with mirroring. They can also be used for other MOSIS standard frames. io, in, out, Vblank, vdd, and gnd has none-well maximum bonding box (MBB) of 200x210 microns each. The well MBB is 210x218 microns. The stuffed frame has a non-well MBB of 2220x2250 microns. There are 9 pads on each edge plus 4 corners used as Vdd and GND pads. The top edge has a GND pad in the middle and its 2 corners are Vdd pads, while the bottom edge has a Vdd pad in the middle and its 2 corners are GND pads. This gives 3 Vdd and 3 GND pads total.

3. CONTENTS OF THE ANALOG PADS SET

gndN.CIF	internal GND power supply - not connected to pad GND
vddN.CIF	internal Vdd power supply - not connected to pad Vdd
analogN.CIF	analog input/output pad
llN.CIF	GND Bottom Left corner pad
urN.CIF	Vdd Top Right corner pad
40pc22x22_stuffed_analog.CIF	contains a complete io pad ring layout in size 2220x2250 um

* Description

ESD protection is achieved by two lateral PNP parasitic transistor in N-well
(1) reverse biased diode connected to Vdd when a positive ESD stress is applied.
(2) PNP transistor from GND to input when a negative ESD stress is applied.



TINY CHIP PAD SET

4. SIMULATION and MEASUREMENT

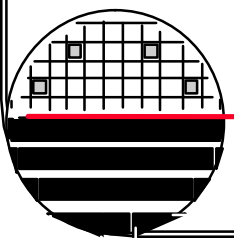
Both pad set have been fabricated by MOSIS for verification, but only pads in digital set are simulated and measured. Their result are listed as follows:

* Delay OUTPUT Driver Load (SIMULATED)

	10pF	30pF	50pF
rise time	8ns	21ns	30ns
fall time	7ns	17ns	25ns

OUTPUT Driver Load (MEASURED)

	no load	10pF	22pF	47pF
prop. delay (0 to 1)	8.6ns	10.8ns	13.0ns	18.5ns



TINY CHIP PAD SET

INPUT Driver Load (SIMULATED)

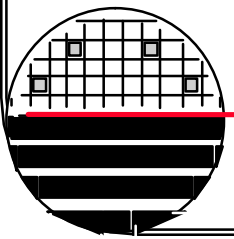
signal	signal	load: INbar/IN 0.5/1pF prop/rise/fall delay/time/time	INbar/IN prop/rise/fall	load: INbar/IN 1/2pF prop/rise/fall delay/time/time	load: 2/4pF delay/time/time
PAD	INbar	1.1/3.9/2.0	1.6/5.5/3.0	2.2/8.5/4.5	
INbar	IN	2.2/3.0/2.2	2.2/5.0/3.5	3.8/8.5/6.5	

* DC Current Capability

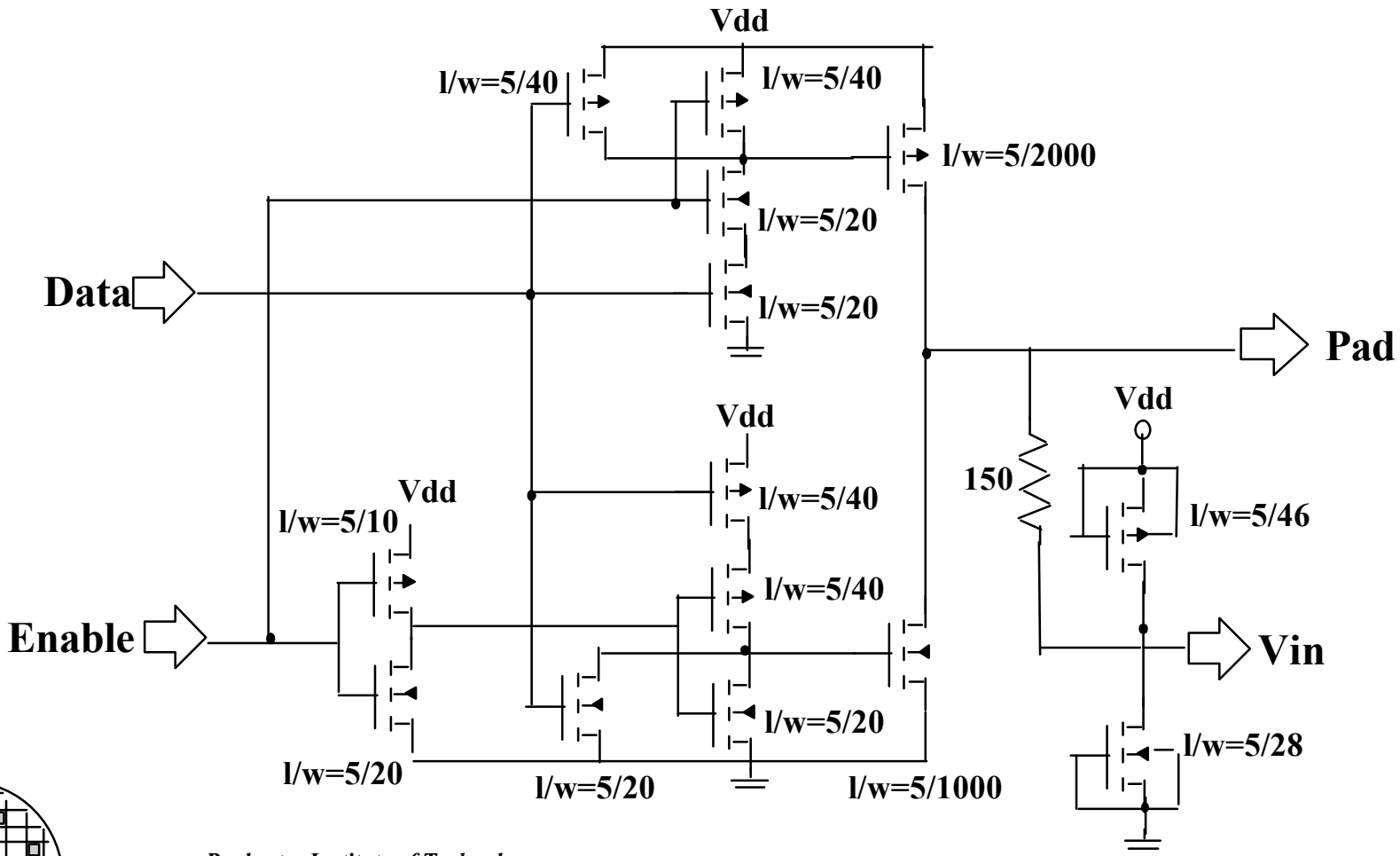
Maximum current :: 11 mA per I/O pad with 50pF loading

5. Magic CIF input

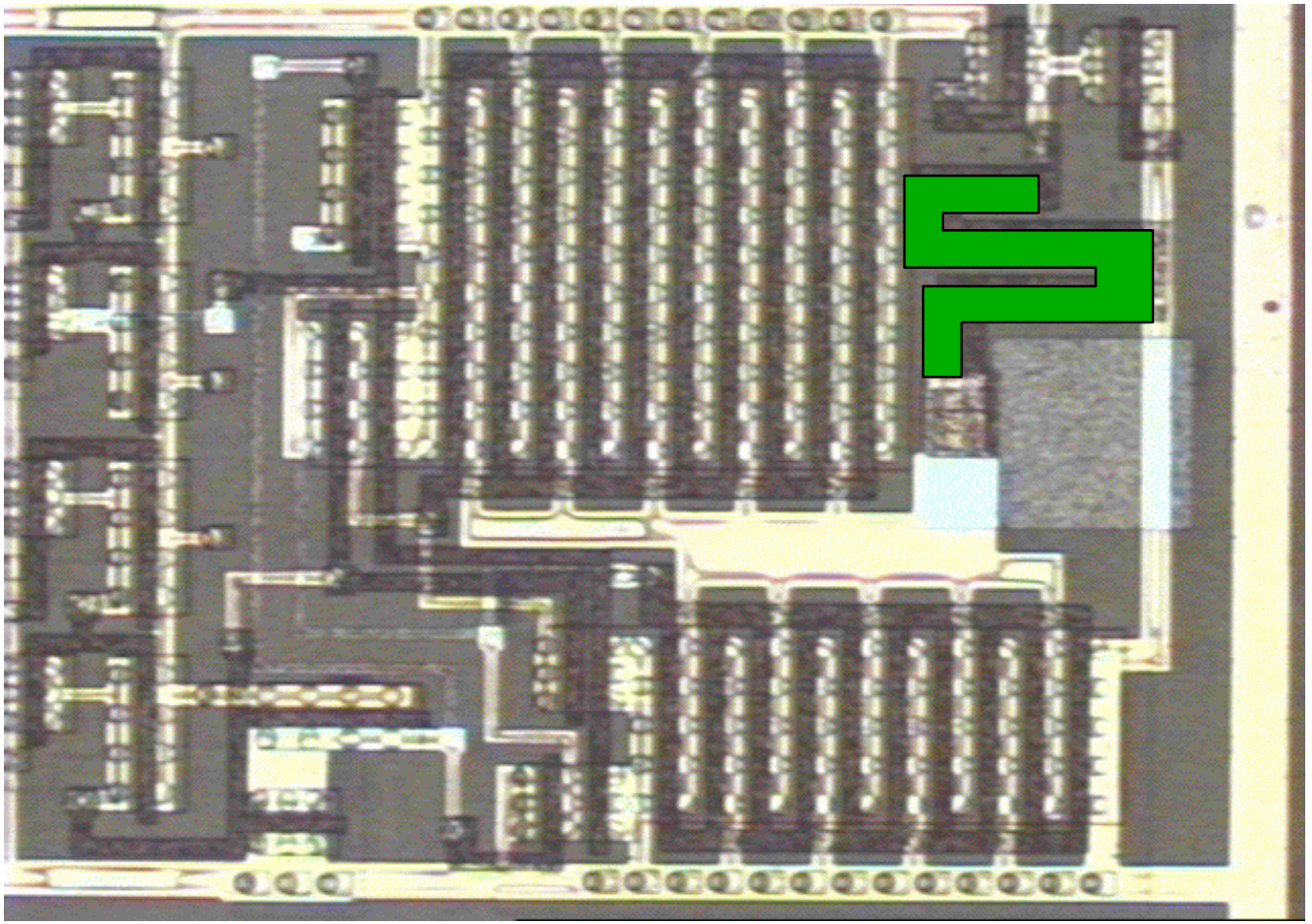
In Magic, Berkeley's layout editor, use ":cif is lambda=1.0(nwell)“ to specify the appropriate CIF input style before using ":cif read ..." command.



KODAK-RIT I/O CELL SCHEMATIC



KODAK-RIT I/O CELL LAYOUT



ESD PROTECTION

§ANALOG IO PADS

Adapted from AMI

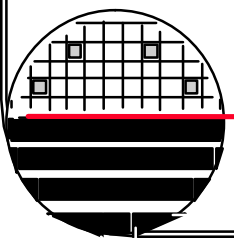
- §Ground/Power pad
- §Analog Reference Pad
- §IO Pad

0.5um High ESD Library

§DIGITAL IO PADS

ESD protection

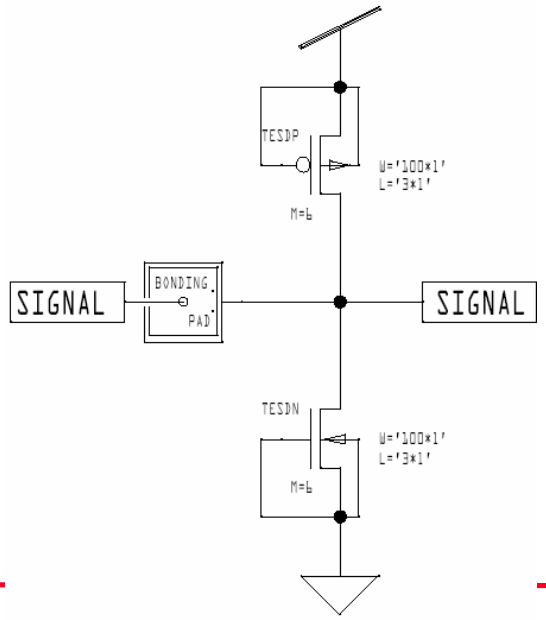
- –Field transistor
- –150 ohm



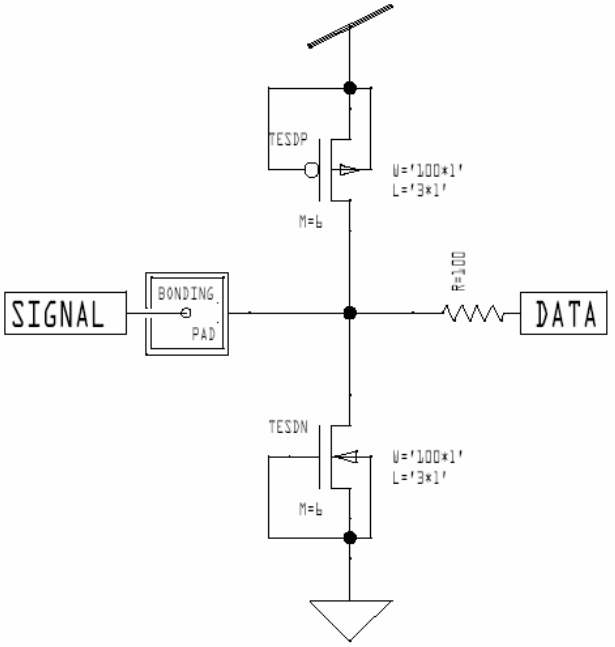
PADS

Tanner CES	mAMI05P – MOSIS AMI 0.5µm Hi-ESD Pad Cell Library	Rev. A PADIO

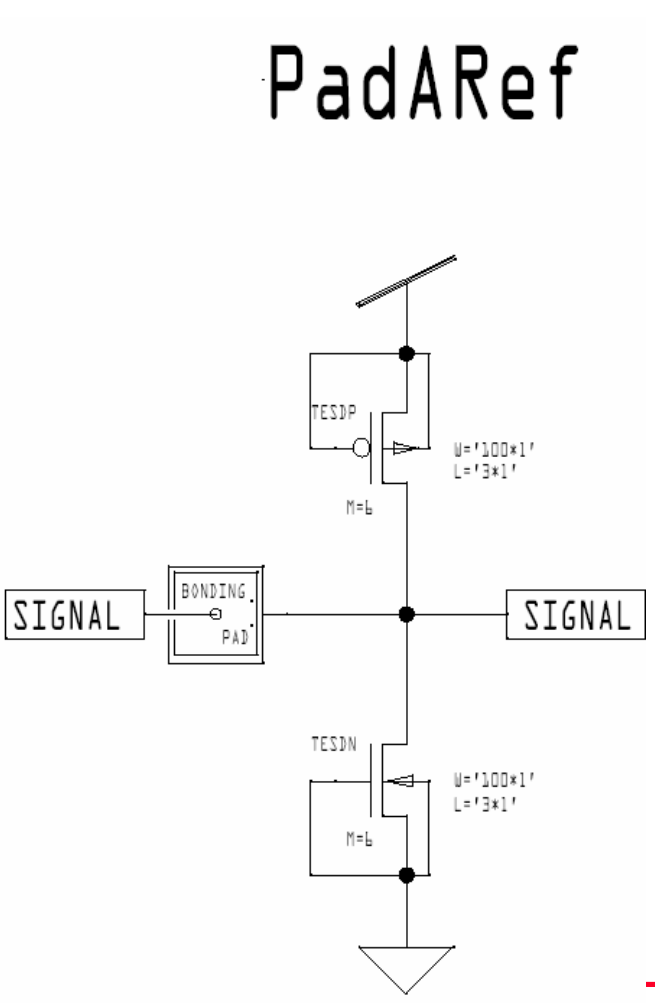
PadARef

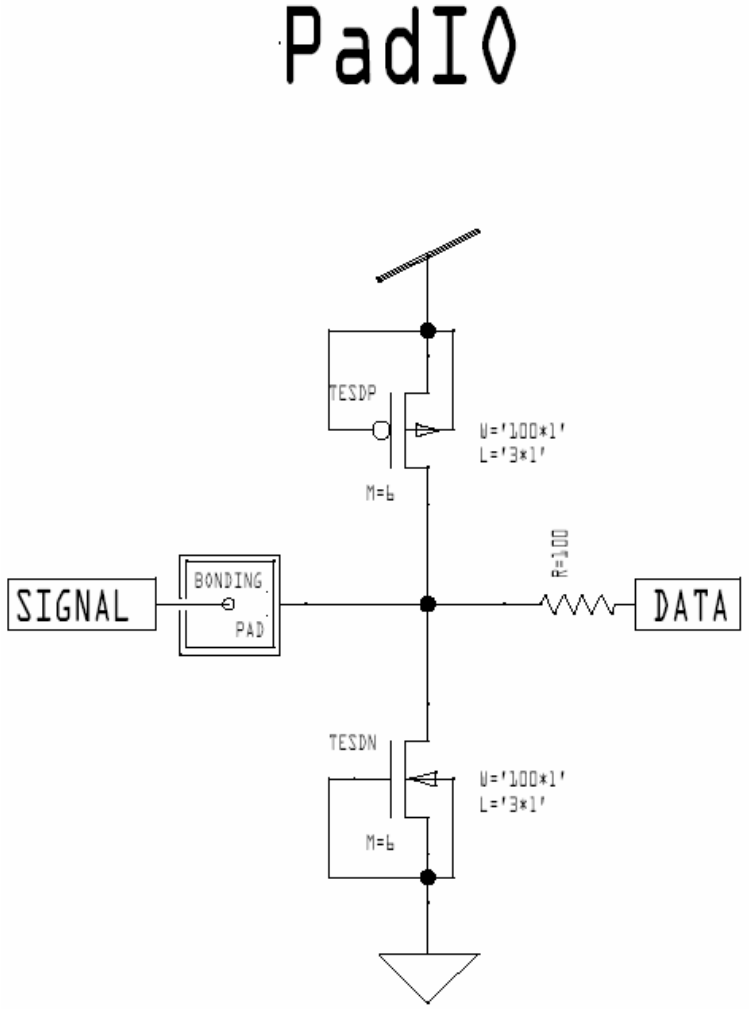


PadIO

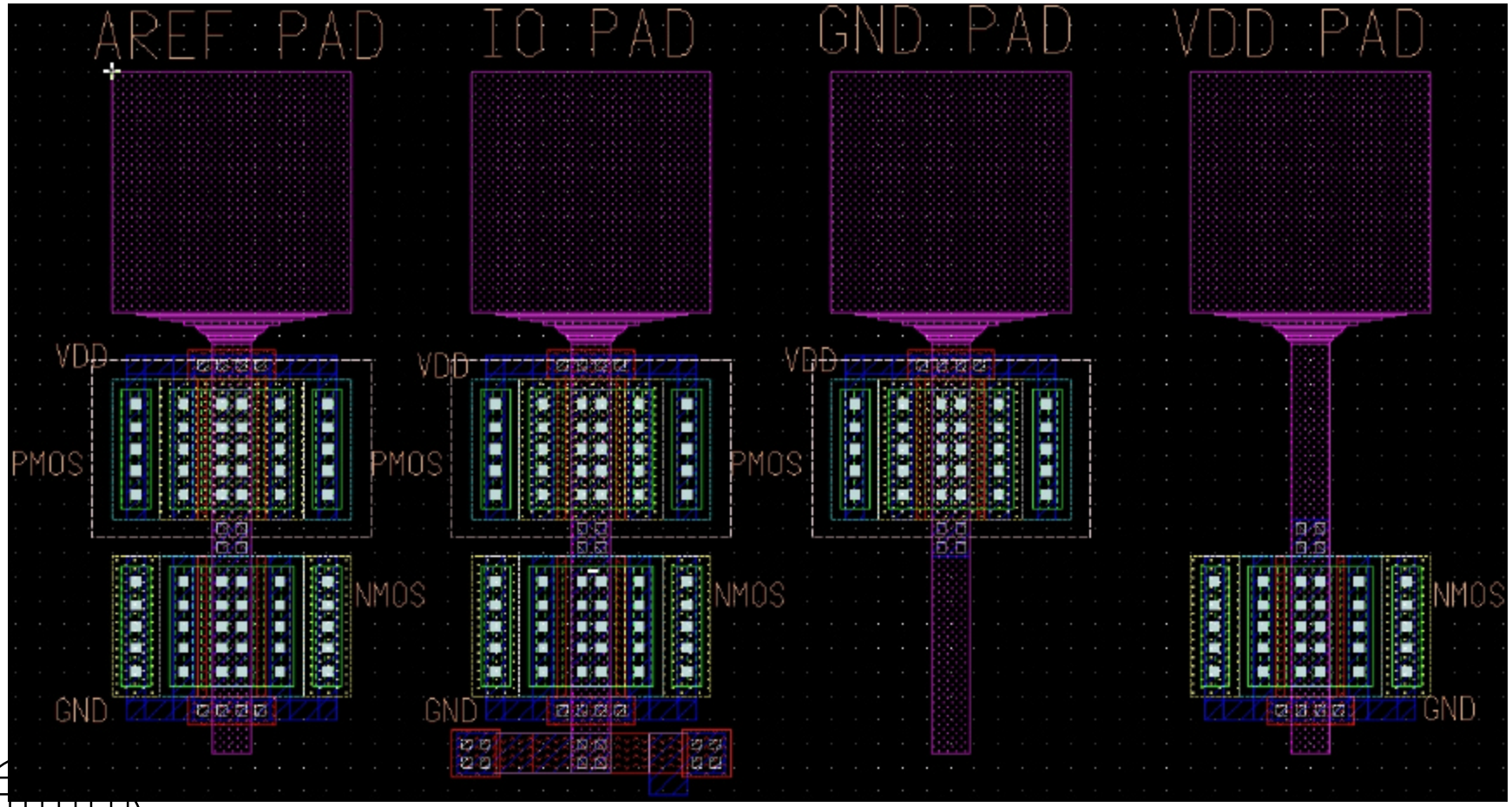


PADS

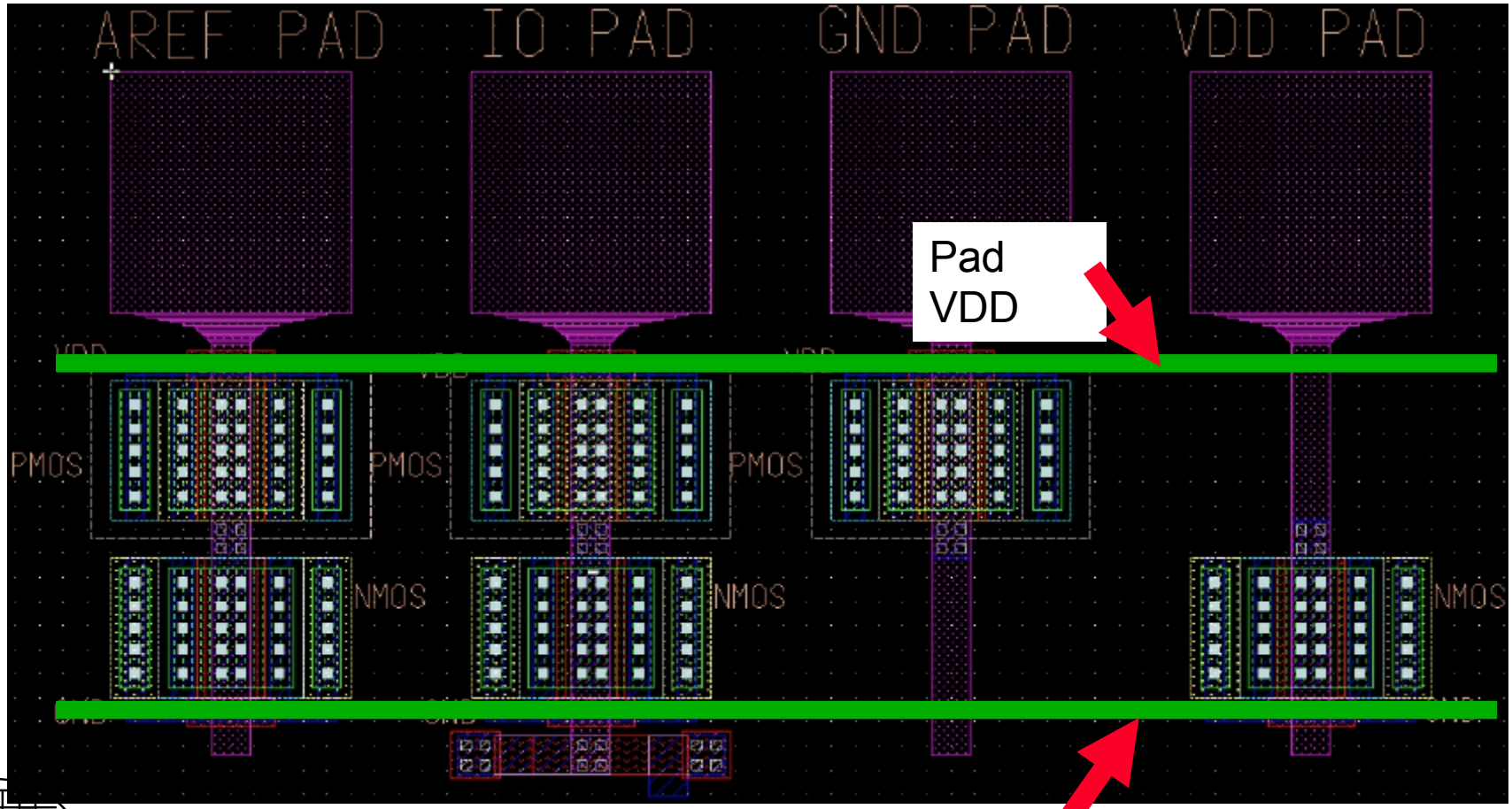

PadARef
TESDP
W='100*1'
L='3*1'
M=6
SIGNAL
BONDING
PAD
SIGNAL
TESDN
W='100*1'
L='3*1'
M=6


PadI0
TESDP
W='100*1'
L='3*1'
M=6
R=100
SIGNAL
BONDING
PAD
DATA
TESDN
W='100*1'
L='3*1'
M=6

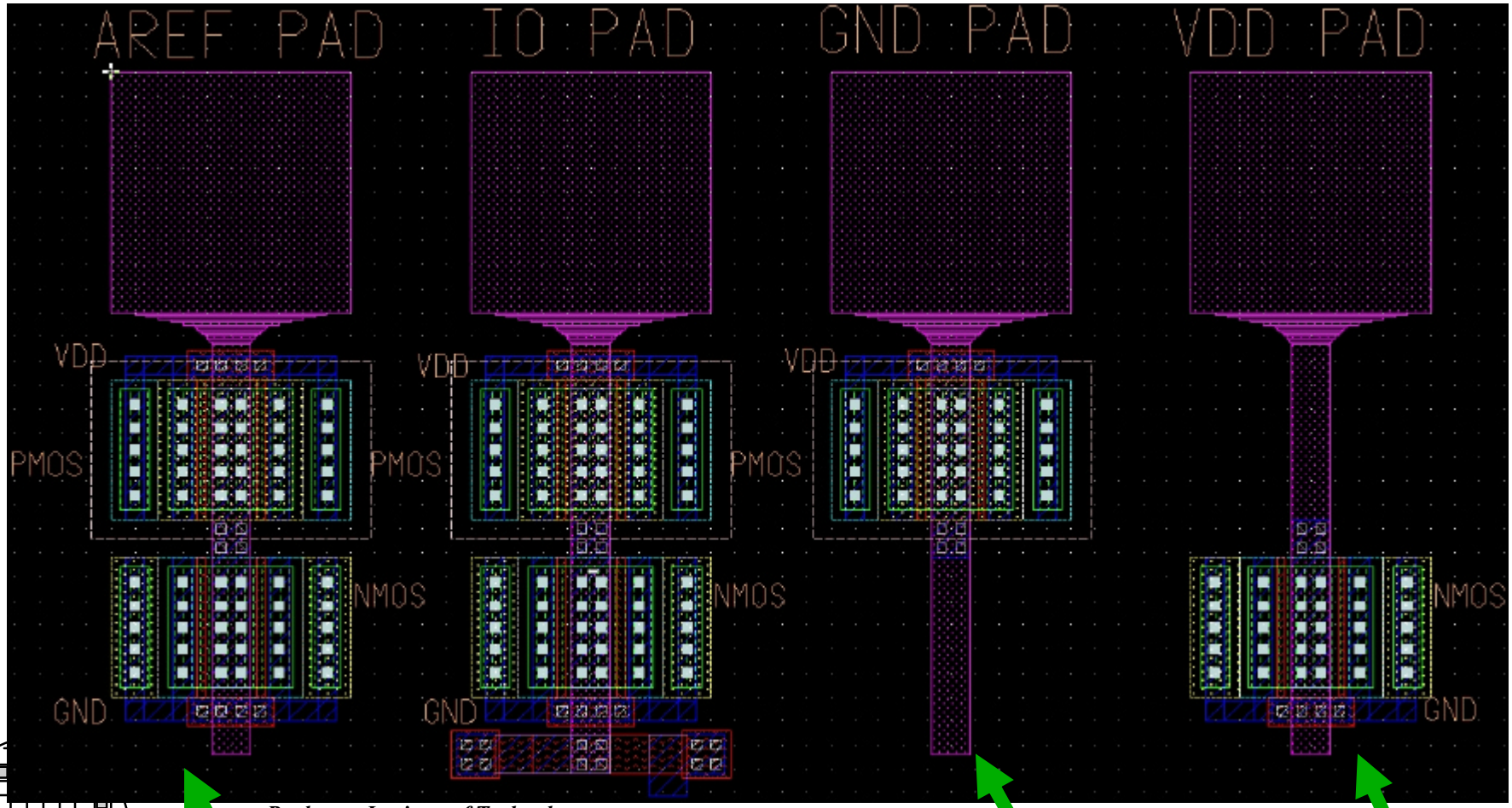
PAD LAYOUT



PAD POWER HOOKUP



CHIP HOOKUP



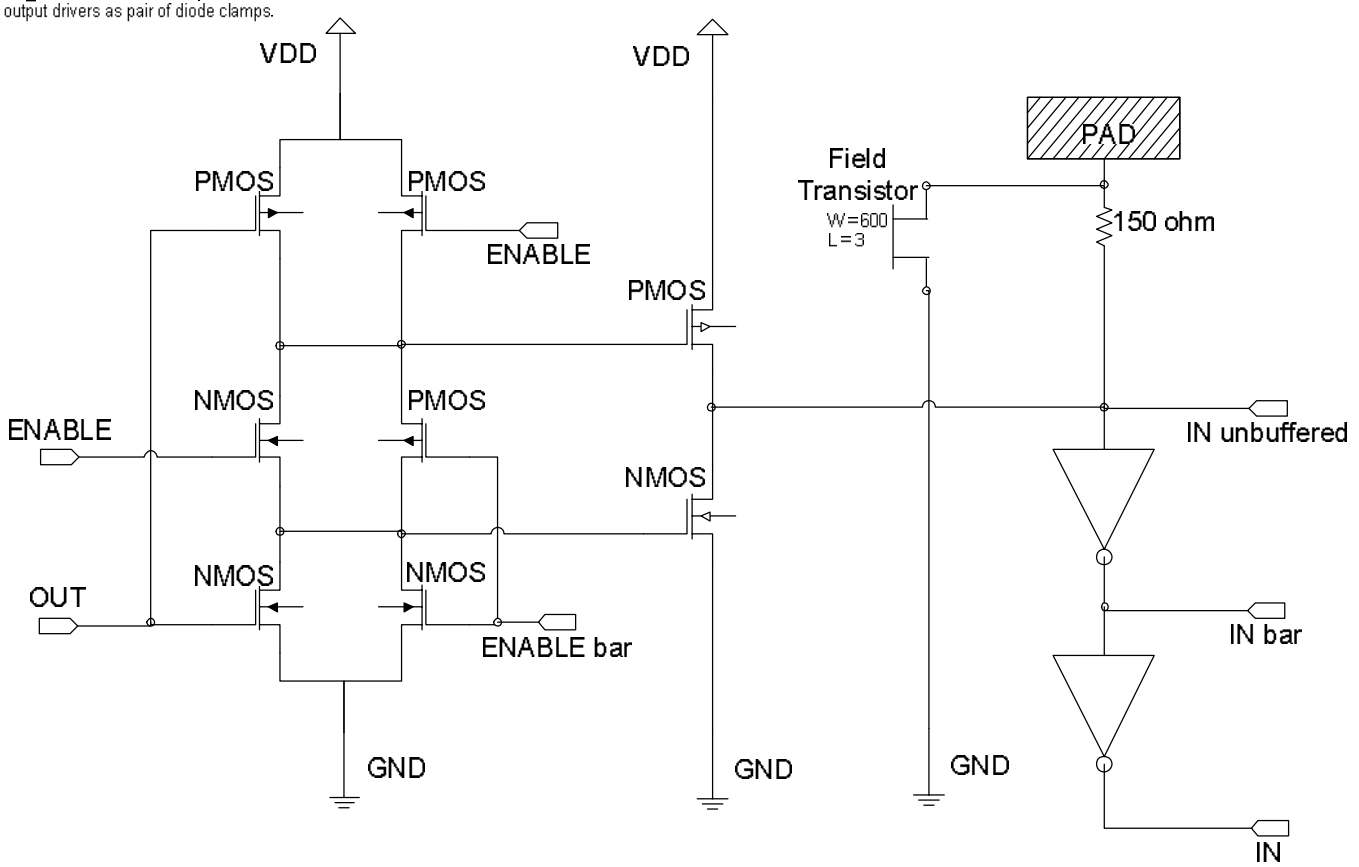
DIGITAL I/O PAD CIRCUIT

From this tri-state I/O pad we derived the IN pad and the OUT pad. A circuit diagram for this tri-state I/O pad is given below. Connecting ENABLE to GND will turn this I/O pad into an input pad. Connecting ENABLE to Vdd will result an output pad.

ESD protection is done with
(1) Thick-Field Oxide transistor of size WxL=600/3 microns,
(2) 150 ohms N_diffusion resistor/diode, and
(3) Tri-state output drivers as pair of diode clamps.

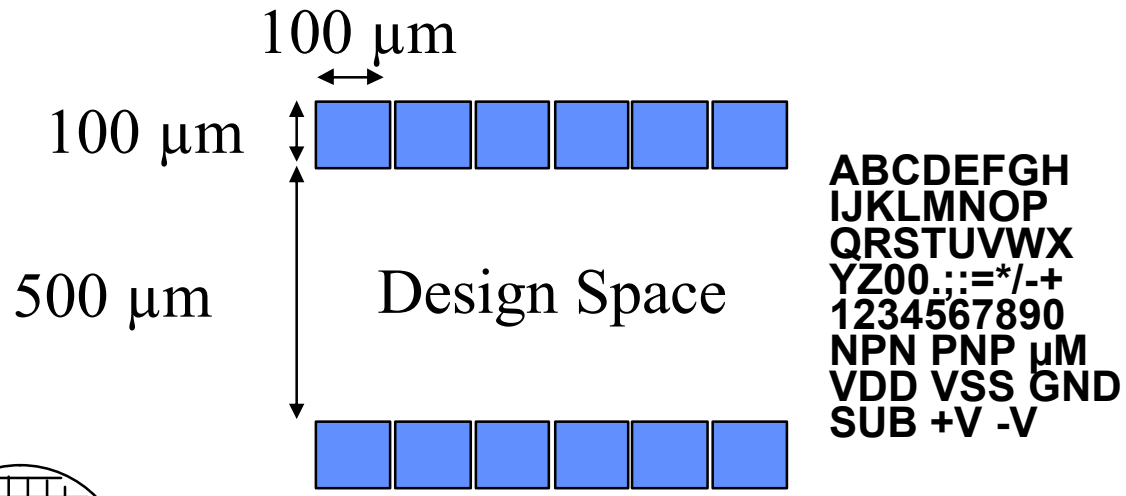
MOSIS DIGITAL I/O PAD

ROBERT SAXER
05/05/2004



USING THE HP WORKSTATIONS AND MENTOR GRAPHICS CAD TOOLS - PAD CELL AND LETTERS

From the banner at the top of the page choose Objects>add>cell. A tan pop-up window will appear at the bottom of the page. Type in the following cell name, all lower case, /tools/ritpub/padframes/ritpmos/ritpmos_12_pads and click the left mouse button on the location button. Then position the cursor at the origin 0,0 and click the left mouse button. Click the left mouse button on the cancel button on the tan pop-up box. Press SHIFT and F8 to View All. You should see a white box with ritpmos_12_pads written inside it. Type flatten and select, OK. Press F2 to unselect all.



REFERENCES

1. Principles of CMOS VLSI Design, Neil Weste, Kamran Eshraghian, Addison-Wesley Publishing Co. , 1993.
2. Introduction to VLSI Systems, Carver Mead, Lynn Conway, Addison-Wesley Publishing Co. , 1980.
3. Proceedings of the IEEE Custom Integrated Circuits Conference.
4. CMOS Analog Circuit Design, Phillip E. Allen and Douglas R. Holberg, Holt, Rinehart and Winston Publishers, 1987.
5. MOSIS Scalable Design Rules, Revision 7.2, dr-scmos721.pdf
6. MOSIS Scalable CMOS Design Rules for Generic CMOS Proc esses, Information Sciences Institute, University of Southern Ca lifornia, 4676 Admiralty Way, Marina del Rey, CA 90292, pi@isi.edu, April 15, 1995. www.mosis.org