The University of Alabama in Huntsville
Electrical and Computer Engineering
Course Syllabus
CPE 628 01
Fall 2008

Textbook:	VLSI Test Principles and Architectures, Laung-Terng Wang, Cheng-Wen Wu and Xiaoquing Wen, Morgan Kaufmann Publishers, 2006
Web Page:	http://www.ece.uah.edu/courses/cpe628
Instructor:	Dr. Rhonda Kay Gaede, Office: EB 211, Phone: 824-6573, email: gaede@ece.uah.edu
Office Hours:	M 10:00 AM – 12:00 PM, W 2:00 PM – 4:00 PM, T 11:00 AM – 12:00 PM, F 2:00 PM – 3:00 PM, or by appointment
Grading:	Homework 25 % Tests(2) 40 % Final Exam 35 %
Homework:	NO late homework will be accepted without extenuating circumstances. Contact me as soon as a problem occurs.
Important Dates:	August 22 – Last day to add a class August 29 – Last day to withdraw with refund September 1- Holiday September 8– Last day to apply for Pass/Fail September 15 – Last day to change from credit to audit October 6 – Midterm October 9-11 – Fall Break October 29 - Last day to withdraw November 3 - Registration for Spring 2009 begins November 25 – Last TR class
Final Exam:	Thursday, December 4, 6:30 PM – 9:00 PM
Miscellaneous:	Mute your cell phones before you bring them to class.

Course Outline:

Chapter Topics

1 Introduction

Importance of Testing, Testing During the VLSI Lifecycle, Challenges in VLSI Testing, Levels of Abstraction in VLSI Testing, Historical Review of VLSI Test Technology

2 Design for Testability

Testability Analysis, Design for Testability Basics, Scan Cell Designs, Scan Architectures, Scan Design Rules, Scan Design Flow, Special-Purpose Designs, RTL Design for Testability

3 Logic and Fault Simulation

Simulation Models, Logic Simulation, Fault Simulation

4 Test Generation

Random Test Generation, Theoretical Background: Boolean Difference, Designing a Stuck-At ATPG for Combinational Circuits, Designing a Sequential ATPG, Untestable Fault Identification, Designing a Simulation-Based ATPG, Advanced Simulation-Based ATPG, ATPG for Non-Stuck-At Faults, Other Topics in Test Generation

5 Logic Built-In Self-Test

BIST Design Rules, Test Pattern Generation, Output Response Analysis, Logic BIST Architectures, Fault Coverage Enhancement, BIST Timing Control, A Design Practice

8 Memory Testing and Built-In Self-Test

RAM Functional Fault Models and Test Algorithms, RAM Fault Simulation and Test Generation Algorithm, Memory Built-In Self-Test

10 Boundary Scan and Core-Based Testing

Digital Boundary Scan (IEEE Std. 1149.1), Boundary Scan for Advanced Networks (IEEE Std. 1149.6), Embedded Core Test Standard (IEEE Std. 1500), Comparisons between the 1500 and 1149.1 Standards

Possible Coverage

6 Test Compression

Test Stimulus Compression, Test Response Compaction, Industry Practices

7 Logic Diagnosis

Combinational Logic Diagnosis, Scan Chain Diagnosis, Logic BIST Diagnosis

9 Memory Diagnosis and Built-In Self-Repair

Refined Fault Models and Diagnostic Test Algorithms, BIST with Diagnostic Support, RAM Defect Diagnosis and Failure Analysis, Built-In Self-Repair

11 Analog and Mixed-Signal Testing

Analog Circuit Properties, Analog Circuit Testing, Mixed-Signal Testing, IEEE 1149.4 Standard for a Mixed-Signal Test Bus

12 Test Technology Trends in the Nanometer Age

Test Technology Roadmap, Delay Testing, Coping with Physical Failures, Soft Errors, and Reliability Issues, FPGA Testing, MEMS Testing, High-Speed I/O Testing, RF Testing

I promise or affirm that I will not at any time be involved in cheating, plagiarism, fabrication, misrepresentation, or any other form of academic misconduct as outlined in the UAH Student Handbook wile I am enrolled as a student at UAH. I understand that violating this promise will result in penalties as severe as indefinite suspension from the University of Alabama in Huntsville.

Name (Printed)	Signature	Date