



## EECS 42 – Introduction to Electronics for Computer Science

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Dept. EECS,  
UC Berkeley  
Course Web Site <http://www-inst.EECS.Berkeley.EDU/~ee42/>

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Tentative OH M, Tu, W, (Th), F 11

### Solutions Midterm #2 November 7th, 2001

**Closed Book, Closed Notes**  
**Write on the Exam paper**

**Print Your Name:** \_\_\_\_\_

**Sign Your Name:** \_\_\_\_\_

**Show your work so that the method as well as the answer can be graded for correctness and completeness. Correct answers alone are only worth 70% of full credit.**

Problem	Possible	Score
I	30	
II	25	
III	22	
IV	23	
Total	100	

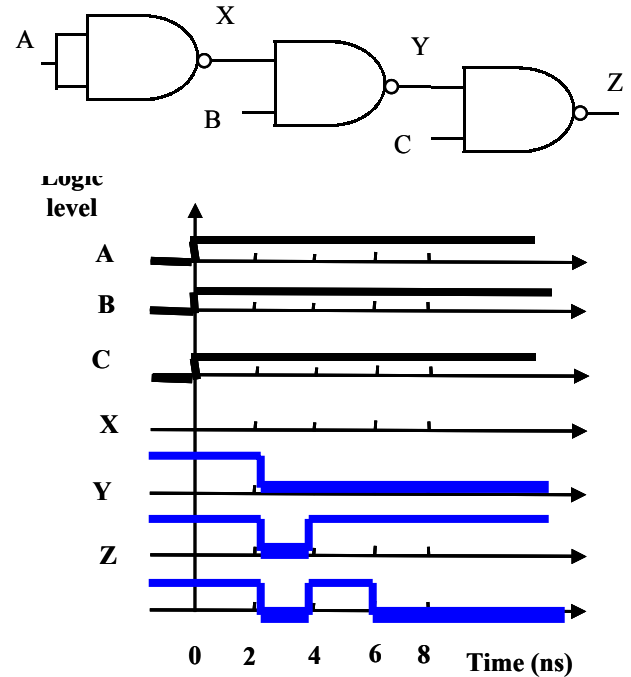
## I (30 Points) Logic and Timing Diagrams

Inputs A, B, and C have all been zero (low) for a long time and then at  $t = 0$ , A, B and C go to (high) for a long time.

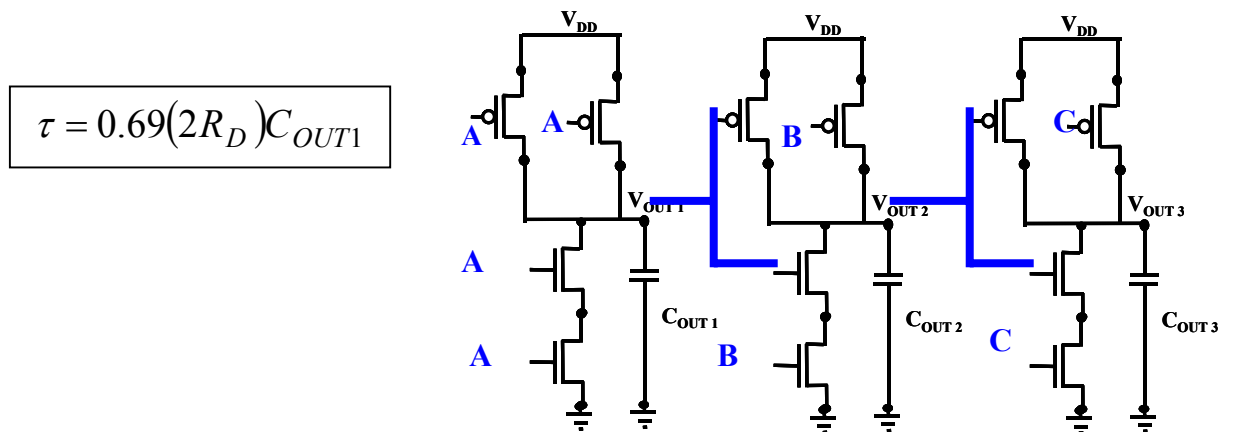
- a) (5 Points) Find the values of X, Y and Z just before  $t = 0$ , and then as  $t$  goes to infinity.

	Before $t=0$	As $t \Rightarrow$ infinity
X	1	0
Y	1	1
Z	1	0

- b) (10 points) Complete the timing diagram to the right assuming that each gate has a propagation delay of 2 ns before the correct output appears at its output.



- c) (7 Points) For the CMOS circuit implementation to the right of the NAND gate logic circuit above and the signal changes in part a), **find the time at which the change reaches  $V_{OUT1}$** . State the delay in terms of  $0.69RC$  using  $R_U$  and  $R_D$  (from the switched resistor device models) and the capacitors shown.



$$\tau = 0.69(2R_D)C_{OUT1}$$

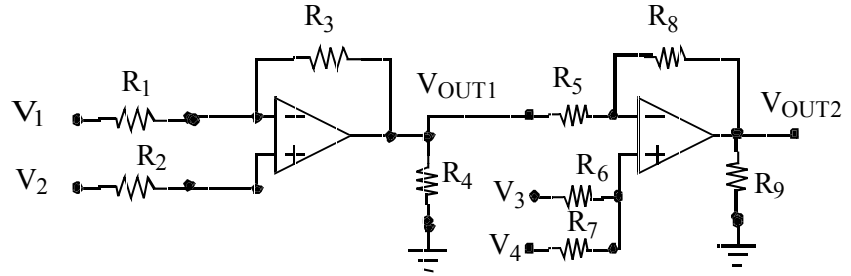
- d) (10 points) (8 Points) For the CMOS circuit implementation to the right of the NAND gate logic circuit above and the signal changes in part a), **find the time at which the change reaches  $V_{OUT3}$** . State the delay in terms of combinations of  $0.69RC$  using  $R_U$  and  $R_D$  (from the switched resistor device models) and the capacitors shown.

$$\tau = 0.69(2R_D)C_{OUT1} + 0.69(R_U)C_{OUT2} + 0.69(2R_D)C_{OUT3}$$

## II (25 Points) Ideal Op-Amp Analysis

Use the ideal op-amp analysis method in this problem.

- a) (8 Points) Find  $V_{OUT1}$  in terms of the resistances and input voltages.



$$\frac{(V_1 - V_2)}{R_1} + \frac{(V_{OUT1} - V_2)}{R_3} = 0$$

$$V_{OUT1} = V_2 + \frac{R_3}{R_1} (V_2 - V_1)$$

- b) (9 Points) Give sufficient additional equations for finding  $V_{OUT2}$  in terms of the resistances and input voltages. Do not solve.

$$V_{+2} = V_4 + (V_3 - V_4) \frac{R_7}{R_6 + R_7}$$

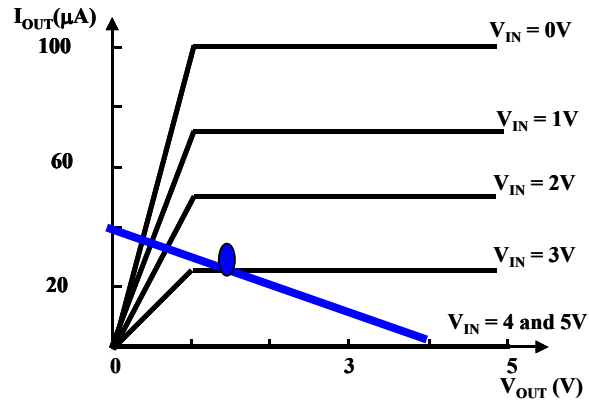
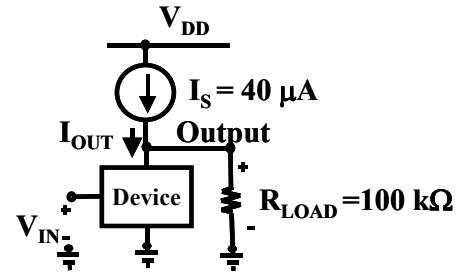
$$V_{OUT2} = V_{+2} + \frac{R_8}{R_5} (V_{+2} - V_{OUT1})$$

- c) (8 Points) Assume that  $V_{OUT2} = k_1 V_1 + k_2 V_2 + k_3 V_3 + k_4 V_4$ . For  $i = 1, 4$  complete the table below by determining the sign of  $k_i$  and listing the resistors that will contribute to  $k_i$ . Hint: Start with what you know from part a) to reach  $V_{OUT1}$  and then apply this principle again.

Term	Sign	Contributing Resistors
V1	+	<b>R1, R3, R5, R8</b>
V2	-	<b>R1, R3, R5, R8</b>
V3	+	<b>R5, R6, R7, R8</b>
V4	+	<b>R5, R6, R7, R8</b>

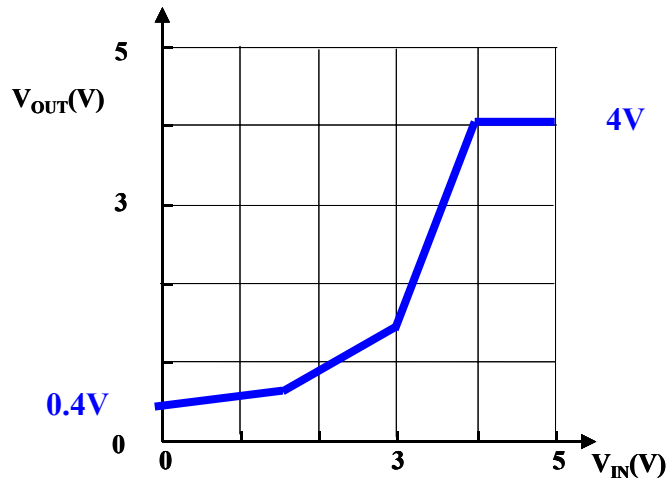
### III (22 Points) Device I vs. V Curves

- a) (10 Points) For the logic circuit and device characteristics shown find  $V_{OUT}$  when  $V_{IN} = 3V$ .



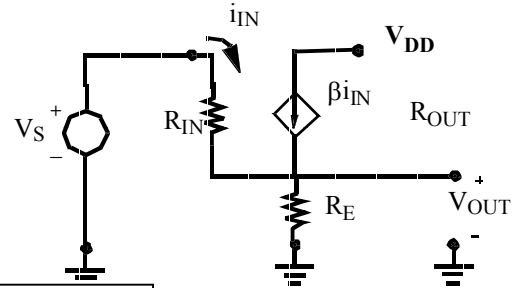
$V_{oc} = 40 \mu A \times 100k \text{ ohms} = 4V$   
 $I_n = 40 \mu A$   
 Intersection with  $V_{in} = 3V$  at  
 $V_{out} = 1.5V$

- b) (12 Points) For the logic circuit shown approximately sketch the voltage transfer function  $V_{OUT}$  vs.  $V_{IN}$ . Specify values of  $V_{OUT}$  for  $V_{IN} = 0, 3$  and  $5V$ .



## IV (23 Points) Advanced Circuits with Dependent Sources

a) (10 Points) Find  $V_{OUT}/V_{IN}$ .



Node equation (KCL) at the output node.

$$i_{IN} + \beta i_{IN} + \frac{(0 - V_{OUT})}{R_E} = 0$$

$$i_{IN} = \frac{(V_S - V_{OUT})}{R_{IN}}$$

Substitute

$$(\beta + 1) \frac{(V_S - V_{OUT})}{R_{IN}} + \frac{(0 - V_{OUT})}{R_E} = 0$$

Rearrange

$$V_{OUT} = \frac{(\beta + 1)R_E}{(R_{IN} + (\beta + 1)R_E)} V_S$$

=> Gain is less than but close to 1 so the output follows the input.

b) (13 Points) Find the Thevenin resistance looking into the output.

$$i_{OUT} = \frac{V_{OUT}}{R_{IN}} + \frac{V_{OUT}}{R_E} - \beta i_{IN}$$

$$i_{IN} = -\frac{V_{OUT}}{R_{IN}}$$

$$i_{OUT} = \left( \frac{1}{R_E} + \frac{(\beta + 1)}{R_{IN}} \right) V_{OUT}$$

=> sees  $R_E$  in parallel with  $R_{IN}/(\beta + 1)$  which is a low output impedance

Looking in the output  $R_E$  and  $R_{IN}$  are in parallel and current flows backward through  $R_{IN}$ . However the dependent source draws  $\beta$  times more current than goes backward through  $R_{IN}$  and by drawing a current proportional to the conductance of  $R_{IN}$  it increases the conductance and reduces the resistance by a factor of  $(\beta + 1)$ . It is a form of a current supply that sucks in additional current.