University of California, Santa Cruz
Board of Studies in Computer Engineering
CMPE-100 Spring-2001

Final Exam

S.C. Petersen
7 June 2001 8-11AM

Name:_____ **Score**_____**/212**
SSN (last four numbers only) xxxx-xx-_____

This exam is closed-book and notes. A calculator is permitted.

HONOR CODE: At the end of the examination, please sign:

> *In recognition of the integrity of the engineering profession and the UCSC Honor Code, I certify that I have neither given nor received unpermitted aid during this examination.*
>
> Signature:_____

TRUE/FALSE Each question is worth 2 points. Mark an unambiguous **T** or **F** for each statement.

____ 1. Any logic circuit made only with NOR gates will always be strictly a combinational circuit.

____ 2. A state machine with *n* inputs, *m* outputs, and *p* flip-flops has 2^{p+n} output states.

____ 3. Using only OR gates, *any* logic can eventually be realized.

____ 4. The maximum speed of a ripple counter is limited primarily by the propagation delay of the first flip-flop.

____ 5. Hazard covers eliminate glitches due to inconsistent propagation delays in a combinational or sequential logic circuit.

____ 6. Covering ones on a K-map gives the SOP solution to F = 1.

____ 7. Covering zeroes on a K-map gives the SOP solution to F = 0.

____ 8. A Moore machine is one whose outputs depend only on memory devices.

____ 9. Digital logic circuits without feedback can be either combinational or sequential.

____ 10. The canonic sum for a function of 4 variables has 16 terms.

____ 11. The canonic product for a function of 4 variables has 16 factors.

____ 12. 1001110b is the unsigned binary form of +38d, and the two's complement form of –50d.

____ 13. -27d has 2's complement form: 1100101b, then 11100101b is also another equivalent form.

____ 14. The most significant bit is never the sign bit in unsigned binary notation.

____ 15. The significant timing parameter associated with edge-triggered flip-flops is setup and hold times for the clock.

____ 16. A *J-K* flip-flop can't "remember" the state associated with the inputs when both are logic 1.

____ 17. A sequential circuit whose states change as inputs change is not a synchronous circuit.

____ 18. Asynchronous circuits always have one or more clocks associated with them.

____ 19. An eight-phase clock can be generated using a 4-bit shift register configured as a Johnson Counter and eight 2-input AND gates.

____ 20. Generic array logic (GAL) may be configured to mimic combinational or sequential PAL's.

____ 21. A sequential circuit whose output is a 5 Hz digital square wave when its input is a 10 Hz digital square wave is a T flip-flop.

____ 22. Metastability is associated with voltages that are always within guaranteed logic levels.

____ 23. A level-triggered D-latch is one whose output always follows its D input whenever the clock is active.

____ 24. A *J-K* flip-flop made from a D-F/F does not exhibit the "one's catching problem".

____ 25. State diagrams can always be expressed as a next-state table and vice-versa.

____ 26. The state of a Mealy machine can change asynchronously with inputs.

____ 27. K-maps follow a Gray code between adjacent rows or columns.

____ 28. A fundamental memory cell can be created from NOR gates alone.

____ 29. DeMorgan's theorem is equivalent to taking the complement then the dual of any switching algebra function.

____ 30. A NAND gate and NOR gate with the same number of inputs are complements of each other.

____ 31. An XOR gate is the dual of itself.

____ 32. two D-latches and an inverter can be used to make an edge-triggered flip-flop.

____ 33. The memory flip-flops within a synchronous FSM will ideally always change states at the same time.

____ 34. A Mealy machine can only change states when either the clock ticks or an input changes.

____ 35. Metastability is not associated with transients or glitches.

____ 36. A 2-level AND-OR device that can only be programmed to implement SOP expressions is known as a CPLD.

____ 37. The PAL16L8 and PAL16R8 are otherwise identical except for memory.

____ 38. Hi-Z or tri-state logic was invented to allow multiple digital outputs do be connected together.

____ 39. A "registered" PLD contains internal D flip-flops.

____ 40. Hardware description languages like VHDLhave a strong similarity to procedural languages programming languages, where instructions are executed in a specific and sequential order.

____ 41. CPLD's are non-volatile while FPGA's are volatile.

____ 42. Propagation delay is the time it takes for an input change to appear at an affected output.

____ 43. Within the same logic family, the number of inputs that can be tied to one output is called Fanout

____ 44. In a datasheet, $I_{OL} = 30mA$. This means that current is flowing into the output.

____ 45. A two-bit full adder would be implemented with four levels of logic.

____ 46. The current state of a clocked synchronous state machine with *n*-flip flops can always be determined by looking only at the inputs that were applied to it at the previous 2^n clock ticks.

____ 47. A flip-flop having asynchronous clear and presets means that it can be set or cleared independent of a clock.

____ 48. The maximum clock frequency of a synchronous digital circuit can be increased by physically spreading the memory chips further away from each other on a circuit board.

____ 49. A D flip-flop having two outputs can be made into a T flip-flop without having to add additional logic.

____ 50. The total number of possible states in a machine with *n* flip-flops is always 2^n, regardless of the number of inputs or outputs.

____ 51. Tri-state is used to allow many different outputs to be connected one at-a-time to a common wire.

____ 52. Besides being able to define active-low logic, the XOR gate present at many PLD outputs also allows one to use either POS or SOP, whichever is simpler.

____ 53. Unused CMOS inputs should always be tied to a solid logic level to prevent excessive currents.

____ 54 A NAND latch has only a single feedback loop.

____ 55. Incompletely specified state diagrams with only input variable combinations not being accounted for will always cause instabilities after the circuit has been designed and built.

____ 56 Assigning coded states in Gray code order always results in the simplest excitation logic.

____ 57 A modulo-48 counter can be built with 5 flip-flops.

____ 58. CPLD's were invented to overcome the scaling and electrical limitations associated with large PAL's.

____ 59 Four 4-variable K-maps are required for an equation with 6 variables.

60. (12 pts.) Indicate whether each of the following equations is true or false. That is, mark "T" if the left-side equals the right-hand side for every possible combination of the input variables, otherwise mark "F". (*Scoring:* 3pts for correct answer, 1 for blank, 0 for incorrect or ambiguous.)

____(a) $A \cdot B + C' + M = (A + C' + M) \cdot (B + A' \cdot M + A \cdot M)$

____(b) $(W' + X + Y' + Z') \cdot (W' + X' + Y' + Z) = (W \cdot X' \cdot Y \cdot Z + W \cdot X \cdot Y \cdot Z')^D$

____(c) $\sum_{WXYZ}(2,8,9,13) = W' \cdot X' \cdot Y \cdot Z' + W' \cdot X \cdot Y \cdot Z + W \cdot X' \cdot Y' \cdot Z + W \cdot X \cdot Y' \cdot Z$

____(d) $W \oplus X \oplus Y \oplus Z = \sum_{WXYZ}(1,2,4,7,8,11,13,15)$

61. (15 pts.) The following sequential circuit exhibits a hazard. Determine where it is and show how it occurs with an excitation table and illustrate with a timing diagram. Assume the propagation delay of the inverter is 10ns and the three remaining gates are 2ns each.

62. (10 pts) Simplify the following circuit by eliminating one level of logic.

63. Write a state/output table, transition/excitation table, and excitation equations for the state diagram shown. This will be implemented using D flip-flops.

Coded state definitions [S1,S0]: A = 00; B = 01; C = 11; D = 10

State/output Table (16pts.)

	X,Y			
S	00,	01,	11,	10,
A				
B				
C				
D				
	S^+, Z			

Transition/Excitation table (16pts.)

	X,Y			
S1,S0	00	01	11	10
	$S1^+ S0^+$			

Excitation Equations (in minimal sum-of-products form) (12 pts.)

$S1^+ =$ _____

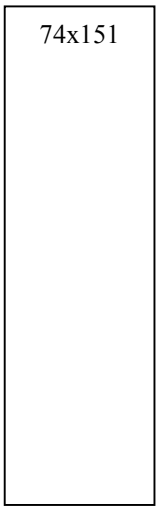
$S0^+ =$ _____

64. (5 pts.) Draw a circuit diagram that implements the state machine designed in the last problem using positive edge-triggered flip-flops.

65. (10pts.) Fill in the Karnaugh map and find a *minimal sum of products* expression for the function, F.

$$F = \prod_{WXYZ}(1, 2, 4, 7)$$

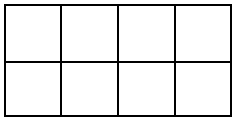
66. A 74x151 8-input multiplexer circuit is shown that realizes a combinational logic function. The circuit shown realizes a combinational function F of four variables.



[F03: this will be given in lecture on Monday, 12/1/03]

(a) (5pts.) Determine by inspection the function's SOP form, $F = \sum_{DCBA}(...)$.

(b) (5pts.) Realize the same function F above using a 4-input multiplexer instead.
Hint: use the K-map below to help you determine the inputs.



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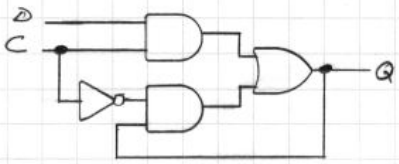
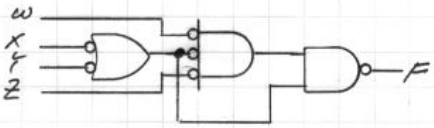
ADDENDUM

61.



62.



63.