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ESDA ONLINE ACADEMY COURSE REGISTRATION

ESDA Online Academy course registration page 2

First Name: _____ Last Name: _____

Phone: _____ Fax: _____ Email: _____

✓	Course Title/ # 1 hour Sessions	Date
	DD110 ESD Basics to Advanced Protection Design 3 Sessions	Mar-22,24,29
	FC215: Device Technology & Failure Analysis Overview 3 Sessions	Apr-5,6,7

✓	Course Title	# 1 hour Sessions
	Advanced ESD/EMI Auditing Techniques (1 Hour)	1
	Advanced HBM – Dealing with Tester Parasitics, High Pin Count and Two Pin Testing (1 Hour) (D)	1
	Advanced Latch-up for CMOS	1
	CDM Testing Essentials (1 Hour) (D)	1
	Changes to ANSI/ESD S20.20 from the 2007 version to the 2014 version (1 Hour)	1
	Charged Board Events: A Growing Industry Concern (1 Hour)	1
	Charged Device Model Phenomena, Design and Modeling (3 Hours)	3
	Cleanroom Considerations for the Program Manager (3 Hours) (PrM)	3
	Compliance Verification: Pitfalls of Auditing (1 Hour)	1
	Controlling ESD in Automated Equipment by Proper Grounding (1 Hour)	1
	Developing a Compliance Verification Program (1 Hour)	1
	Device Stress Testing Standards Update (1 Hour) (D-R)	1
	Device Technology and FA Overview (3 Hours) (PrM)	3
	Device Testing Correlation to Root Cause Failure Analysis (1 Hour)	1
	Electric Fields: Practical Considerations (1 Hour)	1
	Electrostatic Attraction (1 Hour)	1
	Electrostatic Calculations for the Program Manager (4 Hours) (PrM)	3
	Electrostatic Discharge Effects In Integrated Circuit Technologies (1 Hour)	1
	EOS - A Big Challenge in Today's Handling of Customer Rejects (1 Hour)	1
	ESD Fundamentals I for Stress Testing (1 Hour) (D)	1
	ESD Fundamentals II for Stress Testing (1 Hour) (D)	1
	ESD Problem Solving (1 Hour)	1
	ESD Test Simplification with Approved Sampling Methods in HBM (1 Hour) (D-e)	1
	Essentials for Controlling the ESD Work Area (1 Hour) (D)	1
	Fundamentals of Failure Analysis (1 Hour) (D)	1

(PrM) (DD) Taking all parts of this online class will fill the requirement for the full length tutorial that is a requirement of the ESDA Certification Program curriculum. Details on the Professional Certification Programs offered by ESDA are on our website at www.esda.org/certification.html.

✓	Course Title	# 1 hour Sessions
	Fundamentals of System Level Testing (1 Hour) (D-e)	1
	Grounding in an Electrostatic Protected Area (1 Hour)	1
	HBM & MM Testing Essentials (1 Hour) (D)	1
	HBM Tester Artifacts (1 Hour)	1
	Highlights and key concepts of Footwear/Flooring standards (1 Hour)	1
	Highlights and key concepts of Footwear/Flooring standards THAI (1 Hour)	1
	Highlights and key concepts of Footwear/Flooring standards Korean (1 Hour)	1
	High Speed Digital Oscilloscope Fundamentals (1 Hour) (D)	1
	HMM – System Level Testing of Components (1 Hour) (D-e)	1
	Integrated Circuit ESD Fundamentals (3 Hours)	3
	Integrated ESD Device and Board Level Design Part (2 Hours)	2
	Ionization Issues and Answers for the Program Manager (3 Hours) (PrM)	3
	Latch-up Fundamentals (1 Hour)	1
	Latchup Testing and Troubleshooting (1 Hour) (D-e)	1
	On-Chip ESD Protection in RF Technologies (DD)	1
	Overview on Efficient and Reliable System-Level ESD (1 Hour)	1
	Packaging Principles for the PrM (3 Hours) (PrM)	3
	ESD Protection and I/O Design	3
	ESD Standards Overview for the Program Manager (3 Hours) (PrM)	3
	Susceptibility Testing of Devices and Systems (1 Hour)	1
	System Level ESD/EMI: Testing IEC & Other Stand (3 Hours) (PrM) (DD)	3
	TCAD Fundamentals (1 Hour)	1
	TCAD Methodologies for Industrial ESD Design (1 Hour)	1
	TLP Fundamentals – Understanding the Equipment Options (1 Hour) (D-e)	1
	Ultra-Sensitivity Trends and CDM (1 Hour)	1
	VF-TLP, An Introduction to Capabilities and Applications (1 Hour) (D-e)	1

Total # 1-hour sessions_____x $195 = _____

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Ten 1-hour sessions _____X $1,755 = _____
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(D)Core class (D-e)Elective (D-R)Renewal class - Device Stress Testing Certification Courses-required and elective courses of the ESDA Device Stress Testing Certification curriculum. Details on the Professional Certification Programs offered by ESDA are on our website at www.esda.org/certification.html.

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ESDA ONLINE ACADEMY COURSE CATALOG
COURSE ABSTRACTS

Advanced ESD/EMI Auditing Techniques

Instructor: Al Wallash

In order to solve today's ESD problems, ESD auditing must provide data on not only the static charge and voltage on tooling and devices, but also the transient voltage, current and electromagnetic field interference (EMI) up to at least 1 GHz. This practical course will teach how to use a variety of charge, current, voltage and E-field probes to understand the ESD/EMI threats during processing of ESD sensitive devices.

Advanced HBM – Dealing with Tester Parasitics, High Pin Count and Two Pin Testing

Instructor: Scott Ward

Certification: DST

This tutorial provides an overview of the joint HBM standard by the ESDA and JEDEC which introduces numerous options to set up the test plan for HBM qualification. The options include high pin count devices, reducing relay capacitance from the tester and two pin testing. There was a need to explain these options in detail and a user guide has also been released to provide further guidance in these tests. This tutorial will attempt to cover the user guide and will give examples of setting up the different tests plans that utilize the options outlined in the standard.

Advanced Latch-up for CMOS

Instructor: Scott Ruth

The idea of this tutorial would be to tackle the practical aspects of designing and testing for latch-up robustness. From a design perspective, layout floor-planning, design rules, and EDA checks will be covered. From a test perspective, standard DC latch-up testing as well as transient latch-up testing (including systemlevel ESD, cable discharge, and the evolving transient latch-up standard) will be covered. Finally, real world latch-up failures and diagnoses will be presented.

CDM Testing Essentials

Instructor: Alan Righter

Certification: DST

This tutorial will give students the fundamental information required to quickly learn the CDM testing method on commercial CDM test equipment and the associated oscilloscope / metrology chain information needed to capture and interpret CDM waveforms. Additional information on CDM testing standards and their hardware differences, package effects on the CDM waveforms and package limitations will be covered. Students will also be introduced to the background information needed in understanding CDM failure modes along with test program output failure types needed to understand the effects of CDM testing.

Changes to ANSI/ESD S20.20 from the 2007 version to the 2014 version

Instructor: John Kinnear

This presentation will describe the changes to ANSI/ESD S20.20. The reasoning behind the changes will be addressed and questions will be taken from the audience. The actual presentation will be 30 to 35 minutes with time at the end for open discussion.

Charged Board Events: A Growing Industry Concern

Instructor: Terry Welsher

A charged board stores much more energy than a device (IC) because its capacitance is many times larger. In fact, the charge (energy) transferred in the event is so large that it can cause EOS-like failures to the components on the board. In this seminar, this board-level ESD event will be compared with the component level CDM ESD event. The waveforms from both ESD events will be compared and it will be shown that for the same voltage, the current in the board-level ESD event will be much higher than that from the chip-level ESD event. A summary of literature and industry data will be given. It is suggested that failure analysts give stronger consideration to these types of board level events before assigning an EOS diagnosis to the failure. This will support more effective root cause analysis and prevention of these failures.

DD200 Charged Device Model Phenomena, Design and Modeling (3 Parts)

Instructors: Melanie Etherton, Mike Chaine

This course teaches the fundamental concepts required to design ESD protection for Charged Device Model events and provides insight into the specific physical aspects of the phenomenon that need to be considered to verify the CDM ESD protection structures and concepts with circuit simulation. The fundamental physics of the CDM event, such as charge and discharge physics, characterization methods, and failures mechanisms are covered in this tutorial. The basics of CDM ESD design strategies for IOs are discussed and methods to verify the robustness of these ESD structures for the CDM target level. Circuits and strategies for protecting power domain signal crossings are introduced and methods are discussed for verifying the effectiveness of these solutions. Insight into CDM circuit simulation requirements and physical aspects of the CDM ESD phenomenon that are important for reproducing the event with circuit simulation for failure debugging or ESD strategy verification are provided.

Cleanroom Considerations for the Program Manager (3 Parts)

Instructor: Christopher Long

Certification: PrM

Many industries require “Clean Manufacturing”, however with clean manufacturing also come requirements for lowered humidity levels, process-required insulators, ultra-clean surfaces, processes which involve product movement, and a lack of naturally occurring ions. All of these can pose challenges from an electrostatic generation and discharge perspective. It is critical for those who work in industries that require clean manufacturing to know how to control static charge generation in and around contamination and ESD sensitive products. The purpose of class is to provide background on cleanroom/clean environment fundamentals, means of control and measurement of such environments, and methods for controlling/eliminating electrostatic discharge in clean manufacturing processes.

Compliance Verification: Pitfalls of Auditing

Instructor: Ginger Hansel

Accurate data is the foundation of effective ESD Program Management. Therefore, it’s important to have confidence in the measurements. Choosing the correct type of equipment for each measurement is also important and not always obvious. The class will cover the correct use of static locators, resistance meters, event detectors, and how to use ionizers effectively. We will discuss the various pitfalls of commonly used instruments, and the invalid test results that can result. For instance, static locators can yield totally invalid readings when used incorrectly due to voltage suppression. What you learn will help you avoid frequently encountered auditing problems, and improve your compliance verification program.

Controlling ESD in Automated Equipment by Proper Grounding

Instructor: Donn Bellmore

This course will focus on the grounding and material requirements of ESD Controls in Automated Handling Equipment (AHE) for prevention of CDM and MM type damage to ESD sensitive devices. Design methods and material selections that provide effective ground paths through the assembly will be introduced. Test methods used to qualify the design will be discussed. Students will also become familiar with different types of plating and practices to provide effective designs.

Developing a Compliance Verification Program

Instructor: John Kinnear

Compliance verification is one of the required elements in the ANSI/ESD S20.20 standard. Without periodic verification of the ESD materials used within an Electrostatic Protected Area (EPA) programs can degrade over time. This course will cover some of the items that need to be considered for a successful compliance verification program.

Topics covered in this program include,

- What is a compliance verification program?
- What is the difference between product qualification and compliance verification?
- How does the ESD program manager determine the frequency of testing?

As part of the course, common ESD control items will be covered and how to do the testing efficiently and to meet the requirements of ANSI/ESD S20.20 and TR53. Questions can be submitted in advance to be answered as part of the course.

Device Stress Testing Standards Update

Instructor: Alan Righter

Certification: DST

This tutorial will describe major updates to the HBM and CDM Device Stress Testing Standards. After a brief introduction to both the Joint ESDA/JEDEC HBM and proposed Joint CDM Standards and the motivations for their developments, specific improvements in each standard (relative to their previous separate ESDA and JEDEC standards) will be described. These stress testing method improvements will be supported by test setup and measurement data where appropriate. Examples of the HBM and CDM stress testing procedures (setting up, measurement) using the new updated standards will be given. After taking this course, students will have the basic understanding of the improvements in the Joint HBM and proposed Joint CDM Standards and a basic understanding of how to apply these improvements to existing testers for stress testing.

FC215: Device Technology and Failure Analysis Overview (3 Parts)

Instructor: Jim Vinson

Certification: PrM

This tutorial provides an overview of the device technology used to provide ESD protection, ESD protection techniques, and Failure Analysis (FA) techniques to debug non-working ESD protection. This class does not go into the depth necessary to equip the student to be an ESD Protection Designer or an ESD Failure Analysis Engineer. It does familiarize the student with the terms and concepts of ESD protection and FA to allow the student to interact and understand the work being done by the Designer or Failure Analyst. After completing this tutorial the student should be able to understand the basics of device ESD protection design and some of the trade-offs inherent in that process. The student should also be familiar with the most commonly used failure analysis techniques and tools used to identify the root cause of an ESD failure. The topics covered include: the three most common ESD Models: HBM, CDM and System Level (IEC); characteristics of ideal ESD protection; ESD failure analysis schemes; key characteristics of real ESD protection; failure analysis flow; failure analysis tools and how they are applied to ESD failures.

Device Testing Correlation to Root Cause Failure Analysis

Instructor: Leo G. Henry

ESD Device Stress Testing is known to benefit at least three areas: qualifying the product, simulate failures from factory or field, and to improve the design of the product. Three ESD models (HBM, MM and CDM) are used to simulate failures and to differentiate between the different types of ESD failures and also to differentiate the ESD type failures from EOS-type failures. Even though there are no Failure Analysis standards for ESD, there is enough archived data, published data and experience to show correlation exists between the ESD Stress testing types, the physical failure types and the eventual root cause. The type of equipment required to get to the physical failures and see the failures will be emphasized. The class will show how to correlate each ESD model stress testing results to the physical failure type and the physical failure location on the die. A real example will be used to show how the ESD stress testing lead to the root cause of a field failure.

Electrical Fields Practical Considerations

Instructor: David E. Swenson

ANSI/ESD S20.20 requires that process essential insulators with a measured electrical field strength of >2000 volts at 1 inch be kept a minimum of 12 inches from ESD susceptible items. Just what are the practical considerations of this statement? What about electrical fields of 1999 volts at 1 inch? Can items with lower field strength be ignored? Is there a size consideration when it comes to charged objects? If so, what is the size of a charged object that imposes a risk? What is the magnitude of an electrical field that should be of concern in a process?

This tutorial presents information from a recent investigation of electrical field strength that was conducted to support a revision of ANSI/ESD S20.20. The audience should gain a practical perspective of size and distance as related to electrical field strength. Additionally, the audience should be able to relate the information in this tutorial to their own process environments to help estimate the risk of damage to sensitive items that may be grounded within the electrical field from process essential insulators.

Electrostatic Attraction

Instructor: Carl Newberg

This training will cover the causes and effects of electrostatic attraction (ESA) and the solution to ESA problems in a variety of industries. Electrostatic attraction problems plague industries from photographic to medical and electronics. In the electronics industry alone, electrostatic attraction problems can be found in disk drive assembly, wafer fabrication and PC board assembly. The solutions to these problems can be found by applying a combination of the fundamentals of electrostatics and contamination control. An overview of clean rooms, ionization, materials and the control of static electricity will be presented. Real world problems and their solutions will be discussed using case histories.

I. Basics of electrostatics
II. Types of bonding
III. Physics of electrostatic attraction
IV. Industrial problems
V. Solving electrostatic attraction problems
VI. Case studies

Electrostatic Calculations for the Program Manager (4 Parts)

Instructors: Leo G. Henry, Terry Welsher

Certification: PrM

This on-line tutorial is a four part series on Electrostatic Calculations. The material included is the same as is included in the full tutorial usually presented at the EOS/ESD Symposium or ESDA Regional Tutorials. The four parts focus on the basic calculations and techniques of use to the Program Manager and the ESD engineer. The content is at the introductory high school or college pre-calculus and introductory college physics level set in the context of electrostatic discharge and its effects. Each part also includes an additional review of the mathematics used in the practical calculations.

Electrostatic Discharge Effects in Integrated Circuit Technologies

Instructor: Charvaka Duvvury

This course will outline the fundamentals of ESD phenomena and the methods to control the effects of ESD for safe manufacturing of IC devices. The training material will include the nature of ESD transients, their impact on the IC devices, common methods to test for ESD at both the device level and the system board level, and the overall protection techniques. Finally, the course will review the advances in IC technologies that lead to future challenges for ESD development and the resulting important technology roadmap established by the ESD Association.

EOS - A Big Challenge in Today‘s Handling of Customer Rejects An IEW Presentation

Instructor: Gerold Schrittesser

Handling of customer rejects has become more and more challenging over the years in view of EOS. Unlike ten years ago today most customers are asking for an EOS statement containing a conclusive and comprehensive explanation of the failure scenario that has finally resulted in an “EOS-like” damage and this EOS statement has to be discussed on much higher technical level. On the other hand still today there is not much awareness on the customer side that most “EOS-like” failure signatures do not allow a comprehensive conclusion to the origin of EOS and so the final root cause cannot be evaluated without customer’s support. But in order to be prepared to conduct a successful root cause analysis together with customer the supplier is committed to build up an EOS knowledge base for both internal and external needs. The seminar should deliver insight in today‘s handling of customer rejects in terms of EOS and all the background that is necessary to be successful in that important topic – complemented with a few demonstrative examples.

ESD Fundamentals I for Stress Testing

Instructor: Terry Welsher

Certification: DST

This tutorial is part 1 of a condensed version of the ESD Basics for the Program Manager tailored for technicians and engineers who direct or perform ESD stress testing at the device and system level. This tutorial provides the foundational material for understanding electrostatics and ESD along with their role in the manufacturing and handling of ESD sensitive devices. The fundamental properties of charge, electric fields, voltage, capacitance, and current are discussed with a view towards understanding key electrostatic phenomena and electrical processes; these include charge generation and decay, material properties, and induction. An overview of device failure mechanisms is presented, including how these models impact ESD control programs.

ESD Fundamentals II for Stress Testing

Instructor: Terry Welsher

Certification: DST

This tutorial is part 2 of a condensed version of the ESD Basics for the Program Manager tailored for technicians and engineers who direct or perform ESD stress testing at the device and system level. This tutorial provides the foundational material for understanding electrostatics and ESD along with their role in the manufacturing and handling of ESD sensitive devices. The fundamental properties of charge, electric fields, voltage, capacitance, and current are discussed with a view towards understanding key electrostatic phenomena and electrical processes; these include charge generation and decay, material properties, and induction. An overview of device failure mechanisms is presented, including how these models impact ESD control programs.

ESD Problem Solving

Instructor: John Kinnear

It’s Friday at 3:00 and your quality manager calls you, “We are having ESD failures”. Now what do you do? Go out and audit your line? This online course will outline the steps that you should take to examine your process before you audit your line or even leave your office. A systematic approach will be explained on the logical steps to take for ESD troubleshooting. Only after such an analysis should you go on the line for measurements or assessments.

ESD Protection and I/O Design

Instructor: Michael Stockinger

This tutorial is intended to provide the attendees with the tools to take a device and circuit level understanding of ESD protection methods and implement them effectively in I/O designs for CMOS bulk technologies. Beginning with a review of common ESD protection strategies, this course will focus more directly on how to build ESD-robust I/O cells and how to integrate them on a full chip. The tutorial will cover various types of I/O pads including analog, RF and digital pads. Different types of ESD protection strategies and their usage in I/O pad cells will be described, for example rail clamp, self-contained, and SCR based protection schemes. This course will also discuss the decisions and challenges which ESD and I/O designers typically face when designing I/O pads. More complex ESD solutions will also be described such as stacked rail clamps, ghost rails, and protecting signals that can swing below ground or above the supply. Finally, this tutorial will touch on various supply schemes including multiple power domains and isolated grounding schemes. It will end with discussing pad ring construction aspects for both wire-bond and flip-chip packages.

ESD Test Simplification with Approved Sampling Methods in HBM

Instructor: Charvaka Duvvury

Advances in semiconductor technology development have enabled significantly more complex integrated circuits (IC). This complexity has driven an increased number of pins on an IC package. These higher pin count IC packages have led to a significantly higher ESD qualification cost and complexity. However, many designs often have a large number of common or "cloned" IOs which enables the possibility of using statistical sampling schemes to help improve ESD qualification in an efficient manner without reducing the overall quality of the stress test method. This tutorial will discuss the details behind the changes that are being made to the joint ANSI/ESDA/JEDEC JS-001-2012 HBM Test Method, including the definition of cloned IOs, the procedure for sampled testing of cloned IOs and a clear statistical justification behind these changes. The tutorial will conclude with a discussion of possible future opportunities in both HBM and CDM test methods for even further improvements in using statistical sampling techniques.

Essentials for Controlling the ESD Work Area

Instructor: Ginger Hansel

Certification: DST

This tutorial focuses on the basic components of an ESD controlled work area and how to verify the correct operation of each component. Most ESD protected Areas (EPA) include grounded workstations (special mats or table tops) and personnel grounding techniques (wrist straps, constant monitors, heel grounders, footwear, conductive flooring and dissipative chairs). In addition, the proper use and testing of smocks and ionization will be covered.

Fundamentals of Failure Analysis

Instructor: Jim Vinson

Certification: DST

Failure analysis is the diagnostic tool of the semiconductor industry. It is the semiconductor equivalent of forensic science. Failure analysis unravels the mystery behind how and why a part failed, determining the root cause and corrective actions needed to prevent future failures. This tutorial is targeted toward people doing stress testing on a daily basis where failures are generated and need to be analyzed to determine what failed and how to improve a part's robustness. The focus will be on failure analysis methods and tools use to analyze failures resulting from ESD, TLP, or latchup related stressing but will be applicable for wearout as well as infant mortality related failures as well. The tutorial will cover the 5 basic steps necessary to perform a failure analysis: 1) Information Gathering, 2) Failure Verification, 3) Failure Site Localization, 4) Root Cause Investigation, and 5) Corrective Action.

Fundamentals of System Level Testing

Instructor: Mike Hopkins

Certification: DST

This tutorial provides an understanding of how testing done at the system level is essential to understanding the stress that will be applied to a device installed in the final product. This tutorial will cover the various system level testing standards including how the tests are performed and evaluated. Guidance is provided for applying these tests at the device level. Test results will be discussed and differences between hard and soft failures examined. In addition, a brief overview of tools available for root cause analysis at the system level will be examined.

Grounding in an Electrostatic Protected Area

Instructor: David E. Swenson

Grounding is perhaps the single most important technical aspect in establishing an electrostatic protected area. The ESD Association grounding standard ANSI/ESD S6.1 provides potential users with specifications, guidance and suggestions for implementing a grounding/bonding system suitable for nearly any imaginable application. This information is not found anywhere else in industry literature.

This web-based training session will include answers to the following questions:

- What grounding method is appropriate for a work area?
- What measurements are needed?
- Are there any new terms or definitions?
- What are the proper ways to ground personnel in the workplace?

HBM & MM Testing Essentials

Instructor: Leo G. Henry

This tutorial reviews how HBM and MM ESD stress testing are approached from the basic understanding of how the HBM and MM ESD events can occur in the factory and or the field. The tutorial covers the difference between the two in terms of qualification (HBM only) and characterization (both HBM and MM) of product. HBM and MM standards will be used to teach the basics of the two stress testing methods. The use of the correct measurement equipment will also be covered.

HBM Tester Artifact Overview An IEW Presentation

Presenter: Scott Ward

A number of HBM tester artifacts have been discovered, characterized and published in recent years. Although several of the artifacts have been addressed with hardware improvements, many must be avoided by modification to the HBM stress plan. Due to ever shrinking device geometries, new tester artifacts are expected to be encountered. This seminar makes on-chip ESD protection designers aware of these tester artifacts to prevent unnecessary time spent on debugging failures that have a root cause inside the HBM tester architecture and not on the on-chip ESD protection network.

Highlights and key concepts of Footwear/ Flooring Standards

Instructor: Kevin Duncan

Footwear/Flooring Systems can play a major role in a successful ESD Control Program. How do you properly select and implement an ESD Footwear/Flooring System? This course will provide an overview of the concepts and Standards used for product qualification of footwear and flooring, as well as compliance verification of a Footwear/Flooring System.

This course will focus on the Footwear/Flooring Standards and Standard Test Methods related to selecting and implementing a Footwear/Flooring System for use an ANSI/ESD S20.20 Control Program.

High Speed Digital Oscilloscope Fundamentals

Instructor: Marcos Hernandez

This tutorial reviews the basic characteristics of oscilloscopes, general use of modern oscilloscopes and their specification as they relate to ESD measurements. Examples of measurements capturing waveforms and analysis on HBM, MM, HMM, CDM, and TLP waveforms will be presented. The basic specifications of a typical oscilloscope and their implications for accuracy on ESD measurements will be reviewed. Topics include sampling rate along with analog and digital bandwidth considerations.

HMM – System Level Testing of Components

Instructor: Mirko Scholz

Certification: DST

This tutorial will explain in detail the intent of the HMM standard test method. The tutorial starts with the hurdles of testing components to the IEC 61000-4-2 standard. The scope and purpose of the HMM standard test method will be discussed. The waveform used in this test and its critical specifications are presented along with the qualified equipment used to deliver the waveform. Three test configurations are introduced to address equipment specifics and recommending grounding. The tutorial will also provide some data to show the measurement variability that this test method has.

Integrated Circuit ESD Fundamentals

Instructors: Alan Righter, Warren Anderson

This three hour tutorial is focused on integrated circuit ESD fundamentals, and is targeted for two audiences: for the IC circuit designer who needs knowledge of how ESD can affect IC design, test, handling and system use; and those engineers wishing to be introduced to IC ESD, as a primer to further study. The tutorial covers the following topics:

- •ESD Definitions
- •Overview of the ESD Threat and ESD Controlled Workspaces
- •ESD Stress Models and Standards
- •Introduction to Transmission Line Pulse (TLP) ESD Testing
- •ESD Design Window
- •ESD Protection Network Design
- •Power Clamp ESD Design and Tradeoffs
- •Input Protection ESD Design
- •Output Drivers ESD Design
- •Switches (Transmission Gates) ESD Design
- •RF ESD Protection
- •IC ESD - Integration Issues
- •CDM Protection Guidelines
- •ESD Design Verification
- •ESD Debug and Diagnosis

Integrated ESD Device and Board Level Design

Instructors
part1: David Pommerenke, University of Missouri-Rolla
part2: Harald Gossner, Intel Mobile Communications

Efficient ESD design for system level ESD can only be achieved if board and device level protection circuitry coincide. The purpose of this tutorial is to develop an understanding of board/ IC interaction under IEC 61000-4-2 testing conditions and to discuss useful design strategies supported by appropriate tools. This is meant to be beneficial both for ESD engineers of ICs and board designers responsible for EMC/ESD compliant design of the system. While it has clearly been pointed out that even elevated IC level HBM targets are insufficient for achieving the required IEC 61000-4-2 ESD level, more awareness has to be developed for the detailed turn-on and clamping behavior of IC level and board level ESD protection components. High current characterization of board protection and IO circuit by TLP is a first step. This enables the board designer to assess the behavior of IC pins and select appropriate board protection elements. The design optimization should be based on high current models of board components and IC IOs and the numerical simulation of the protection network under ESD conditions. Finally, various test methods are available to evaluate the efficiency of implemented protection on board level quantitatively

Ionization Issues and Answers for the Program Manager (3 Parts)

Instructor: Arnold Steinman

Certification: PrM

The primary method of static charge control is direct connection to ground for conductors, static dissipative materials, and personnel. But a complete static control program must also deal with isolated conductors, insulating materials, and moving personnel that cannot be grounded. Air ionization can neutralize the charge on insulated and isolated objects. It does this by charging the molecules of the gases in the surrounding air. Whatever charge is present on objects in the work area, it will be neutralized by attracting opposite polarity charges from the air. This webinar will present the information needed to use ionizers to solve problems caused by static charge. It is a basic course on ionizers, providing an introduction to their use, as well as advanced application information.
NOTE: Taking all three parts of this online Ionization class will fill the requirement for the full length tutorial that is part of the ESDA Program Manager Certification curriculum. Details on the Professional Certification Programs offered by ESDA are on our website at www.esda.org/certification.html.

DD112 Latch-up Fundamentals

Instructor: Steve Voldman

Certification: DD

Latch-up continues to be of interest today in advanced CMOS, mixed signal (MS) CMOS, RF CMOS, BiCMOS and smart power technologies. Those attending this course will understand the fundamentals of CMOS latch-up. The course will focus on theory, test structures, application, experimental results, simulation and CAD design systems. Those attending will also understand the impact of design, semiconductor process and circuits on CMOS latch-up.

Latchup Testing and Troubleshooting

Instructor: Marty Johnson

Certification: DST

This tutorial focuses on latch-up testing and troubleshooting. Latch-up is primarily seen in CMOS and BiCMOS technologies but can be present in bipolar technologies. Resistance to latch-up is generally characterized during process development and design rules are implemented at device circuit block layout. Design checks for latch-up are often implemented but latch-up immunity is still mainly guaranteed by testing. This tutorial will help the student to understand the issues related to latch-up, ways to prevent it and methods used for verifying latch-up resistance in products.

DD110 ESD Basics to Advanced Protection Design

Instructor: Charvaka Duvvury

Certification: DD

This tutorial addresses important issues in the design of IC protection circuits built with advanced deep sub-micron CMOS technologies, including silicon-on-insulator (SOI) and high voltage MOSFETs. The tutorial will present fundamental aspects of ESD protection design such as basic NMOS and SCR concepts, as well as gate-biased and substrate driven NMOS protection concepts. Protection design methods to meet the human body model (HBM), machine model (MM), and charged device model (CDM) will be presented. Other topics to be covered include BiCMOS protection circuits, mixed voltage protection, and compatibility to latch-up. Specific design examples will be presented to assist in understanding the methods for design synthesis. This tutorial is useful for design, device, process, product, failure analysis, and reliability engineers and will assist those attending other design related tutorials. Attendees should have a minimum knowledge of MOS device operation in integrated circuits.

On-Chip ESD Protection in RF Technologies

Instructor: Steve Voldman

Certification: DD

In this tutorial, electrostatic discharge (ESD) protection in both MOSFET- and bipolar-based radio frequency (RF) technologies is discussed. It covers ESD protection in RF CMOS, BiCMOS silicon germanium, gallium arsenide, and RF silicon-on-insulator (SOI). The tutorial will focus on how RF ESD design is distinct from digital CMOS ESD design. This tutorial will focus on device physics, technology, ESD layout design, ESD circuits, and design systems. It will present methods for co-synthesizing ESD networks for RF applications. The tutorial will provide examples of RF testing methodologies for ESD qualification of components and systems. HBM, MM, and TLP measurements of RF technologies will be provided. The tutorial will provide ESD input networks, differential pair networks, and ESD power clamps used in both RF CMOS and in RF BiCMOS

technologies.

Overview on Efficient and Reliable System-Level ESD Protection Design An IEW Presentation

Instructor: Mirko Scholz

The ongoing integration of system functionality in ICs requires that IC pins comply with system-level ESD specifications. Often without knowing the final application, component-level ESD designers need to provide designs which are also robust to system-level ESD stress. In contrary, system-level ESD designer usually have no access to information about the component-level ESD protection design. To overcome this situation, the system-efficient ESD design (SEED) has been proposed. This online seminar introduces and evaluates two main system-level design methodologies: datasheet-based design and SEED (System-efficient ESD design). Different examples illustrate which data is used as design input and what are the limitations of each methodology. It is shown how component-level ESD testing and transient simulations (SPICE and mixed-mode) enable an efficient and reliable system-level ESD protection design.

Packaging Principles for the Program Manager

Instructor: David Swenson

Certification: PrM

Shipping electronic parts within a factory, to another factory, distributor, or to an end-user has always been an area of uncertainty within the manufacturing process.

To provide clear-cut information on what type of controlled packaging should be used in any situation, the ESD Association released a comprehensive revision of the obsolete industry standard EIA 541-1988. The newer document, ANSI/ESD S541, is the focus of this inclusive session. It provides information and guidance, as well as material specifications, to assist in the design and implementation of a packaging plan for use within an ANSI/ESD S20.20 based ESD Control Program. Current and newly released test method standards suitable for packaging material evaluation will be described. Course credit applies to the ESD Program Manager Certification curriculum. Previous attendance at the “ESD Basics” and “How To’s…” tutorials are highly recommended.

ESD Standards Overview for the Program Manager (3 Parts)

Instructor: David E Swenson

Certification: PrM

The ESD Association’s introduction of the Program Manager Certification curriculum has created a need to modify the Standards Tutorial that has been presented for a number of years, mainly to help individuals prepare for the iNARTE Engineering and Technician Exams. Currently, many of the ESDA Standards and Standard Test Methods are discussed in depth in the individual tutorials related to the specific subject matter. This Standards Tutorial provides an overview of all the Standards, grouped into common test types, based on measurement probe and test instruments. A common methodology is used in this tutorial to cover the requirements, applications and specifications for each Standard and Standard Test Method.

Susceptibility Testing of Devices and Systems

Instructor: Michael Hopkins

There is a disconnect in the EMC (Electro Magnetic Compatibility) world between system manufacturers testing systems for upset and device manufacturers testing devices for failure. Some system level manufacturers are pushing device manufacturers to test semiconductor devices using system level compliance standards – specifically, IEC 61000-4-2 for ESD (Electrostatic Discharge). Product manufacturers would like to believe that if devices are qualified to IEC standard(s); finished products will likewise be qualified. Unfortunately, there is a fundamental difference between system level and device level testing; fortunately however, this difference can be bridged using new susceptibility scanning techniques on the board or device. Until now, EMC and ESD susceptibility testing at the device level has not been done. In this course, we will cover scanning methods (using a magnetic field noise source and probe) that allow identification of susceptible devices in a system, sensitive areas/pins of devices and associated circuitry.

System Level ESD/EMI – System Level ESD Testing & Evaluation to the IEC ESD Standard

Instructor: Mike Hopkins

Certification: PrM

This tutorial is intended to help those tasked with ESD testing of products and devices to understand how testing is done and how failures are defined at the System Level. It will provide detailed information on IEC 61000-4-2, the most commonly used ESD test at the system level, as well as specific information about Automotive, Medical, and Avionics test requirements. The course will answer common questions regarding test set-ups, test points and procedures and address key issues, including the use of IEC 61000-4-2 for testing devices now being required of some device manufacturers.

TCAD Fundamentals

Presenter: Kai Esmark

TCAD (technology computer aided design) tools have become an indispensable utensil for the semiconductor industry. The possibilities to analyze, predict and optimize a certain semiconductor device behavior through modeling semiconductor fabrication (Process TCAD) and semiconductor device operation (Device TCAD) are countless. This includes the area for ESD and Latch-up development, as early access to fundamental device parameters under very high current density and high temperature transients is the key to overcome the conceptual problem of concurrent engineering for ESD engineers.

This tutorial serves as a basic introduction into TCAD tool chain including process and device simulation as well as the creation and integration of compact models for mixed more simulation. Focus points are the capabilities but also limitations of these tools, like the requirements for a 2D/3D simulation approach and the validity of the models describing the fundamental physics,

especially in the high temperature regime.

TCAD Methodologies for Industrial ESD Design An IEW Presentation

Presenter: Vladislav Vashchenko

This seminar provides a comprehensive overview of the TCAD methodologies and best practices for industrial ESD design. Both the generic simulation workflow review and the classification of the most representative cases are covered. The advanced capability of mixed-mode simulation approach with device, circuit and process parameterization is demonstrated. Fabless and fab-light industry trends are addressed by overcoming the critical requirement of the well calibrated process simulation flow. The overall goal of the seminar is to add a new dimension to the standard R&D methodology and make it directly useful to a broad audience of ESD device, circuit and application engineers rather than corporate TCAD experts.

TLP Fundamentals – Understanding the Equipment Options and IV Data

Instructor: Evan Grund

Certification: DST

This tutorial will explain what Transmission Line Pulsing (TLP) is and how it can be used for ESD design and development. Taking accurate TLP measurements is important thus how TLP systems make measurements and produce IV plots will be reviewed. The IV plots provide very valuable device parameters that are key to understanding the DUT being stressed. The tutorial will also explain the parameters that can be extracted from those IV curves. Finally typical equipment used in TLP systems will be reviewed.

Ultra-Sensitivity Trends and CDM

Instructor: Ted Dangelmayer

The electronics industry faces a double challenge: increasing use of ultra-sensitive devices and lack of experience with the Charge Device Model (CDM). This class will give you the background to understand the challenges and prepare to meet them. Case studies will illustrate how CDM failures can persist even with a robust HBM program in place. A series of photographs of common CDM issues in manufacturing will enable students to visualize how to implement CDM controls. A brief summary of the work by the Industry Council on ESD Target Levels will be included.

VF-TLP, An Introduction to Capabilities and Applications

Instructor: Mirko Scholz

VF-TLP stands for Very Fast Transmission Line Pulsing. Standard TLP uses typically 100 ns long pulses. It allows the device characterization in the HBM time domain. VF-TLP uses pulses with a duration of a few nanoseconds and faster rise times than standard TLP. It allows the device characterization and (transient) voltage and current measurement in the CDM time domain. This tutorial explains the VF-TLP measurement setups, equipment options and how the extracted data is interpreted. Several examples explained how the VF-TLP setup parasitic are de-embedded and applied to the obtained “raw” measurement data. The goal of the tutorial is to enable the operator to deliver high quality measurement data to the ESD protection designer.