# *logiREF-SDSoC-FACE-EVK*

## *Using an Existing HDL IP Core as a C-Function in the Xilinx® SDSoC™ Development Environment*

## *Demo – Xylon Face Detection and Tracking*

# User‘s Manual

***Version: 1.0.0***

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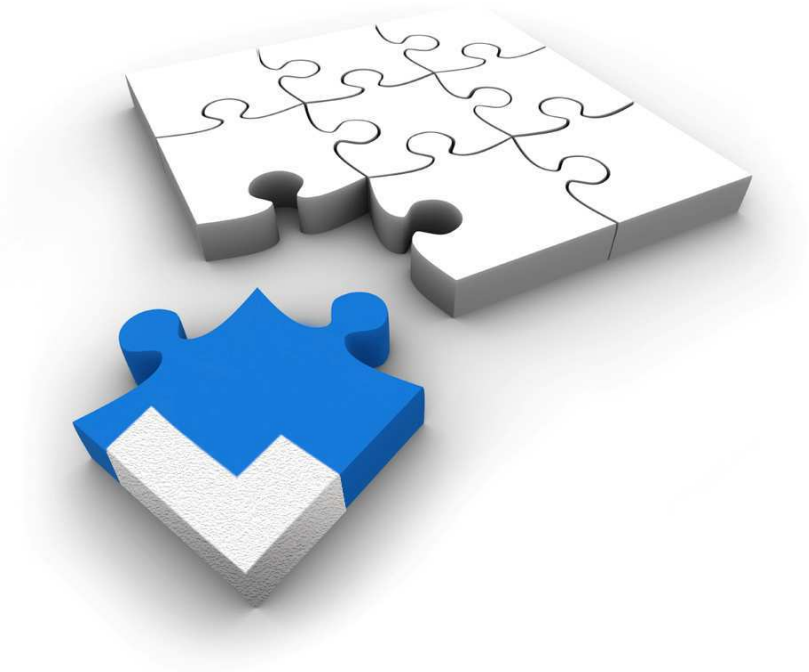


# 1 INTRODUCTION

The logiREF-SDSoC-FACE-EVK is free and pre-verified logicBRICKS reference design that includes evaluation logicBRICKS IP cores and hardware design files prepared for the Xilinx SDSoC Development Environment. It also includes the SDSoC platform files for the targeted hardware platform, demo software, and documentation.

The showcased application example is a real-time face and facial features tracking [Fig 1.] in video sequences from a video camera REF [1]. The design is prepared for the Xilinx Zynq®-7000 All Programmable SoC based MicroZed™ Embedded Vision Development Kit from Avnet Electronics Marketing fitted with the ON Semiconductor's PYTHON-1300 1.3 MP video camera.

The Xilinx SDSoC development environment enables developers to easily combine HDL-based IP cores and the C/C++ implemented IP cores within a single familiar framework, and this demo demonstrates how an existing Xylon's logiFDT Face Detector and Tracker IP core can be wrapped into a C-function and used within software defined SDSoC development environment.

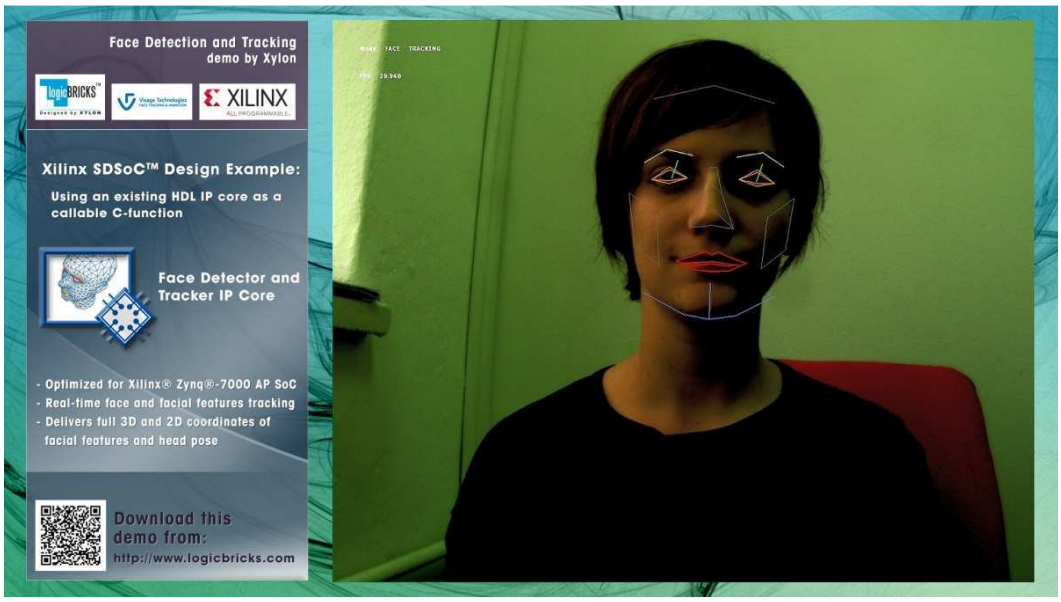



**Figure 1: Screenshot from the Xylon Face Tracking Demo**

This reference design is functionally equal to Xylon's logiREF-FACE-TRACK-EVK Face Detection and Tracking reference design, which is implemented fully in the Xilinx Vivado® Design Suite:
http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Face-Detection-for-Zynq-AP-SoC.aspx

Please check Xylon's Video Gallery web pages (http://www.logicbricks.com/logicBRICKS-IP-Library/Video-Galleries/logicBRICKS-Face-Tracking-Demo.aspx) to preview the Face Tracking demo provided with the logiREF-SDSoC-FACE-EVK installation for your MicroZed EVK development kit.

## 1.1 About Face Detection and Tracking Application

A human face provides a variety of different communication functions in complex interactions between humans. Beside to identification, humans use head pose and facial expressions during conversation to express emotions, reveal intents, display attention and more. The face detection and tracking is a computer technology that uses video images captured by the video camera to determine and track those distincttive facial features.

This technology significantly improves human-machine interaction and opens a very wide range of applications, such as driver drowsiness detection in automotive safety systems that prevent accidents, speaker detection in video conferencing systems capable to automatically zoom to the current speaker, hands-free interfacing helping disabled people to improve their daily lives, character animations in virtual reality entertainment and gaming, health, robotics, audio processing and others.

Xylon and Visage Technologies AB have entered a technology partnership with the goal of jointly delivering Visage Technologies' state-of-the-art face detection and tracking technology through the Xylon logicBRICKS IP library. As the result of this partnership, Xylon has designed the logiFDT Face Detector and Tracker IP core optimized for use with Xilinx Zynq-7000 All ProgrammableSoC.

The logiFDT IP core finds and tracks the face and facial features in video sequences in real time (up to 30 fps) and returns full 3D head pose, gaze direction, facial features coordinates and a wealth of other information that can be used in different applications developed on top of it.

*logiFDT I SDK Face Track tracking engine is sourced from Technology Partner Visage Technologies AB*

## 1.2 About Xilinx SDSoC Development Environment

The Xilinx SDSoC development environment is a member of the Xilinx SDx™ family that provides a greatly simplified ASSP-like C/C++ programming experience including an easy to use Eclipse IDE and a comprehensive design environment for heterogeneous Zynq® All Programmable SoC and MPSoC deployment.

Complete with the industry's first C/C++ full-system optimizing compiler, SDSoC delivers system level profiling, automated software acceleration in programmable logic, automated system connectivity generation, and libraries to speed programming.

To access the capabilities of SDSoC, please visit www.xilinx.com/sdsoc

***Xylon is an SDSoC development environment-qualified Xilinx Alliance Member and offers logicBRICKS IP cores, complete Xilinx All Programmable based solutions and design services.***

## 1.3 Required Hardware Platform

The logiREF-SDSoC-FACE-EVK prepared for the MicroZed Embedded Vision Kit from Avnet Electronics Marketing. The compatible demonstration platform requires the following hardware components:

**Figure 2: Avnet MicroZed Embedded Vision Kit**

- MicroZed Embedded Vision Development Kit
  (Part Number*: AES-MBCC-EMBV-DEV-KIT)

or the equivalent combination built of:

- MicroZed 7020 SOM
  (Part Number*: AES-Z7MB-7Z020-SOM-G)
- MicroZed Embedded Vision Carrier Card Kit
  (Part Number*: AES-MBCC-EMBV-G)

and:

- ON Semiconductor PYTHON-1300-COLOR Camera
  (Part Number*: AES-CAM-ON-P1300C-G)

* Avnet Electronics Marketing part number – for more details visit www.microzed.org

## 1.4 Required Development Software

The logiREF-SDSoC-FACE-EVK reference design and Xylon logicBRICKS IP cores are compatible with the Xilinx SDSoC Development Environment 2015.2.

## 1.5 How to Get the Reference Design

This reference design is available for free and with no obligations to registered logicBRICKS web users. To get the design, please visit our web site and follow instructions from the Chapter 8.:

www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Face-Detection-Tracking-SDSoC-Demo.aspx

# 2 DESIGN DELIVERABLES

## 2.1 SDSoC platform

- Supports standalone applications
- Includes software drivers for included logicBRICKS and Avnet IP cores
- Contains the pre-built hardware files for faster software development.
- Xylon evaluation logicBRICKS IP cores:
    - logiWIN Versatile Video Input
    - logiCVC-ML Compact Multilayer Video Controller
    - logiCLK Programmable Clock Generator
    - logiBAYER Color Camera Sensor Bayer Decoder

## 2.2 Software

- logicBRICKS standalone (bare-metal drivers) with driver examples
- Zynq FSBL sources and the Xilinx SDK project – custom version for standalone applications
- Bare-metal demo application for face detection and tracking

## 2.3 Binaries

- Precompiled SD Card image for the fastest demo startup

# 3 USAGE MODES

The logiREF-SDSoC-FACE-EVK reference design can be used in different ways, which are listed in this paragraph and thoroughly explained through this document.

## 3.1 Quick Evaluation with no HW and/or SW Changes

- Download and install the logiREF-SDSoC-FACE-EVK reference design (chapter 8 GET AND INSTALL THE REFERENCE DESIGN)
- Setup the demo hardware and use the provided SD card image to run the precompiled demo application (paragraph 6.1 Set Up the MicroZed EVK kit for Use with the Precompiled Demo From the SD Card)

## 3.2 Change the HW/SW through the SDSoC workflow

In order to develop standalone software applications and optionally to add your own C/C++ or HDL-based hardware accelerators in the programmable logic, please follow these steps:

- Download and install the logiREF-SDSoC-FACE-EVK reference design (chapter 8 GET AND INSTALL THE REFERENCE DESIGN)
- Setup the demo hardware (paragraph 6.1 Set Up the MicroZed EVK kit for Use with the Precompiled Demo From the SD Card)
- Obtain logicBRICKS IP core evaluation licenses from Xylon (chapter 9 GETTING LOGICBRICKS EVALUATION LICENSES)
- To set up the working environment follow instructions listed in the **`start.html`** file from your installation root folder for this reference design
- Try demo compilation and develop your own applications

# 4 LOGIREF-SDSOC-FACE-EVK DESIGN

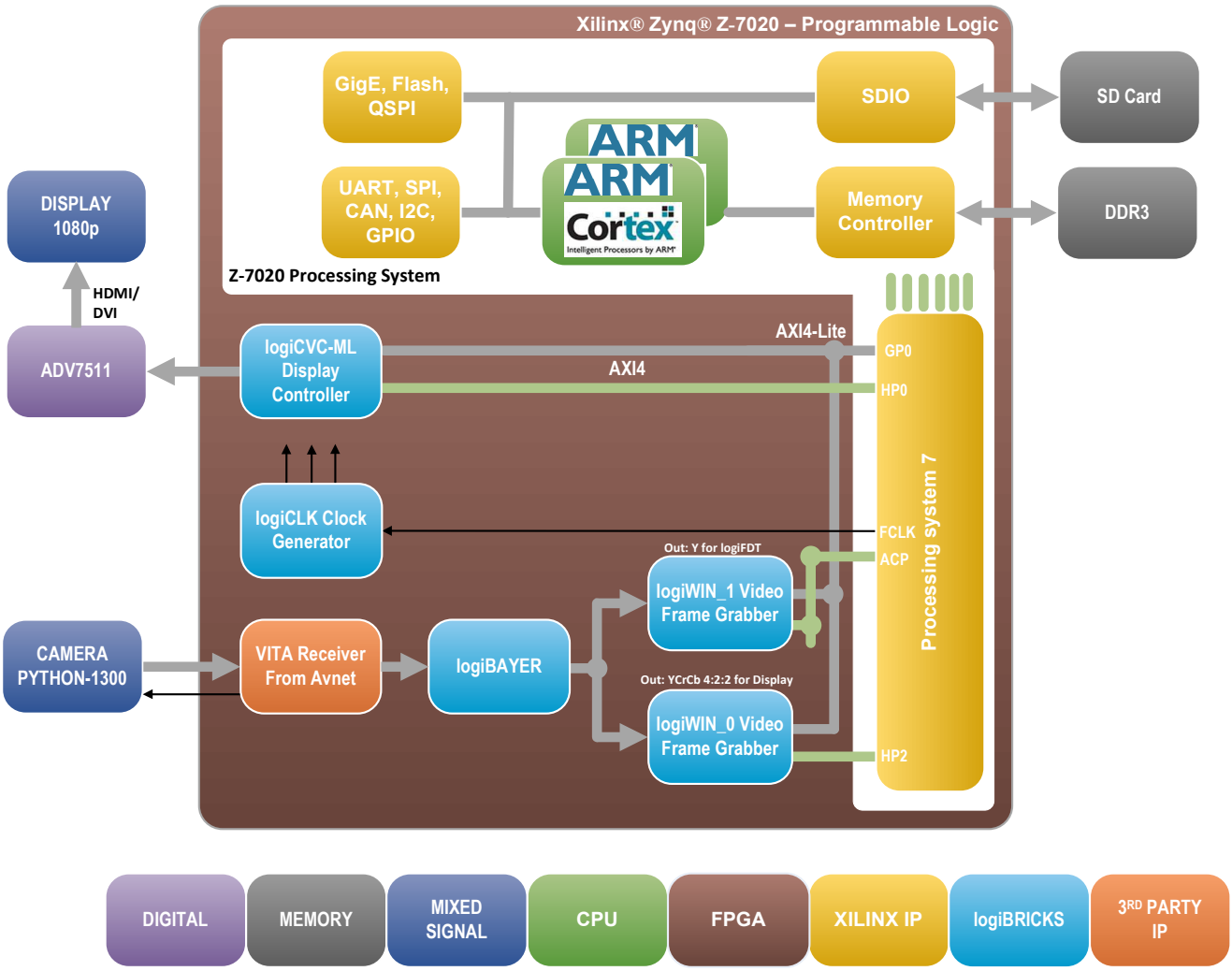



**Figure 3: logiREF-SDSoC-FACE-EVK SoC Block Diagram (Pre-Defined Platform)**

Figure 3 shows the simplified block diagram of the logiREF-SDSoC-FACE-EVK **`evk_fdt`** SDSoC platform without the logiFDT IP core accelerator instantiated.

Figure 4 shows the block diagram of the SoC design completed with the instantiated logiFDT IP core for face tracking acceleration, which is used as a C-callable function within the SDSoC design environment.

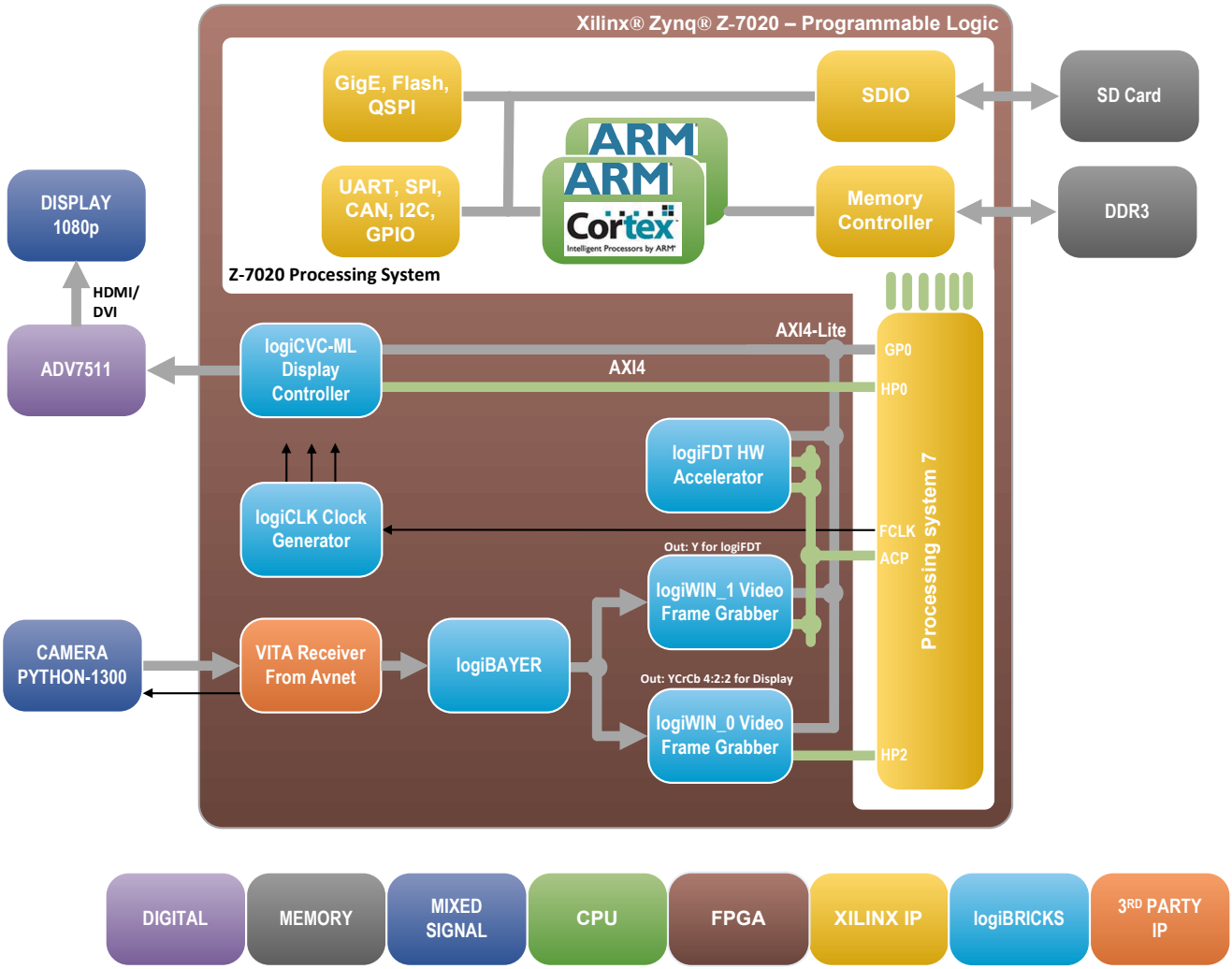



**Figure 4: logiREF-SDSoC-FACE-EVK SoC Block Diagram (Platform with the logiFDT IP)**

From the input to the output, image from camera is processed using a number of IPs. The VITA Receiver IP core from Avnet Electronics Marketing receives the video data from the ON Semiconductor PYTHON-1300 camera module (LVDS data) and provides raw Bayer video data and video sync signals at its outputs. The logiBAYER IP core converts camera sensor video from Bayer color space to YUV color space.

The design utilizes two instances of Xylon logiWIN Versatile Video Input frame grabbing IP core. One logiWIN IP core does a full resolution frame grabbing, then formats and stores the video for the display. The other logiWIN IP core scales the video input to the resolution required by the logiFDT face tracking engine and, as it is requested by the face tracking software, generates the single-channel video containing only the Y (luminance) component of the YUV video input. Xylon's logiCVC-ML Compact Multilayer Video Controller IP core displays the camera video overlaid by graphically presented face tracking results.

The logiWIN frame grabbers store the video in video frame buffers implemented in external DDR3 memories. The logiWIN is AXI4 bus protocol compliant and can be easily connected to Zynq-7000 AP

SoC memory controller. The logiWIN IP cores are synchronized with the logiCVC-ML Compact Multilayer Video Controller and the logiFDT Face Detector and Tracker. The IP core enables easy implementation of the multiple buffering video storage method that assures a flicker-free video output.

The memory subsystem is an essential part of any video and graphics based system. It must ensure enough storage space for video buffers, GUI elements and application code, as well as a fast interface to assure enough memory bandwidth for a smooth and uninterrupted SoC operation. The MicroZed board includes two 16-bit DDR3 memories connected as one 1GB 32-bit memory module. The memory is connected to the hard memory controller in the Zynq-7000 AP SoC Processor Subsystem (PS).

The logiCVC-ML Compact Multilayer Video Controller IP core drives a common PC monitor through the ADV7511 – High-Definition Multimedia Interface (HDMI®) transmitter available on the MicroZed Embedded Vision Carrier Card Kit. The logiCVC-ML automatically handles the full HD graphics background layer and the video overlay.

The logiFDT IP core is a template matching hardware accelerator that significantly off-loads the Zynq SoC processing system and improves the face tracking speed. The accelerator fetches a template (image pattern) and source images from the memory, makes cross-correlation between each corresponding pixel in the template and the source image, and finds the most probable match between the source and the template image. The matching is examined by stepping the template image in one pixel steps (left-right and top-down) over the whole source image (Figure 5).


**Figure 5: Pattern Matching – Principle Illustration**

# 5 SDSOC PLATFORM

Xylon's **evk_fdt** platform (see Fig 3) for the targeted hardware kit follows Xilinx's SDSoC platform design specifications [REF 2].

The following Zynq SoC resources are not used by the **evk_fdt** platform and can be used for other purposes within the SDSoC development environment:

- Clocks:
  - Clock id 2 (default): 100 MHz
  - Clock id 3: 120 MHz
- PS-PL ports:
  - M_AXI_GP1
  - S_AXI_GP0
  - S_AXI_GP1
  - S_AXI_HP1
  - S_AXI_HP3
  - S_AXI_ACP over axi_acp interconnect, see chapter 5.2
- Interrupts:
  - Over xlconcat IP, ports from 3 to 15

The Xylon **evk_fdt** platform supports standalone applications and contains precompiled standalone drivers for the included logicBRICKS IP cores. IP software drivers' source files are included within the reference design deliverables – please see the Table 1 in Chapter 8.4.

The provided platform also includes the pre-built SoC bitstream for faster user workflow described in [REF 3]. The bitstream enables users to run and verify custom developed applications, entirely in software and without engaging in the lengthy process of hardware implementation. However, that process cannot be used with the provided demo application as it is using an HDL-defined and preconfigured IP from a C-callable IP library for application acceleration. Alternatively, user can generate bitstream for the Face Detection and Tracking application and then uncheck the **Generate Bit Stream.** It will enable the tools to rebuild only software portions of the design.

## 5.1 Using evk_fdt SDSoC platform and logiFDT IP core

To get more information about the demo setup, please check the Chapter 6 and **readme.html** file in the reference demo installation folder.

Please copy the **evk_fdt** platform folder to folder **<SDSoC_install_dir>/platforms** within your SDSoC installation folders.

## 5.2 Using and configuring logiFDT IP core

In the provided software demo application, the C-function **`fdtu_match_template_hw (fdt_util.cpp)`** serves for the communication with the face tracking accelerator and as an instruction to the SDSoC compiler to instantiate the logiFDT IP core into the provided **`evk_fdt`** platform.

The logiFDT IP core is used by the face tracking engine and user does not need to change anything related to the accelerator call.

The logiFDT IP core is packaged as a C-callable IP for the SDSoC development environment. It is warped in Xilinx Vivado compatible IP-XACT format and includes additional description files and caller function prototype compiled by the **`sdslib`** tool [REF 2]. The associated C-callable IP project is called **`logifdt_lib`** and it is an imported makefile project in the SDSoC GUI.

User can configure the logiFDT IP core's parameters, which are described in the logiFDT IP core's user's manual, by editing the **`fdtu.params.xml`** file. Each logiFDT IP core generic parameter has an assigned default value from the defined range of valid parameter values. If some generic parameter is not listed in the **`fdtu.params.xml`**, a default generic parameter's value is assumed. Use a clean build of the library project in order to apply generic parameters.

## 5.3 Terminate SDSoC exported unused ACP port

The **`axi_acp`** AXI Interconnect block in the Xilinx Vivado Block Design (Figure 6) contains one unconnected Slave AXI port, S00_AXI (ACP). The SDSoC uses the S00_AXI port to connect user-generated logic to cache-coherent memory space. Xylon demo uses this port to connect the logiFDT Face Detector and Tracker IP core.

If you are using the Xylon platform files without the logiFDT IP core, please make sure to terminate the AXI S00_AXI port, or the Validate design phase will generate an error. If you connect some other cache-coherent IP core to that port and use Xylon platform files, no errors shall be generated.

Otherwise, to properly terminate the port, open platform's Vivado Block design and connect the S00_ACLK and the S00_ARESETN as shown by Figure 6. It is advised to connect the S00_ACLK port to the same clock net as the ACLK port. Similarly, the S00_ARESETN port should be connected to the same net as S01_ARESETN port.

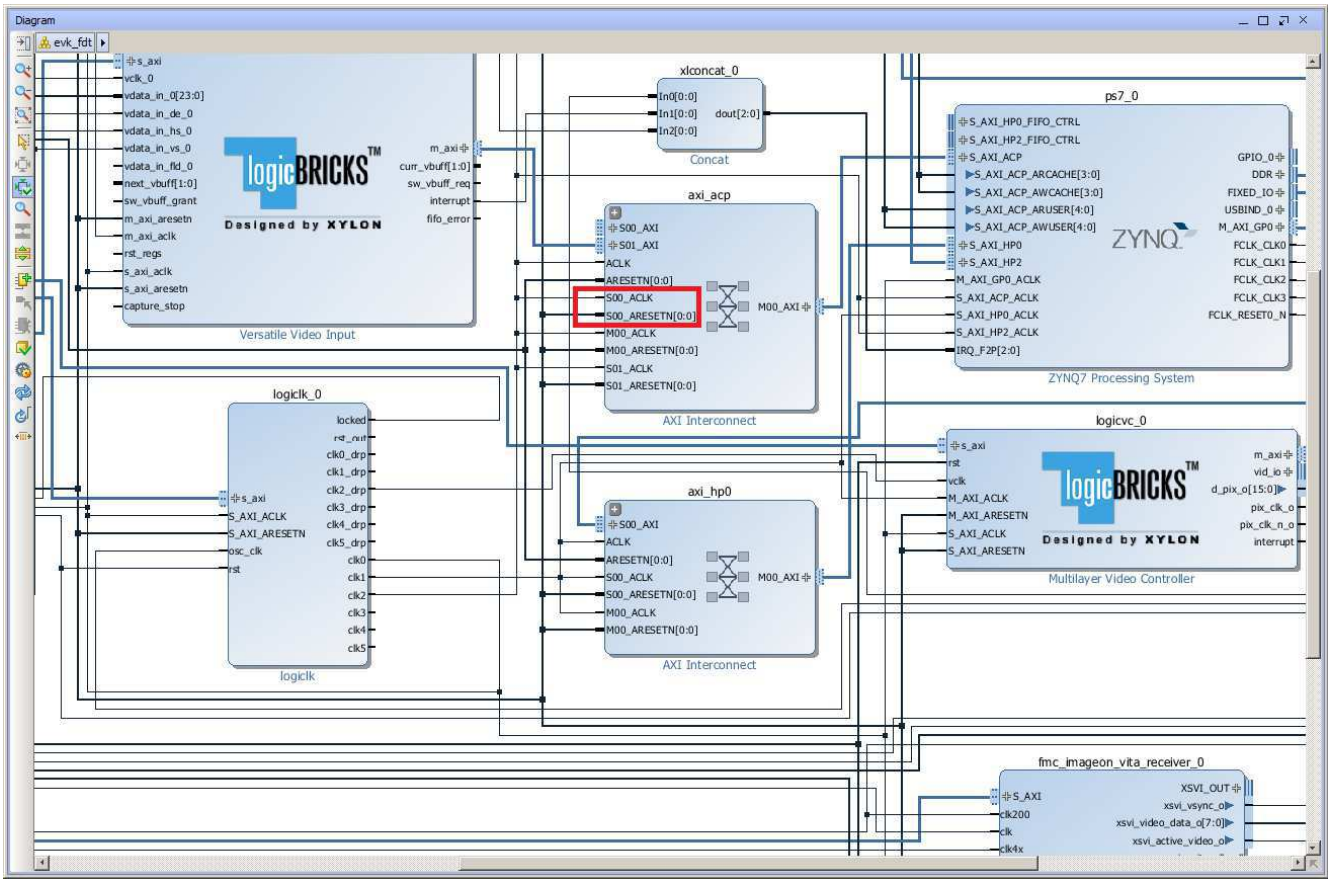



**Figure 6: Terminated S00_ACLK and S00_ARESETN Ports**

# 6 QUICK START

## 6.1 Set up the MicroZed Embedded Vision Kit for Use with the Demo

Xylon provides the demo binaries in the **`binaries/bin`** folder of the delivery. In order to quickly run the precompiled Xylon demo, please copy the contents of the **`binaries/bin`** folder to the root folder on the FAT32 formatted SD card and use it with the hardware kit. The programmed SD card's root folder should look as shown by the Figure 7.

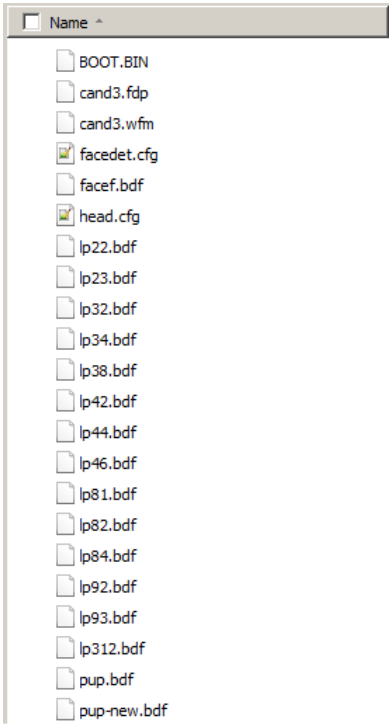



**Figure 7: The Contents of Properly Programmed SD Card**

Set up your MicroZed Embedded Vision Kit as follows:

- Plug the programmed SD card into the micro SD card connector J6 on the MicroZed board
- Select the MicroZed configuration mode by setting up JP1-JP3 jumpers as shown on Figure 8. The presented setup selects the SD card as the boot device.
- Plug the MicroZed board into the Carrier Card board, as shown on Figure 9
- Attach the On Semiconductor PYTHON-1300 camera module to the MicroZed Carrier Card, as shown on Figure 10
- Connect the Full HD (1920x1080) PC monitor and the Carrier Card (HDMI OUT CONN3) by the HDMI video cable
- connect the 5VDC power supply to the Carrier Card

Figure 8: The MicroZed Board Jumpers Settings

Figure 9: The MicroZed Board Plugged In the Carrier Card

Figure 10: The PYTHON-1300 Camera Module Plugged In the Carrier Card

## 6.2 Running the Precompiled Demo from the SD Card Image

To quickly start the precompiled Face Detection and Tracking demo, make sure that you have the SD card with the precompiled image plugged in the board's slot and all jumpers setup as described in the previous paragraph.

The demo supports two tracking modes: single face tracking and detection of multiple faces. To switch between these modes, please push the SW1 push-button on the MicroZed board.

# 7 LOGICBRICKS IP CORES

## 7.1 About logicBRICKS IP Library

Xylon's logicBRICKS IP core library provides IP cores optimized for Xilinx All Programmable devices. logicBRICKS IP cores shorten development time and enable fast design of complex embedded systems based on Xilinx All Programmable devices.

The key features of the logicBRICKS IP cores are:

- Compatibility* with the Xilinx Vivado and ISE Design Suites – logicBRICKS can be used in the same ways as Xilinx IP cores and require no skills beyond general tools knowledge. IP core feature sets and programmable logic utilization can be setup through Xilinx tool GUI.
- Each logicBRICKS IP core comes with the extensive documentation, reference design examples and can be evaluated on reference hardware platforms. Xylon provides evaluation logicBRICKS IP cores to enable risk-free evaluation prior to purchase.
- Broad software support – from bare-metal software drivers to standard software drivers for different operating systems (OS).
- Xylon assures skilled technical support.

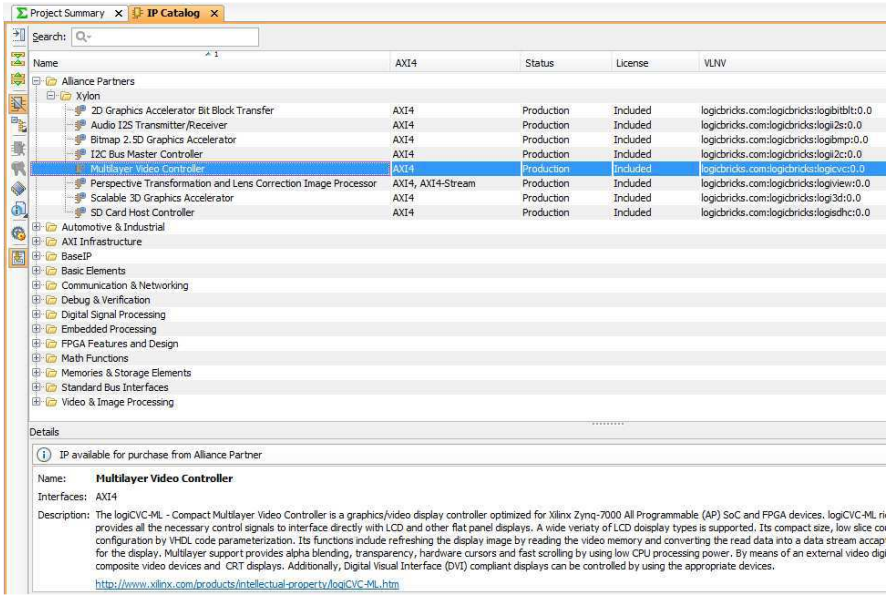



**Figure 11: logicBRICKS IP Cores in the Vivado IP Catalog**

** Some of the latest logicBRICKS IP cores are provided in the Vivado compatible version only. Please visit our web site, or contact Xylon to learn more about the tools compatibility of the specific logicBRICKS IP core.*

Figure 11 shows imported logicBRICKS IP cores into Vivado Design Suite, while the **Error! Reference source not found.** shows a typical logicBRICKS IP core's configuration GUI.

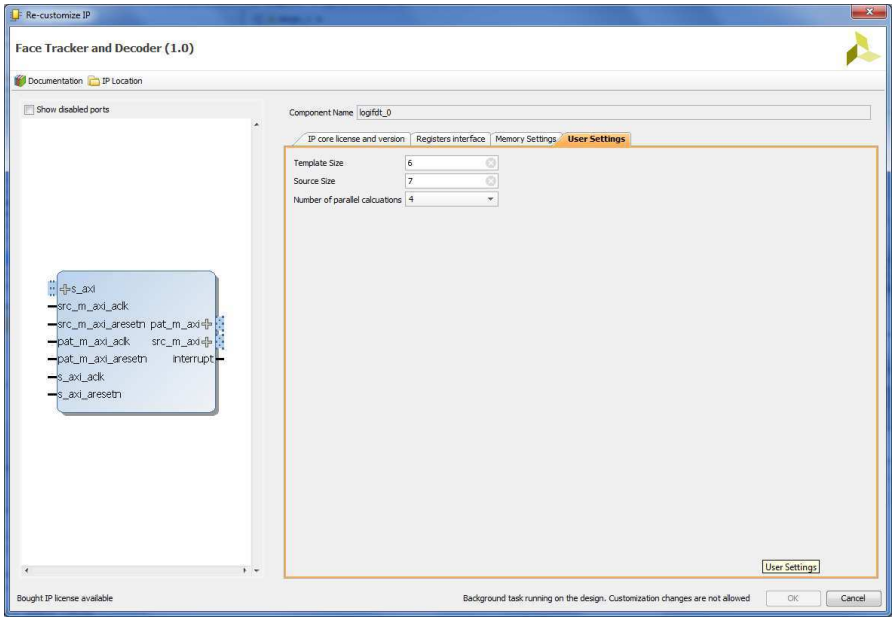



**Figure 12: Example of logicBRICKS IP Configuration GUI**

**: Example of logicBRICKS IP Configuration GUI**

Click on the Documentation icon in the GUI opens the User's Manual of the logicBRICKS IP core!

## 7.2 Evaluation logicBRICKS IP Cores

Xylon offers free evaluation logicBRICKS IP cores which enable full hardware evaluation:

- Imported into the Xilinx ISE Platform Studio (XPS) and Vivado IP Integrator (IPI)
- IP parameterization through the tool GUI interface
- Bitstream generation
- If you need to simulate logicBRICKS IP cores, please contact Xylon

The logicBRICKS evaluation IP cores are run-time limited and cease to function after some time. Proper operation can be restored by reloading the bitstream. Besides this run-time limitation, there are no other functional differences between the evaluation and fully licensed logicBRICKS IP cores.

Evaluation logicBRICKS IP cores are distributed as parts of the Xylon reference designs: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design.aspx.

Specific IP cores can be downloaded from Xylon's web shop:

http://www.logicbricks.com/Products/IP-Cores.aspx.

## 7.3 logicBRICKS IP Cores Used in This Design

### 7.3.1 logiFDT Face Detector and Tracker

The logiFDT Face Detector and Tracker IP core finds and tracks the face and facial features in video sequences in real time and returns full 3D head pose, gaze direction, facial features coordinates and a wealth of other information that can be used in different applications developed on top of it.

- Supports Xilinx Zynq-7000 All Programmable SoC
- Real-time face and facial features tracking in video sequences from a camera or a file
- Easy-to-Use API for accessing the tracking data:
    - 3D head pose (translation and rotation)
    - Gaze direction and eye closure
    - Facial feature coordinates in global 3D space
    - Feature points specified according to the MPEG-4 FBA standard
    - Action units describing the current facial expressing, i.e. brow raise, lips stretch, jaw drop, etc.
    - 3D model of the face in current pose and expression returned as single textured 3D triangle mesh
    - Other tracking data...
- Fully automatic operation and robust recovering from losses due to occlusions, face turning away and similar
- Tracking internally works on a single-channel YUV video (Y-luminance component used), which can be recorded by color, grayscale and infrared camera. For thermal video info, please contact Xylon
- Carefully hardware/software partitioned to assure maximal performance and minimal resources utilization
- The tracking engine uses single ARM Cortex-A9 CPU core supported by hardware acceleration of the most used computing intensive operations implemented in programmable logic
- The required Zynq-7000 AP SoC resources utilization and achievable performance allows for parallel execution of other real-time vision applications on the same SoC
- Parametrical VHDL design that allows tuning of slice consumption and features set
- Prepackaged for Xilinx Vivado Design Suite and fully controllable through the IP Integrator GUI interface
- IP deliverables include the software driver, documentation and technical support

More info: http://www.logicbricks.com/Products/logiFDT.aspx
Datasheet: http://www.logicbricks.com/Documentation/Datasheets/IP/logiFDT_hds.pdf

### 7.3.2 logiCVC-ML Compact Multilayer Video Controller

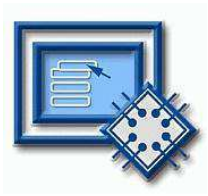
The logiCVC-ML IP core is an advanced display graphics controller for LCD and CRT displays, which enables an easy video and graphics integration into embedded systems with Xilinx Zynq-7000 All Programmable SoC and FPGAs.

This IP core is the cornerstone of all 2D and 3D GPUs. Though its main function is to provide flexible display control, it also includes hardware acceleration functions: three types of alpha blending, panning, buffering of multiple frames, etc.

- Supports all Xilinx FPGA families
- Supports LCD and CRT displays (easily tailored for special display types)
- 64x1 to 2048x2048 display resolutions
- Available SW drivers for: Linux, Android, QNX and Microsoft Windows Embedded Compact OS
- Support for higher display resolutions available on request
- Supports up to 5 layers; the last one configurable as a background layer
- Configurable layers' size, position and offset
- Alpha blending and Color keyed transparency
- Pixel, layer, or Color Lookup Table (CLUT) alpha blending mode can be independently set for each layer
- Packed pixel layer memory organization:
    - RGB – 8-bpp, 8-bpp using CLUT, 16bpp Hi-color RGB 565 and True-color 24bpp
    - YCbCr – 16bpp (4:2:2) and 24bpp (4:4:4)
- Configurable CoreConnect™ PLBv4.6, Xylon XMB or ARM® AMBA® AXI4 memory interface data width (32, 64 or 128)
- Programmable layer memory base address and stride
- Simple programming due to small number of control registers
- Support for multiple output formats:
    - Parallel display data bus (RGB): 12x2-bit, 15-bit, 16-bit, 18-bit or 24-bit
    - YCbCr 4:4:4 or 4:2:2 output format
    - Digital Video ITU-656: PAL and NTSC
    - LVDS output format: 3 or 4 data pairs plus clock
    - Camera link output format: 4 data pairs plus clock
    - DVI output format
- Supports synchronization to external parallel input
- Versatile and programmable sync signals timing
- Double/triple buffering enables flicker-free reproduction
- Display power-on sequencing control signals
- Parametrical VHDL design that allows tuning of slice consumption and features set
- Available for Xilinx Vivado IP Integrator and ISE XPS implementation tools

More info: http://www.logicbricks.com/Products/logiCVC-ML.aspx
Datasheet: http://www.logicbricks.com/Documentation/Datasheets/IP/logiCVC-ML_hds.pdf

### 7.3.3 logiWIN Versatile Video Input

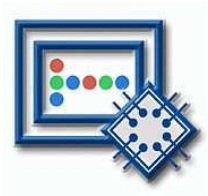


The logiWIN IP core enables easy implementation of video frame grabbers. Input video can be decoded, real-time scaled, de-interlaced, cropped, anti-aliased, positioned on the screen…

- Supports Xilinx Zynq-7000 AP SoC and FPGAs
- Maximum input and output resolutions 2048x2048
- Supports different input interface standards:
    - ITU656 and ITU1120 (PAL and NTSC)
    - RGB
    - YUV 4:2:2
- Built-in YCrCb to RGB, YUV to RGB and RGB to YCrCb converters
- Real-time scale-up to 64x and scale-down to 16x; lossless scaling down to 2x or 4x in the cascade scaling mode
- Supports video de-interlacing, cropping, positioning, pixel alpha blending...
- Embedded image color enhancements: brightness, contrast, hue, saturation
- ARM AMBA AXI4 and AXI4-Lite bus compliant
- Available for Xilinx Vivado IP Integrator and ISE XPS implementation tools

More info: http://www.logicbricks.com/Products/logiWIN.aspx
Datasheet: http://www.logicbricks.com/Documentation/Datasheets/IP/logiWIN_hds.pdf

### 7.3.4 logiBAYER Color Camera Sensor Bayer Decoder



Converts Bayer color coded video inputs into RGB video. Supports all possible Bayer patterns. Supports input resolutions up to 4096x4096 (including 4K2K). Also supports input video scaling.

- Supports Xilinx Zynq-7000 AP SoC and FPGAs
- Converts camera sensor video from Bayer color space to RGB or YCrCb 4:2:2
- Supports all possible Bayer pattern combinations (first two pixels: BG, RG, GB, GR)
- Maximum input and output resolutions 4096x4096
- Supports different input interface standards:
    - Parallel – data, control and clock signals
    - AXI4-Stream – AXI4 compliant video interface
    - LVDS – 1:12 deserialization with embedded clock
- Supports different output interface standards:
    - Parallel – data, control and clock signals
    - AXI4-Stream – AXI4 compliant video interface
    - Memory – XMB, PLBv46, NPI and AXI4
- Cropping two pixels or two lines from each side of the input image
- RGB (24-bit RGB888 or 32-bit ARGB8888) or YCrCb (16-bit 4:2:2) output color representation
- Available for Xilinx Vivado IP Integrator and ISE XPS implementation tools

More info: http://www.logicbricks.com/Products/logiBAYER.aspx
Datasheet: http://www.logicbricks.com/Documentation/Datasheets/IP/logiBAYER_hds.pdf

### 7.3.5 logiCLK Programmable Clock Generator

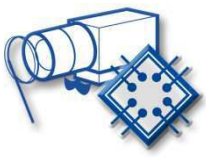
The logiCLK is a programmable clock generator IP core featuring twelve independent and fully configurable clock outputs. While six clock outputs can be fixed by generic parameters prior to the implementation, the other six clock outputs can be either fixed by generics or dynamically reconfigured in a working device. The Dynamic Reconfiguration Port (DRP) interface gives system designers the ability to change the clock frequency and other clock parameters while the design is running by mean of a set of PLL registers.

- Supports Xilinx Zynq-7000 All Programmable SoC, 7 series and Spartan®-6 FPGAs
- Provides 12 independent clock outputs that can be configured by generic parameters:
  - 6 outputs can be dynamically configured through the DRP interface
  - 6 outputs can be configured by generics only
- Input clock frequency range*:
  - Spartan-6: 19 – 540 MHz
  - 7 series: 19 – 1066 MHz
- Output clocks frequency range*:
  - Spartan-6: 3.125 – 400 MHz
  - 7 series: 6.25 – 741 MHz
- Configurable ARM AMBA AXI4-Lite and CoreConnect PLBv46 compliant registers interface
- Software support for Linux and Microsoft Windows Embedded Compact operating systems
- Available for Xilinx Vivado IP Integrator and ISE Platform Studio

** Depending on the used device's speed grade*

More info: http://www.logicbricks.com/Products/logiCLK.aspx
Datasheet: http://www.logicbricks.com/Documentation/Datasheets/IP/logiCLK_hds.pdf

## 7.4 logicBRICKS IP Cores for Video Processing



The logiISP Image Signal Processing Pipeline IP core is a full high-definition ISP pipeline designed for digital processing and image quality enhancements of an input video stream in Smarter Vision embedded designs based on Xilinx Zynq-7000 All Programmable SoC and 7 Series FPGA devices.

More info: http://www.logicbricks.com/Products/logiISP.aspx
Datasheet: http://www.logicbricks.com/Documentation/Datasheets/IP/logiISP_hds.pdf

The logiISP Image Signal Processing (ISP) Pipeline IP core can be combined with the logiFDT Face Detector and Tracker in order to enhance the video quality prior to the face tracking processing.

The logiISP IP core accepts diversely formatted video inputs generated by different sensors and removes defective pixels, de-mosaics Bayer encoded video, makes image color and gamma corrections, filters the noise from the video, collects video analytics data for various control algorithms and manipulates video data formats and color domains. The IP core can be used with processor-based control algorithms for Auto White Balancing (AWB) and Auto Exposure (AE) that can be licensed from Xylon.

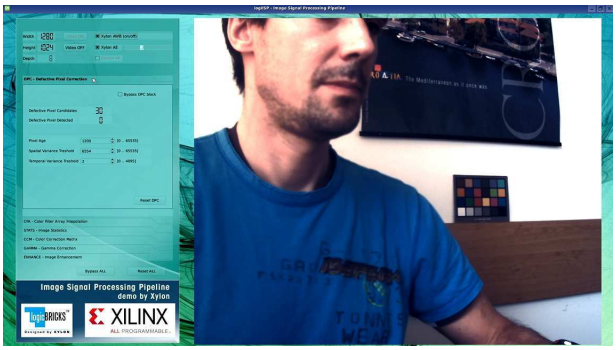



**Figure 13: Screenshots from the Xylon logiISP Demo (logiREF-VIDEO-ISP-EVK)**

To get Xylon free ISP reference design, please visit:

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/ISP-Pipeline-for-Xilinx-All-Programmable.aspx

To learn more about other Xylon logicBRICKS IP cores for the video processing, please visit:

http://www.logicbricks.com/Products/IP-Cores.aspx

## 7.5 logicBRICKS IP Cores for Graphical User Interface (GUI)

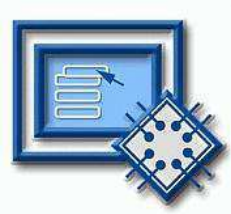
Xylon's logicBRICKS library of IP cores optimized for Xilinx All Programmable devices includes several graphics logicBRICKS IP cores for full range implementation of 2D and 3D Graphics Processing Units (GPU) on Xilinx Zynq-7000 All Programmable SoC and FPGAs. Xylon's graphics logicBRICKS IP cores can be quickly combined with the graphic processing IP cores when it is necessary to support complex GUI interfaces. Graphics logicBRICKS IP cores are well supported by Xylon provided software drivers for the most popular operating systems: Linux, Android™, QNX® and Microsoft® Windows® Embedded Compact. A number of Xilinx partners who provide BSPs (Board Support Package) for different operating systems support Xylon logicBRICKS IP cores for graphics.

To get Xylon free GUI reference designs, please visit:
http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design.aspx

To learn more about the available software support for graphics logicBRICKS IP cores, please visit:

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/OS-IP-Core-Support.aspx

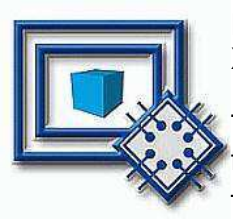
### logiBITBLT Bit Block Transfer 2D Graphics Accelerator



This 2D graphics accelerator speeds up the most common GUI operations and off-loads the processor. The logiBITBLT transfers graphics objects from one to another part of system's on-screen or off-screen video memory, and performs different operations during transfers, such as ROP2 raster operations, bitmap scaling (stretching) and flipping, Porter & Duff compositing rules or transparency.

More info: http://www.logicbricks.com/Products/logiBITBLT.aspx
Datasheet: http://www.logicbricks.com/Documentation/Datasheets/IP/logiBITBLT_hds.pdf

### logi3D Scalable 3D Graphic Accelerator



The logi3D* Scalable 3D Graphics Accelerator IP core is a 3D Graphics Processing Unit (GPU) IP core developed for embedded systems based on the Xilinx Zynq-7000 All Programmable SoC.

The IP is designed to support the OpenGL ES 1.1 API specifications – a royalty-free, cross-platform API for full-function 2D and 3D graphics on embedded systems – including consoles, phones, appliances and vehicles.

** Product is based on a published Khronos specification, and is expected to pass the Khronos Conformance Testing Process. Current conformance status can be found at www.khronos.org/conformance.*


**Figure 14: Screenshots from Some Demos Provided with the Reference Designs (logiREF-ZGPU-ZED, logiREF-ZGPU-ZC702 and logiREF-ZGPU-ZC706)**

# 8 GET AND INSTALL THE REFERENCE DESIGN

Xylon offers several logicBRICKS reference designs for different hardware platforms. Short descriptions of all Xylon logicBRICKS reference designs can be found at:

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design.aspx

A quick access to specific reference design is also possible through the main downloads navigation page:

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Xylon-Reference-Designs-Navigation-Page.aspx

Only registered logicBRICKS users can download logicBRICKS reference designs. Unregistered users will be re-directed to the User Login page. The download link is automatically sent by an e-mail, which means that the registration process requires access to the e-mail account. Xylon reference logicBRICKS designs can be downloaded as cross-platform Java JAR self-extracting installers.

For quick registration and other general instructions, please visit:

http://www.logicbricks.com/logicBRICKS/logicBRICKS-Quick-Info.aspx

## 8.1 Registration Process

Registration is very quick and simple. If you experience any troubles during the registration process, please contact Xylon Technical Support Service – support@logicbricks.com.

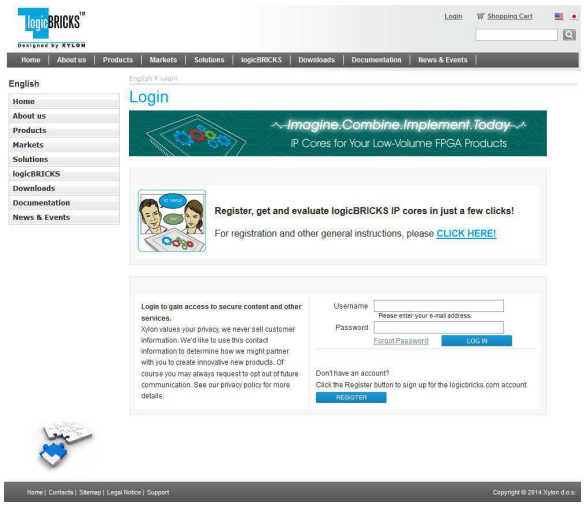



**Figure 15: Registration Process – Step 1**

### Step 1

If you are the registered logicBRICKS user, please type-in your Username and Password. Unregistered users should click on the Register button, which will open the registration form.


**Figure 16: Registration Process – Step 2**

### Step 2

Unregistered users should fill-in the registration form from the Fig 16. Please take care on required form's fields. Your Username is an actual e-mail account used for communication with Xylon logicBRICKS. Xylon accepts only valid company e-mail accounts.


**Figure 17: Registration Process – Step 3**

### Step 3

As soon as your registration form gets accepted by Xylon, you get a confirmation message. Please check your e-mail to find a link that activates your logicBRICKS account. If you do not get the confirmation message in several minutes, please check your Spam Filter or Junk Mail Folder. If you have not received the confirmation message, please contact Xylon support.

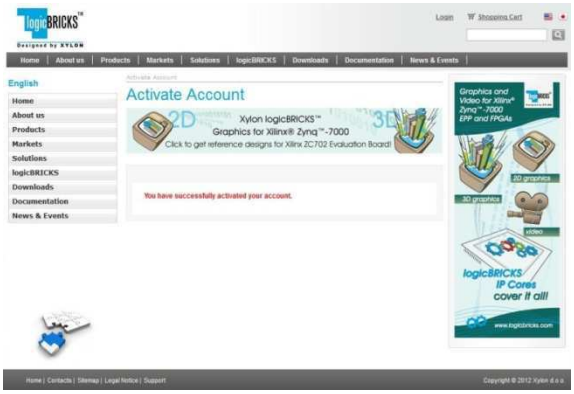



**Figure 18: Registration Process – Step 4**

**Step 4**

Click on the logicBRICKS web account activation link in the received e-mail, and you will get the confirmation status message. Please login to proceed.


**Figure 19: Registration Process – Step 5**

**Step 5**

As soon as you select an appropriate logicBRICKS reference design and installer for your operating system from the Downloads Navigation Page (link bellow), you will get an e-mail with the download link for the selected reference design installation.

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Xylon-Reference-Designs-Navigation-Page.aspx

## 8.2 Installation Process

Installation process is quick and easy. Each logicBRICKS reference design can be downloaded as a cross-platform Java JAR self-extracting installer. Please make sure that you have a copy of the JRE (Java Runtime Environment) version 6 or higher on your system to run Java applications and applets.

Double-click on the installer's icon to run the self-installing executable to unpack and install the reference design on your PC.

At the beginning, you will be requested to accept two evaluation licenses: Figure 20 and Figure 21.

For installation in Linux OS, please follow instructions:

http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Xylon-Reference-Designs-Linux-Installation.aspx.

If you agree with the conditions from the evaluation licenses, click NEXT and select the installation path for your logicBRICKS reference design – Figure 22.

The installation process takes several minutes. It generates the folder structure described in the paragraph 8.3 Folder Structure.

## 8.3 Filesystem permissions of the installed folder (Windows 7)

The reference design installed in the default path **`C:\Program Files\xylon`** will inherit read-only filesystem permissions from the parent directory. This will block you in opening the hardware project file in Xilinx Vivado tools. Therefore it is necessary to change the filesystem permissions for the current user to "Full control" preferably.

To change the user permissions for **`C:\Program Files\xylon`** folder and all of its subfolders, right click on the **`C:\Program Files\xylon`** folder and select "**`Properties`**". Under "**`Security`**" tab select "**`Edit`**". Select "**`Users`**" group in the list and check "**`Full control`**" checkbox in the "**`Allow`**" column.

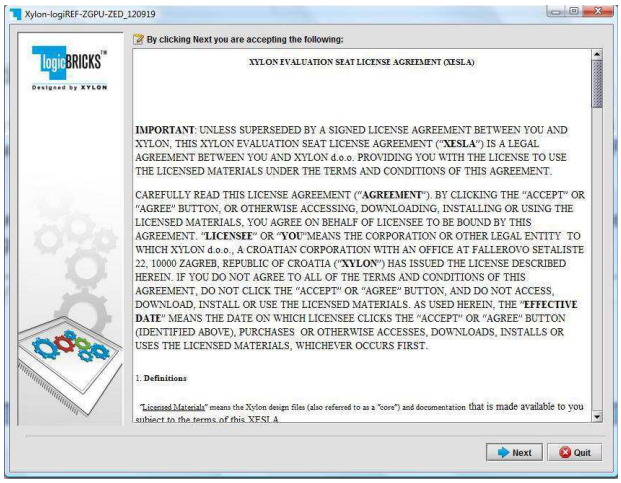



Figure 20: Installation Process – Step 1

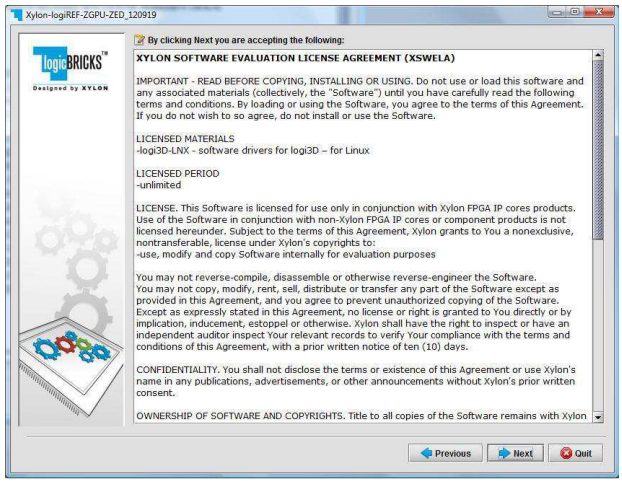



Figure 21: Installation Process – Step 2


Figure 22: Installation Process – Step 3

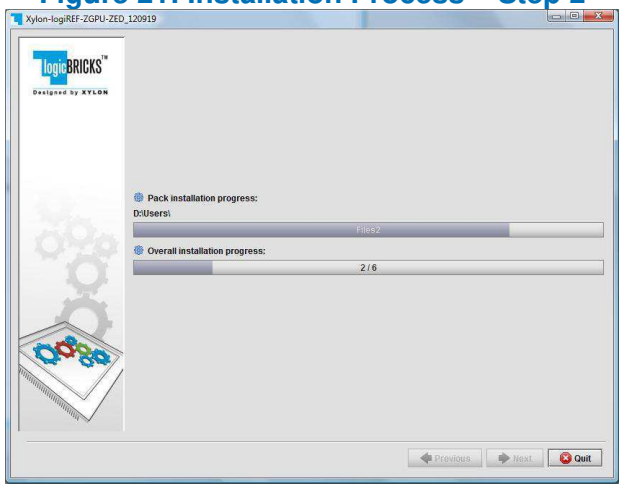



Figure 23: Installation Process – Step 4

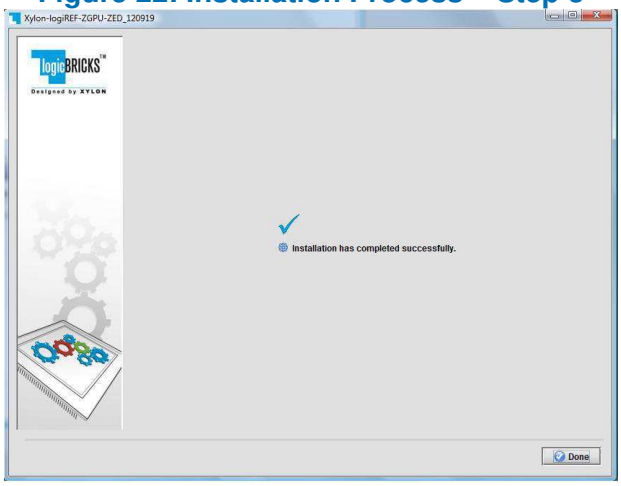



Figure 24: Installation Process – Step 5

## 8.4 Folder Structure

Figure 25 gives a top level view of the folders and files included with the logiREF-SDSoC-FACE-EVK reference design for the MicroZed Embedded Vision development kit. Table 1**Error! Reference source not found.** explains the purpose of folders.

Please use the `start.html` file located in the installation root folder as a jump-start navigation page for exploring the reference design.

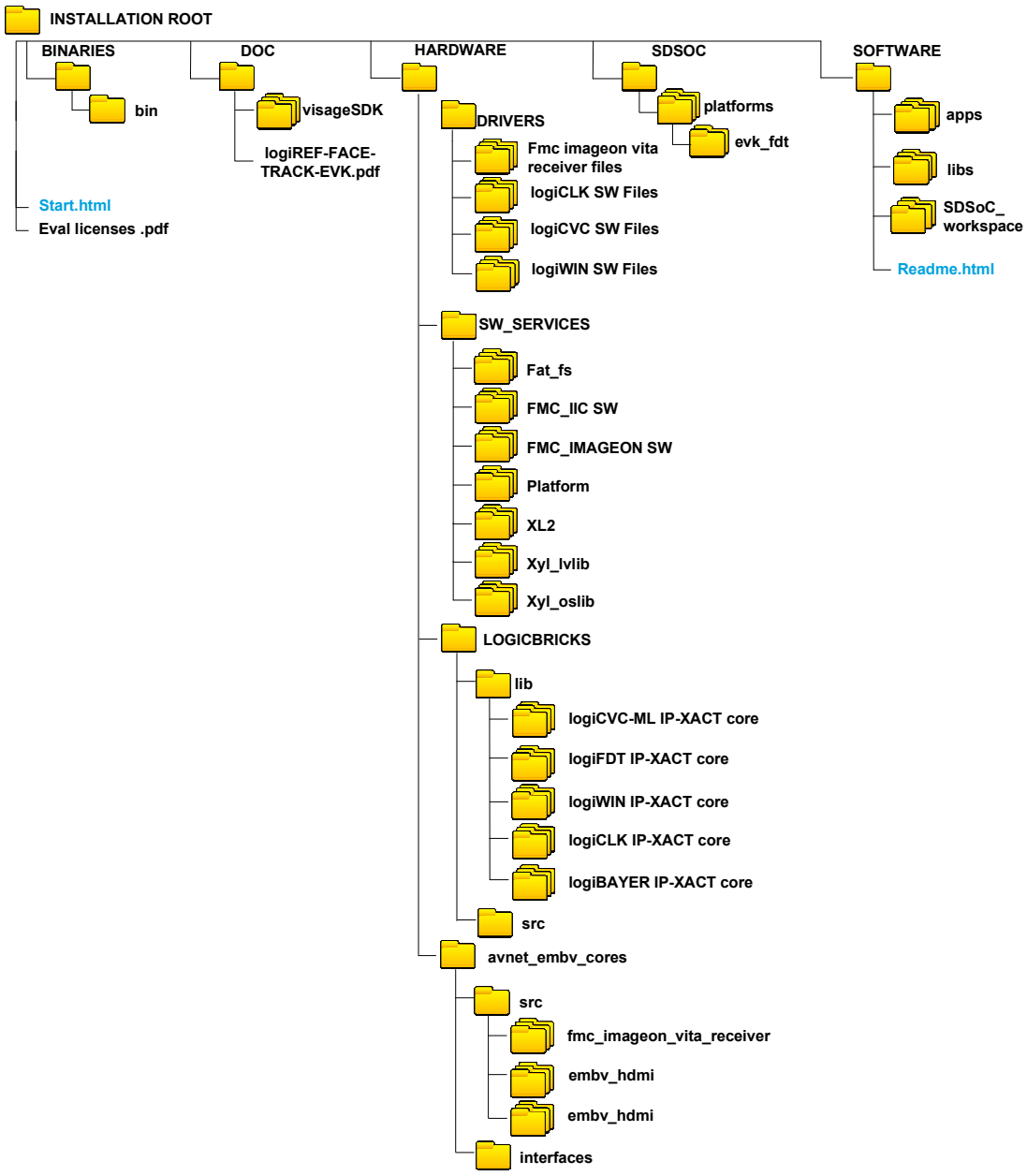



**Figure 25: Installed Reference Design – The Folder Structure**

**Table 1: Explanation of Folders in logiREF-SDSoC-FACE-EVK Reference Design**

| Folder | | Purpose |
|---|---|---|
| `installation root` | | This folder contains the *start.html* page – the jump-start navigation page through the reference design. |
| `binaries` | | Binaries folder. |
| | `bin` | Prepared binaries ready for download to SD card. |
| `doc` | | Project documentation. |
| `hardware` | | |
| | `avnet_embv_cores/src` | Avnet IP-XACT cores |
| | `drivers` | Standalone (bare-metal) drivers for logicBRICKS IP cores with documentation and examples. |
| | `logicbricks/lib` | Evaluation logicBRICKS IP-XACT cores (zip archives). |
| | `logicbricks/src` | Evaluation logicBRICKS IP-XACT extracted IP cores. IP cores' User's Manuals are stored in `doc` subfolders. |
| | `sw_services` | `fat_fs` Open source FAT file system<br>`fmc_iic_sw` Avnet FMC card I2C library<br>`fmc_imageon_sw` Avnet FMC Imageon (sensor) library<br>`platform` Xylon board hardware abstraction library<br>`xl2` Xylon graphical library<br>`xyl_oslib` Xylon OS abstraction library for Xilinx Xilkernel embedded kernel – use in standalone (non-OS) applications. |
| | `design.h` | Hardware description file used by platform. |
| `SDSoC` | | |
| | `platforms` | Location of SDSoC platform files |
| `software` | | |
| | `apps` | Application source files |
| | `libs` | Libraries: EMBV_drv, EMBVPlatform_lib |
| | `SDSoC_workspace` | Xilinx SDSoC workspace folder for building bare-metal applications. |
| | `readme.html` | Navigation page through the software files and instructions for building binaries. |

# 9 GETTING LOGICBRICKS EVALUATION LICENSES

Please note that the logiREF-SDSoC-FACE-EVK reference design installation provides you with everything needed to run the provided demo applications or to use/change the provided software source code. However, to implement any changes to the design files, such as to remove, add or reconfigure some of the provided IP cores, you have to obtain evaluation IP licenses from Xylon.

The following pages describe the procedure for getting and licensing evaluation logicBRICKS IP cores that takes several minutes to complete. If you experience any troubles during this process, please contact Xylon Technical Support Service – support@logicbricks.com.

You must be logged in to the Xylon website using your logicBRICKS user name and password to get an access to evaluation logicBRICKS IP cores. Unregistered users will be re-directed to the User Login page. Paragraph 8.1 Registration Process explains this simple registration procedure.

**Step 1** – Logged in users get the "My logicBRICKS" tab in the main www.logicbricks.com navigation menu. Click on it, and you will be directed to your main web page for communication with Xylon logicBRICKS – Figure 26. Please select the "**Request Eval IP Core**" tab in the left menu.

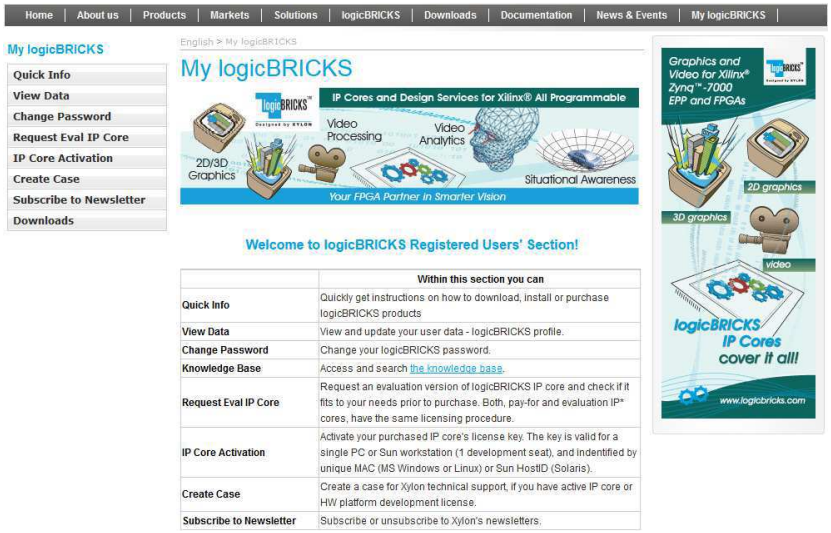



**Figure 26: Step 1 – My logicBRICKS Navigation Page**

**Step 2** – Select the evaluation logicBRICKS IP core and click on "**Obtain evaluation license key**" link – Figure 27. If you are entitled to get the evaluation logicBRICKS IP core, you will be immediately asked (Figure 30) your Ethernet MAC ID number or Sun Host ID – as described in the Step 3.

If the evaluation logicBRICKS IP cores' list looks differently from the one shown on Figure 27, for example as the list presented by the Figure 28, please fill in and submit the request form (Figure 29), and allow us some time to process your request. Scroll down to get to the request form.

For instructions on how to find your Ethernet MAC or host ID, please visit:
http://www.logicbricks.com/Documentation/Article.aspx?articleID=KBA-01186-M0JXKD


**Figure 27: Step 2 – Selecting logicBRICKS IP Core for Licensing**


**Figure 28: Step 2 – A List of Already Activated logicBRICKS IP Licenses**

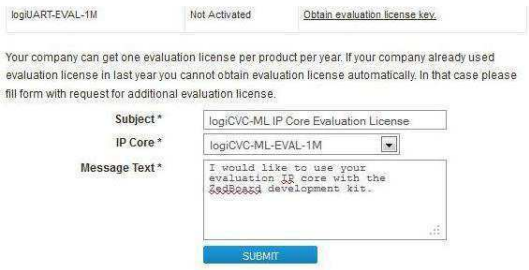



**Figure 29: Step 1 – Licensing logicBRICKS Evaluation IP Cores**

**Step 3** – Evaluation logicBRICKS IP licenses are tied to your Ethernet MAC address or Sun Host ID (Figure 30), and can be used on a single working station only. Fill in this address and click on the "**Request License Key**" button. You should get the confirmation message – Figure 31. If you do not get the confirmation message, please contact Xylon technical support – support@logicbricks.com.

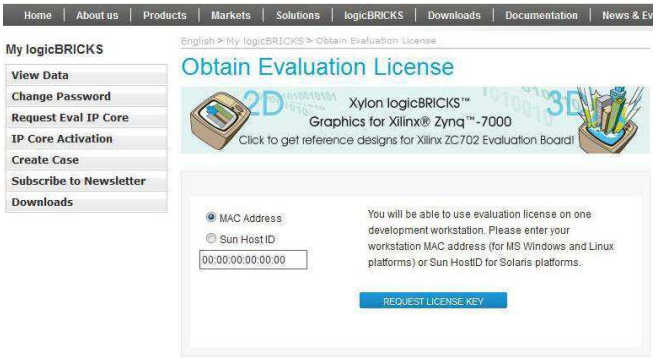



**Figure 30: Step 3 – Licensing logicBRICKS Evaluation IP Cores**


**Figure 31: Step 3 – Confirmation Message**

**Step 4** – You will get an e-mail with the license key (file) and full instructions for setting up the license key and downloading the logicBRICKS IP core. Please follow the provided instructions.

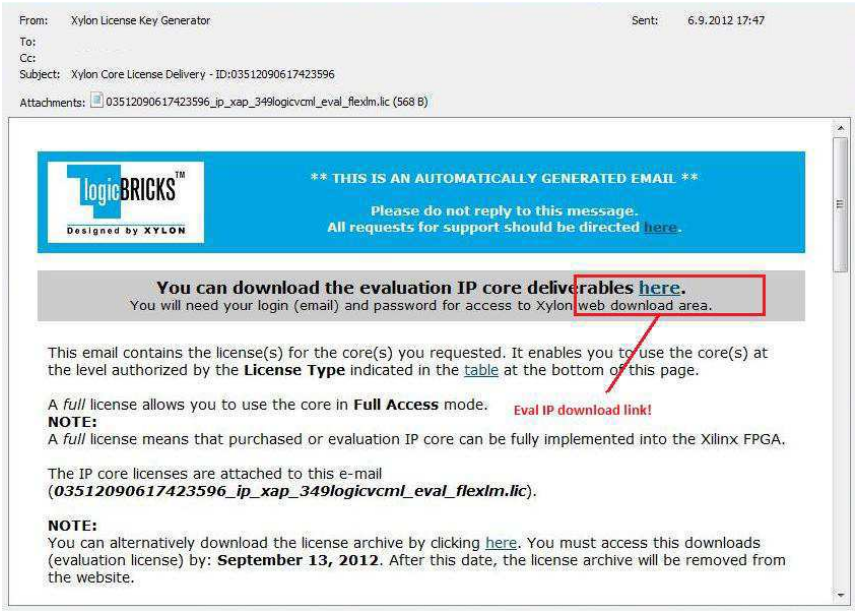



**Figure 32: Step 4 – E-mail with logicBRICKS License and Download Instructions**

# 10 SOFTWARE DOCUMENTATION

## 10.1 logiFDT SDK Documentation

User's Manuals and additional reference manuals that describe the operation of the logiFDT software part are provided in the convenient HTML format. Please open the documentation in your installation folder: **`../doc/visageSDK/doc/Xylon/doc.html`**.

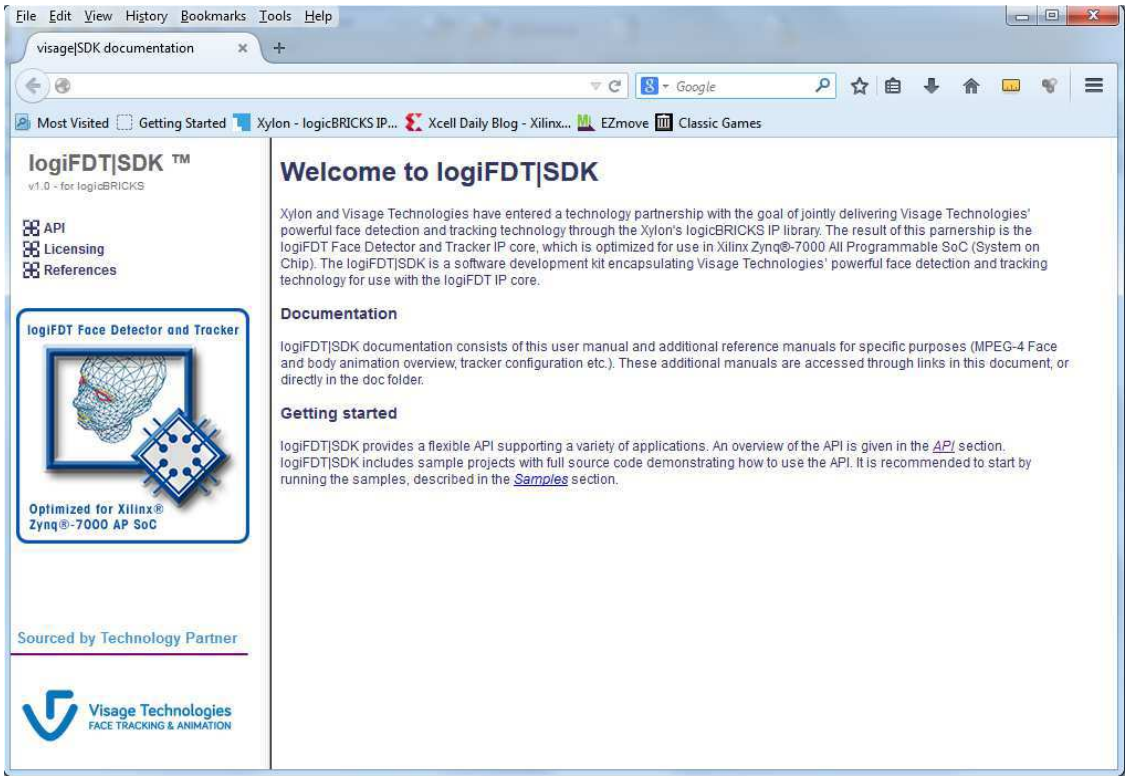



**Figure 33: logiFDT SDK Software Documentation – The Start Page**

## 10.2 logiFDT Tracking Configuration

For the face, the MPEG-4 specification defines 66 low-level Face Animation Parameters (FAPs) and two high-level FAPs. The low-level FAPs are based on the study of minimal facial actions and are closely related to muscle actions. They represent a complete set of basic facial actions, and therefore allow the representation of most natural facial expressions. Exaggerated values permit the definition of actions that are normally not possible for humans, but could be desirable for cartoon-like characters.

To change the profile of the face tracker, please exchange the head.cfg (in the SD card root directory) file with one of the three provided Face Tracker configuration files and restart the kit. The provided profile configuration files are:

- head_high.cfg (high profile configuration file)
- head_mid.cfg (mid profile configuration file)
- head_low.cfg (low profile configuration file)

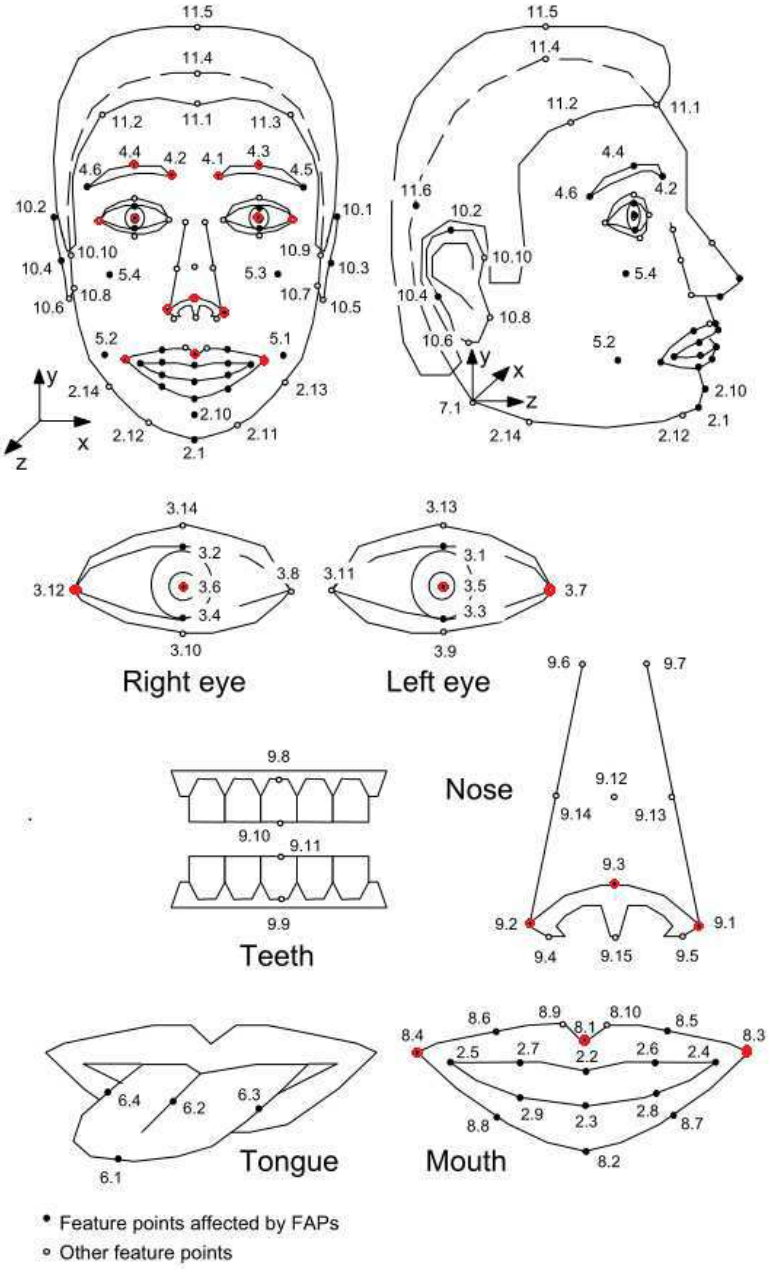



**Figure 34: MPEG-4 FAB Standard Defined Facial Feature Points**

Red dots on Figure 34 mark the facial features tracked by the logiFDT setup with the delivered High-Profile configuration.

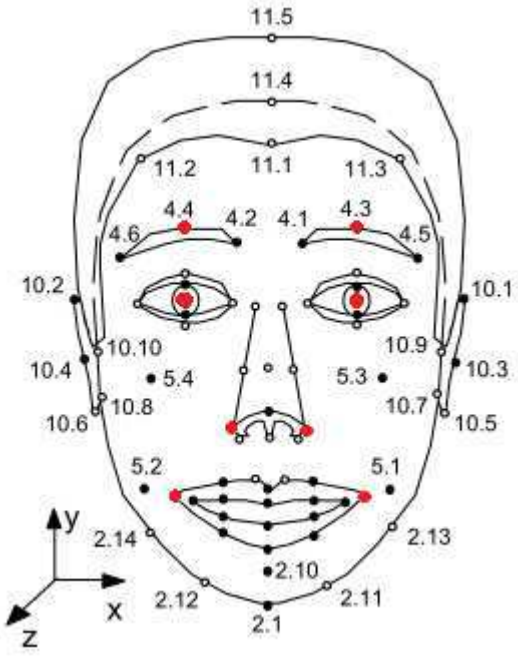



**Figure 35: logiFDT Tracked Points in the Low-Profile Configuration**

## 10.3 Differences to the logiREF-FACE-TRACK-EVK software

The demo application in the logiREF-SDSoC-FACE-EVK reference design consists of two major projects and two smaller library projects. In the logiREF-FACE-TRACK-EVK reference design, which is fully Vivado based version of the Face Detection and Tracking, there are application project and a library project.

The two main projects are a library project that has essentially all of the sources from the logiREF-FACE-TRACK-EVK and an SDSoC project that has application start point and the C-callable IP call. They are partitioned this way because Face Detection and Tracking application uses OpenCV library that is different from the Xilinx's implementation of OpenCV in SDSoC and Vivado HLS. And thus this causes incompatibilities that prevent building of application when configured as single project.

The other two provided projects are C-callable IP library and a utility library.

# 11 REFERENCES

**Table 2: List of References**

| Reference | Description |
|---|---|
| REF [1] | Xylon, logiREF-FACE-TRACK-EVK (logiREF-FACE-TRACK-EVK_v1_01_a.pdf) |
| REF [2] | Xilinx, UG1146 (ug1146-sdsoc_platforms_and_libraries.pdf) |
| REF [3] | Xilinx, UG1027 (ug1027-intro_to_sdsoc.pdf) |

# 12 REVISION HISTORY

| Version | Date | Author | Approved by | Note |
|---|---|---|---|---|
| 1.0.0 | July 20, 2015 | M. Polovic | G. Galic | Initial |
| | | | | |
| | | | | |