3.3 Volt Synchronous 8 Channel Queue

Memory Configuration	Device
131,072 x 40	CQV8110
65,536 x 40	CQV8100
32,768 x 40	CQV890
16,384 x 40	CQV880
8,192 x 40	CQV870
4,096 x 40	CQV860
2,048 x 40	CQV850
1,024 x 40	CQV840

Key Features

- **Single device solution providing complete data queuing and switching functions (up to 166 MHz)**
- **Write cycle time of 6.0ns independent of Read cycle time (Data Setup time = 2.0ns)**
- **Read cycle time of 6.0ns independent of Write cycle time (Data Access time = 4.0ns)**
- **3.3V power supply**
- **5V input tolerant on all control and data input pins**
- **5V output tolerant on all flags and data output pins**
- **5-bit wide data channels, up to sixteen channels per chip (80 bits total)**
- **Reconfigurable data switching supporting channel unicast, multicast and broadcast**
- **Master Reset clears all previously programmed configurations including Write and Read pointers**
- **Partial Reset clears Write and Read pointers but maintains all previously programmed configurations**
- **First Word Fall Through (FWFT) and Standard Timing modes**
- **Presets for eight different Almost Full and Almost Empty offset values**
- **Parallel/Serial programming of $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ offset values**
- **Programmable 8-bit or 10-bit parallel programming modes for offset values**
- **Full, Empty, Almost Full, Almost Empty, and Half Full indicators**
- **$\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ operates in either synchronous or asynchronous modes**
- **Individual synchronous channel output enable signals controlling tri-state data output drivers**
- **Asynchronous device output enable signals controlling tri-state data output drivers**
- **Data retransmission with programmable zero or normal latency modes**
- **Switching management**
- **Available package: 144 - pin Plastic Thin Quad Flat Pack (TQFP)**
- **(0°C to 70°C) Commercial operating temperature available for cycle time of 6.0ns and above**
- **(-40°C to 85°C) Industrial operating temperature available for cycle time of 7.5ns and above**

Product Description

HBA's ChannelQ™ product family represents the next generation bandwidth management solutions by providing advanced data queuing and switching functions within a single chip. System designers can take full advantage of the flexible data switching functions offered by the ChannelQ products while maintaining access to all the advanced features available in HBA's existing FlexQ™ family, such as programmable FIFO status flags, programmable data access timing (First-Word-Fall-Through and Standard modes), data retransmission with programmable latency mode, and tri-state output data drivers.

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Product Description (Continued)

The channel switching capability provides a means for unicast / multicast / broadcast of individual channel data when they are written to the internal FIFO memory. The configuration of the channel switch can be reprogrammed on the fly. Because the device combines data queuing and switching into a single chip, it in effect implements a switching fabric with input data queuing, which has a broad range of applications in data communication. For detailed information on programming and using the ChannelQ™ devices, please refer to the ChannelQ Application Note.

5V tolerant on all input and output pins allow easy interfacing with devices operating at higher voltage levels. Asynchronous Output Enable pin configures the tri-state data output drivers. In addition, synchronous read chip select and synchronous channel output enables are also available to control the state of data output drivers, allowing multiple ChannelQ devices to share a single output data bus. Independent Write and Read controls provide rate-matching capability.

Master Reset clears all previously programmed configurations by providing a low pulse on $\overline{\text{MRST}}$ pin. In addition, Write and Read pointers to the queue are initialized to zero. Partial Reset will not alter previously programmed configurations but will initialize Write and Read pointers to zero.

In FWFT mode, first data written into the queue appears on output data bus after the specified latency period at the low to high transition of RCLK. Subsequent reads from the queue will require asserting $\overline{\text{REN}}$. This feature is useful when implementing depth expansion functions. In this mode, $\overline{\text{DRDY}}$ and $\overline{\text{QRDY}}$ are used instead of $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ respectively.

In Standard mode, always assert $\overline{\text{REN}}$ for a read operation. $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ are used instead of $\overline{\text{DRDY}}$ and $\overline{\text{QRDY}}$ respectively.

Eight different default offset values are available for Almost Full ($\overline{\text{PRAF}}$) and Almost Empty ($\overline{\text{PRAE}}$) flags. Parallel and Serial programming of these offset values provide total flexibility other than the pre-defined default values. Both 8-bit and 10-bit parallel programming modes for offset values can be selected for convenience.

$\overline{\text{PRAF}}$, $\overline{\text{PRAE}}$, and $\overline{\text{HALF}}$ are available in either FWFT or Standard mode. In addition, $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ can operate in either synchronous or asynchronous modes.

At any time, data previously read from the queue can be retransmitted by asserting $\overline{\text{RET}}$ pin at the low to high transition of RCLK for a retransmit operation. Retransmit initializes the Read pointer to zero. Hence, all re-reads will always start from the physical 0^{th} (Read pointer = zero) location of the queue. Both zero and normal latency timing modes are available for retransmit operation.

ChannelQ devices have low power consumption, hence minimizing system power requirements. In addition, industry standard 144 - pin Plastic TQFP is offered to save system board space.

These devices are ideal for applications such as data communication, telecommunication, test equipment, network switching, etc.

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Programming Modes

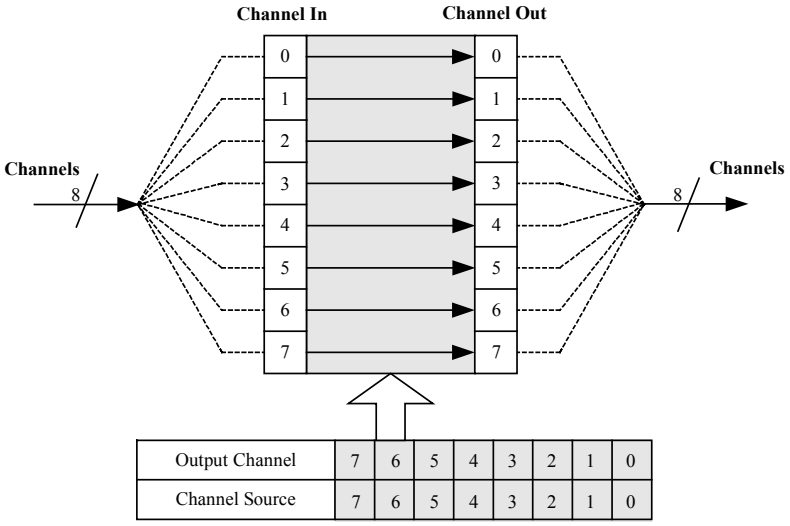

Figure 1. 8x5-to-8x5 ChannelQ Configured in Unicast Mode

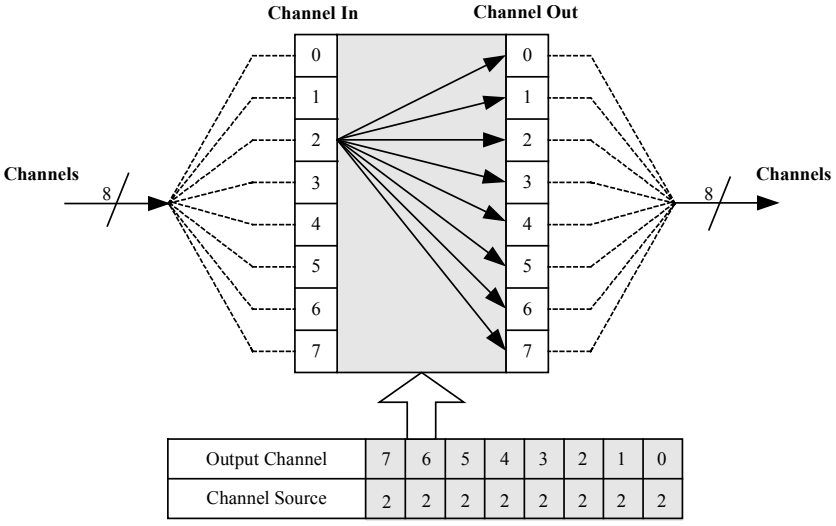

Figure 2. 8x5-to-8x5 ChannelQ Configured in Broadcast Mode

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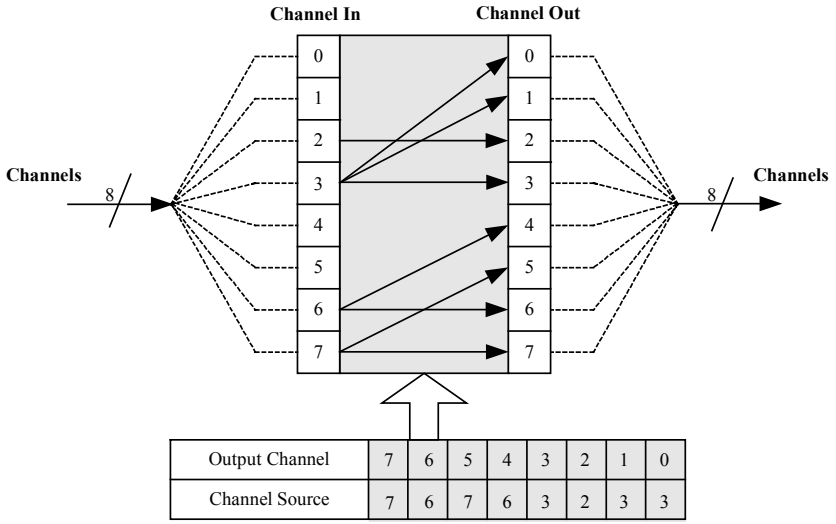

Figure 3. 8x5-to-8x5 ChannelQ Configured in Multicast Mode

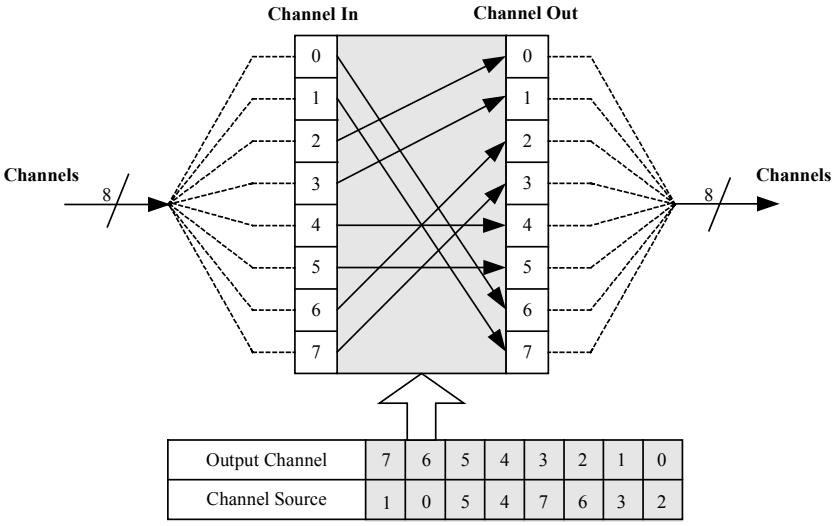

Figure 4. 8x5-to-8x5 ChannelQ Configured as a 4x10-to-4x10 Switch in Switching Mode

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Block Diagram of Single Channel Queue
131,072 x 40 / 65,536 x 40 / 32,768 x 40 / 16,384 x 40 / 8,192 x 40 / 4,096 x 40 / 2,048 x 40 / 1,024 x 40

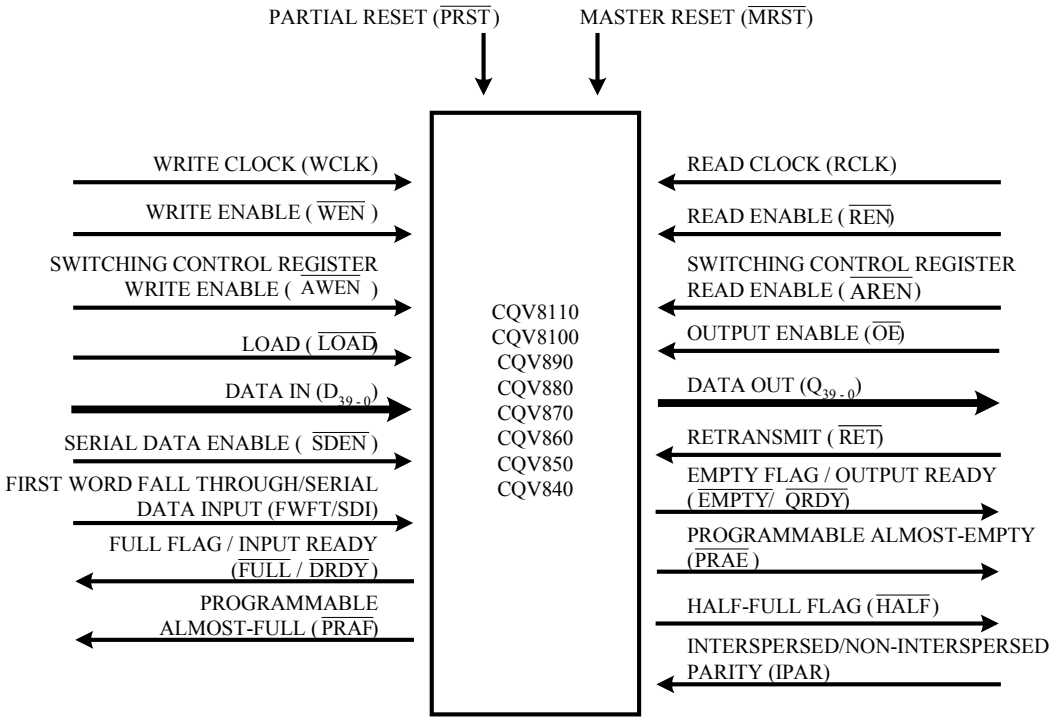

Figure 5. Single Device Configuration Signal Flow Diagram

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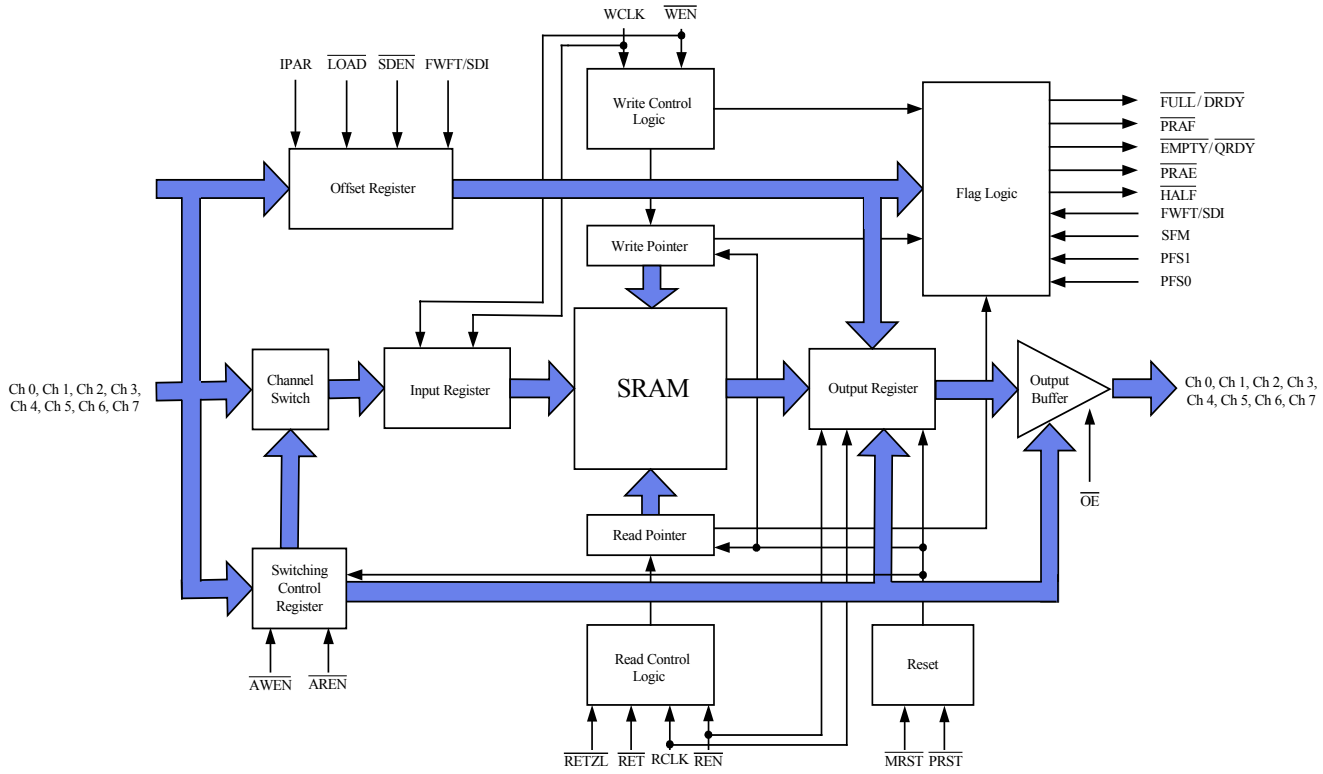

Figure 6. ChannelQ Device Architecture

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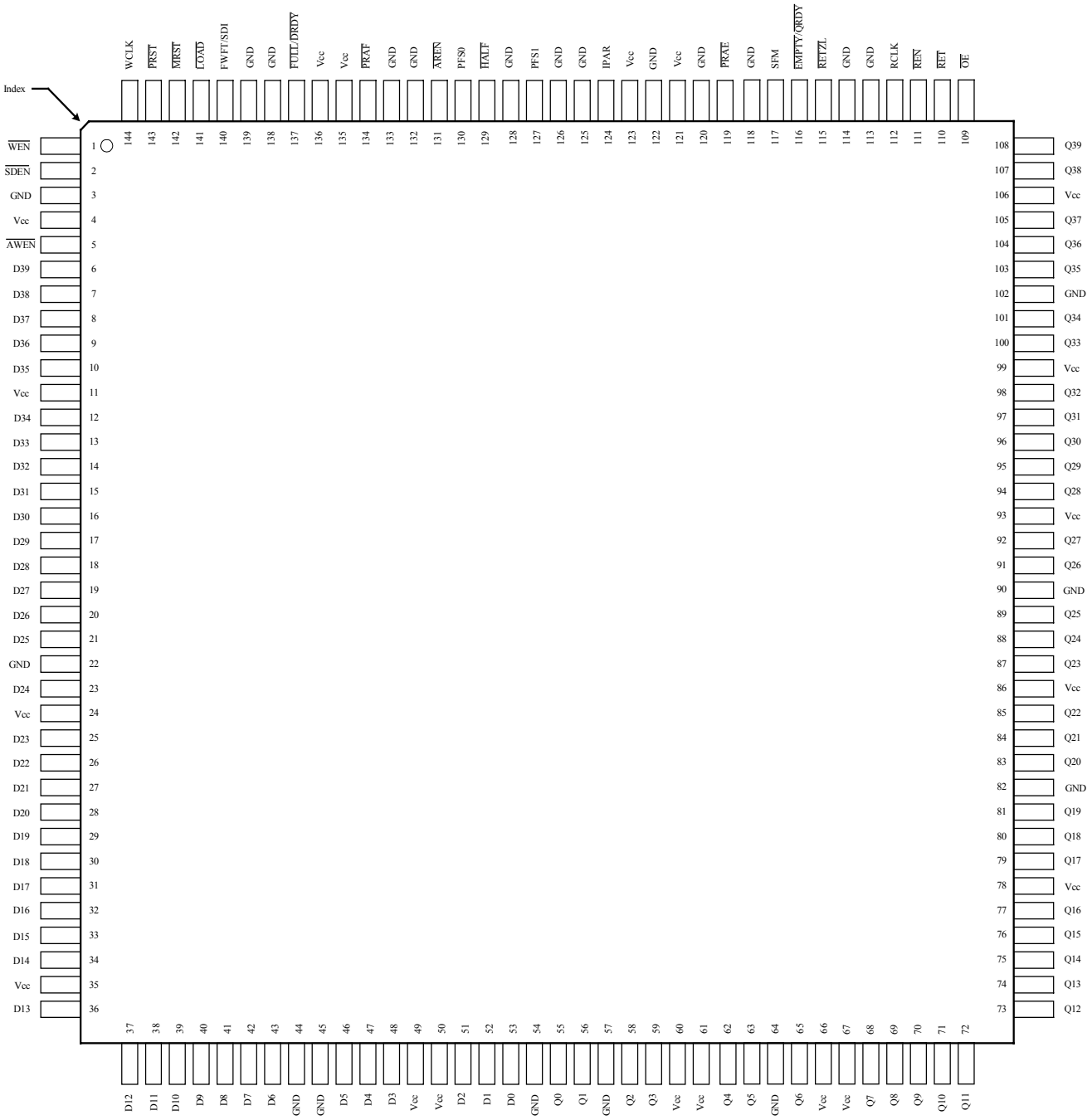

TQFP - 144 (Order code: PF)
Top View

Figure 7. Device Pin Out

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Pin #	Pin Name	Pin Symbol	Input/Output	Description
142	Master Reset	$\overline{MRST}$	Input	Master Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{MRST}$ low. In Standard mode, $\overline{FULL}$ and $\overline{PRAF}$ will go high; $\overline{EMPTY}$ and $\overline{PRAE}$ will go low. In FWFT mode, $\overline{DRDY}$ will go low and $\overline{QRDY}$ will go high. $\overline{PRAF}$ and $\overline{PRAE}$ will go to the same state as Standard mode. In both modes, all data outputs will go low. Previous programmed configurations will not be maintained.
143	Partial Reset	$\overline{PRST}$	Input	Partial Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{PRST}$ low. In Standard mode, $\overline{FULL}$ and $\overline{PRAF}$ will go high; $\overline{EMPTY}$ and $\overline{PRAE}$ will go low. In FWFT mode, $\overline{DRDY}$ will go low and $\overline{QRDY}$ will go high. $\overline{PRAF}$ and $\overline{PRAE}$ will go to the same state as Standard mode. In both modes, all data outputs will go low. Previous programmed configurations will be maintained.
144	Write Clock	WCLK	Input	Writes data into queue during low to high transitions of WCLK if $\overline{WEN}$ is set to low.
1	Write Enable	$\overline{WEN}$	Input	Controls write operation into queue or offset registers during low to high transition of WCLK.
141	Load Enable	$\overline{LOAD}$	Input	During Master Reset, set $\overline{LOAD}$ low to select parallel programming or one of eight default offset values. Set $\overline{LOAD}$ high to select serial programming or one of eight default offset values. After Master Reset, $\overline{LOAD}$ controls write/read, to/from offset registers during low to high transition of WCLK/RCLK respectively. Use in conjunction with $\overline{WEN}$ / $\overline{REN}$.
127	Default Programming 1	PFS1	Input	During Master Reset, select one of eight default offset values. Use in conjunction with $\overline{LOAD}$ and PFS0.
130	Default Programming 0	PFS0	Input	During Master Reset, select one of eight default offset values. Use in conjunction with $\overline{LOAD}$ and PFS1.
47,48,51,52,53	Ch 0	D_{4-0}	Input	40 - bit wide input data bus.
40,41,42,43,46	Ch 1	D_{9-5}		
34,36,37,38,39	Ch 2	D_{14-10}		
29,30,31,32,33	Ch 3	D_{19-15}		
23,25,26,27,28	Ch 4	D_{24-20}		
17,18,19,20,21	Ch 5	D_{29-25}		
12,13,14,15,16	Ch 6	D_{34-30}		
06,07,08,09,10	Ch 7	D_{39-35}		
112	Read Clock	RCLK	Input	Reads data from queue during low to high transitions of RCLK if $\overline{REN}$ is set to low.

Table 1. Pin Descriptions

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Pin #	Pin Name	Pin Symbol	Input/Output	Description
111	Read Enable	$\overline{REN}$	Input	Controls read operation from queue or offset registers during low to high transition of RCLK.
109	Output Enable	$\overline{OE}$	Input	Setting $\overline{OE}$ low activates the data output drivers. Setting $\overline{OE}$ high deactivates the data output drivers (High-Z).
62,59,58,56,55	Ch 0	Q_{4-0}	Output	40 - bit wide output data bus.
70,69,68,65,63	Ch 1	Q_{9-5}		
75,74,73,72,71	Ch 2	Q_{14-10}		
81,80,79,77,76	Ch 3	Q_{19-15}		
88,87,85,84,83	Ch 4	Q_{24-20}		
95,94,92,91,89	Ch 5	Q_{29-25}		
101,100,98,97,96	Ch 6	Q_{34-30}		
108,107,105,104,103	Ch 7	Q_{39-35}		
140	First Word Fall Through/Serial Data Input	FWFT/SDI	Input	Selects FWFT timing or Standard timing mode during Master Reset. After Master Reset, if serial programming is selected ($\overline{LOAD}$ = high), FWFT/SDI is used as the serial data input for the offset registers. Serial data is written during the low to high transition of WCLK. Use in conjunction with $\overline{SDEN}$.
2	Serial Data Input Enable	$\overline{SDEN}$	Input	If serial programming is selected, setting $\overline{SDEN}$ low and $\overline{LOAD}$ low enables serial data input to be written into offset registers during the low to high transition of WCLK.
5	Switching Control Register Write Enable	$\overline{AWEN}$	Input	Setting $\overline{AWEN}$ low causes the value on the input data bus to be written into the switching control register during the low to high transition of WCLK, provided $\overline{WEN}$ is held high at the same transition.
131	Switching Control Register Read Enable	$\overline{AREN}$	Input	Setting $\overline{AREN}$ low allows reading from the switching control register during the low to high transition of RCLK, provided $\overline{REN}$ is held high at the same transition.
110	Retransmit	$\overline{RET}$	Input	Data previously read from the queue can be retransmitted by asserting $\overline{RET}$ pin at the low to high transition of RCLK for a retransmit operation. Retransmit initializes the Read pointer to zero. Hence, all re-reads will always start from the physical 0^{th} (Read pointer = zero) location of the queue.
115	Zero Latency Retransmit	$\overline{RETZL}$	Input	During Master Reset, set $\overline{RETZL}$ low to select zero latency retransmit or $\overline{RETZL}$ high to select normal latency retransmit.

Table 1. Pin Descriptions (Continued)

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Pin #	Pin Name	Pin Symbol	Input/Output	Description
137	Full/Data Input Ready Flag	$\overline{FULL}$ / $\overline{DRDY}$	Output	Queue is full when $\overline{FULL}$ goes low during the low to high transition of WCLK. This prohibits further writes into the queue. In FWFT mode, queue is full when $\overline{DRDY}$ goes high during low to high transition of WCLK. This prohibits further writes into the queue.
116	Empty/Data Output Ready Flag	$\overline{EMPTY}$ / $\overline{QRDY}$	Output	Queue is empty when $\overline{EMPTY}$ goes low during the low to high transition of RCLK. This prohibits further reads from the queue. In FWFT mode, queue is empty when $\overline{QRDY}$ goes high during the low to high transition of RCLK. This prohibits further reads from the queue.
124	Interspersed Parity	IPAR	Input	During Master Reset, set IPAR low to select 9-bit parallel programming mode or IPAR high to select 8-bit parallel programming mode.
117	Synchronous Partial Flag Mode	SFM	Input	During Master Reset, set SFM high to select Synchronous Partial Flag mode or SFM low to select Asynchronous Partial Flag mode.
134	Almost Full	$\overline{PRAF}$	Output	Queue is almost full when $\overline{PRAF}$ goes low during the low to high transition of WCLK. Default (Full-offset) or programmed offset values determine the status of $\overline{PRAF}$.
119	Almost Empty	$\overline{PRAE}$	Output	Queue is almost empty when $\overline{PRAE}$ goes low during the low to high transition of RCLK. Default (Empty +offset) or programmed offset values determine the status of $\overline{PRAE}$.
129	Half Full	$\overline{HALF}$	Output	Queue is more than half full when $\overline{HALF}$ goes low. Triggered by both WCLK and RCLK.
04,11,24,35,49, 50,60,61,66,67, 78,86,93,99,106, 121,123,135,136.	Power	Vcc	N/A	3.3V power supply.
03,22,44,45,54, 57,64,82,90,102, 113,114,118,120, 122,125,126,128, 132,133,138,139	Ground	GND	N/A	0V Ground.

Table 1. Pin Descriptions (Continued)

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Symbol	Rating	Com'l & Ind'l	Unit
VTERM	Terminal Voltage with respect to GND	-0.5 to + 4.5	V
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	-50 to +50	mA

NOTES:
Absolute Max Ratings are for reference only. Permanent damage to the device may occur if extended period of operation is outside this range. Standard operation should fall within the Recommended Operating Conditions.

Table 2. Absolute Maximum Ratings

		CQV8110, CQV8100, CQV890, CQV880, CQV870, CQV860, CQV850, CQV840						
		Commercial Clock = 6ns, 7.5ns, 10ns			Industrial Clock = 7.5ns, 10ns, 15ns			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
Recommended Operating Conditions								
Vcc	Supply Voltage Com'l / Ind'l	3.15	3.3	3.45	3.15	3.3	3.45	V
GND	Supply Voltage	0	0	0	0	0	0	V
VIH	Input High Voltage Com'l / Ind'l	2.0	-	5.5	2.0	-	5.5	V
VIL	Input Low Voltage Com'l / Ind'l	-	-	0.8	-	-	0.8	V
TA	Operating Temperature Commercial	0	-	70	0	-	70	°C
TA	Operating Temperature Industrial	-40	-	85	-40	-	85	°C
DC Electrical Characteristics								
ILI(1)	Input Leakage Current (any input)	-10	-	10	-10	-	10	µA
ILO	Output Leakage Current	-10	-	10	-10	-	10	µA
VOH	Output Logic "1" Voltage, IOH=-2mA	2.4	-	-	2.4	-	-	V
VOL	Output Logic "0" Voltage, IOL = 8mA	-	-	0.4	-	-	0.4	V
Power Consumption								
Icc1(2,3)	Active Power Supply Current	-	-	40	-	-	40	mA
Icc2(4)	Standby Current	-	-	15	-	-	15	mA

Capacitance at 100MHz Ambient Temperature (25°C)				
Symbol	**Parameter**	**Conditions**	**Max.**	**Unit**
CIN(2)	Input Capacitance	VIN= 0V	10	pF
COUT(2,4)	Output Capacitance	VOUT= 0V	10	pF

NOTES:
1. Measurement with 0.4<=VIN<=Vcc
2. With output tri-stated ($\overline{OE}$ = High)
3. Icc(1,2) is measured with WCLK and RCLK at 20 MHz
4. Design simulated, not tested.

Table 3. DC Specifications

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Symbol	Parameter	Commercial		Commercial & Industrial				Unit
		CQV8110-6 CQV8100-6 CQV890-6 CQV880-6 CQV870-6 CQV860-6 CQV850-6 CQV840-6		CQV8110-7.5 CQV8100-7.5 CQV890-7.5 CQV880-7.5 CQV870-7.5 CQV860-7.5 CQV850-7.5 CQV840-7.5		CQV8110-10 CQV8100-10 CQV890-10 CQV880-10 CQV870-10 CQV860-10 CQV850-10 CQV840-10		
		Min.	Max.	Min.	Max.	Min.	Max.	
f_S	Clock Cycle Frequency	-	166	-	133	-	100	MHz
t_A	Data Access Time	1	4	2	5	2	6.5	ns
t_{WCLK}	Write Clock Cycle Time	6	-	7.5	-	10	-	ns
t_{WCLKH}	Write Clock High Time	2.5	-	3.5	-	4.5	-	ns
t_{WCLKL}	Write Clock Low Time	2.5	-	3.5	-	4.5	-	ns
t_{RCLK}	Read Clock Cycle Time	6	-	7.5	-	10	-	ns
t_{RCLKH}	Read Clock High Time	2.5	-	3.5	-	4.5	-	ns
t_{RCLKL}	Read Clock Low Time	2.5	-	3.5	-	4.5	-	ns
t_{DS}	Data Set-up Time	2.0	-	2.5	-	3.5	-	ns
t_{DH}	Data Hold Time	0.5	-	0.5	-	0.5	-	ns
t_{ENS}	Enable Set-up Time	2.0	-	2.5	-	3.5	-	ns
t_{ENH}	Enable Hold Time	0.5	-	0.5	-	0.5	-	ns
t_{RST}	Reset Pulse Width[1]	8	-	10	-	10	-	ns
t_{RSTS}	Reset Set-up Time	10	-	15		15	-	ns
t_{RSTR}	Reset Recovery Time	10	-	10	-	10	-	ns
t_{RSTF}	Reset to Flag and Output Time	-	10	-	15	-	15	ns
t_{OLZ}	Output Enable to Output in Low-Z[1]	0	-	0	-	0	-	ns
t_{OE}	Output Enable to Output Valid	2	4	2	5	2	6	ns
t_{OHZ}	Output Enable to Output in High-Z[1]	2	4	2	6	2	6	ns
t_{FULL}	Write Clock to Full Flag	-	4	-	5	-	6.5	ns
t_{EMPTY}	Read Clock to Empty Flag	-	4	-	5	-	6.5	ns
t_{PRAFS}	Write Clock to Synchronous Almost-Full Flag	-	4	-	5	-	6.5	ns
t_{PRAES}	Read Clock to Synchronous Almost-Empty Flag	-	4	-	5	-	6.5	ns
t_{SKEW1}	Skew time between Read Clock & Write Clock for Full Flag / Empty Flag	4	-	5	-	7	-	ns
t_{SKEW2}	Skew time between Read Clock & Write Clock for $\overline{PRAE}$ & $\overline{PRAF}$	6	-	7	-	10	-	ns
t_{LOADS}	Load Setup Time	2.0	-	2.5	-	3.5	-	ns
t_{LOADH}	Load Hold Time	0.5	-	0.5	-	0.5	-	ns

Table 4. AC Electrical Characteristics

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		Commercial		Commercial & Industrial				
		CQV8110-6 CQV8100-6 CQV890-6 CQV880-6 CQV870-6 CQV860-6 CQV850-6 CQV840-6		FQV8110-7.5 FQV8100-7.5 FQV890-7.5 FQV880-7.5 FQV870-7.5 FQV860-7.5 FQV850-7.5 FQV840-7.5		FQV8110-10 FQV8100-10 FQV890-10 FQV880-10 FQV870-10 FQV860-10 FQV850-10 FQV840-10		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
t_{RETS}	Retransmit Setup Time	2.5	-	3.5	-	3.5	-	ns
t_{HALF}	Clock to $\overline{HALF}$	-	12	-	12.5	-	16	ns
t_{PRAFA}	Write Clock to Asynchronous Programmable Almost-Full Flag	-	12	-	12.5	-	16	ns
t_{PRAEA}	Read Clock to Asynchronous Programmable Almost-Empty Flag	-	12	-	12.5	-	16	ns

NOTES:

1. Design simulated, not tested.

Table 4. AC Electrical Characteristics (Continued)

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Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load, clock = 6ns, 7.5ns, 10ns	Refer to Figure 8

Table 5. AC Test Condition

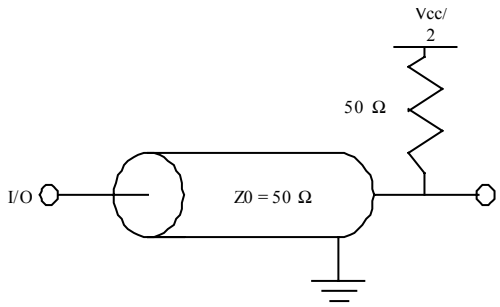

Figure 8. AC Test Load
for clock = 6ns, 7.5ns

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Pin Functions

$\overline{\text{MRST}}$ Master Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{\text{MRST}}$ low. In Standard mode, $\overline{\text{FULL}}$ and $\overline{\text{PRAF}}$ will go high; $\overline{\text{EMPTY}}$ and $\overline{\text{PRAE}}$ will go low. In FWFT mode, $\overline{\text{DRDY}}$ will go low and $\overline{\text{QRDY}}$ will go high. $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ will go to the same state as Standard mode. In both modes, all data outputs will go low. Previous programmed configurations will not be maintained.

$\overline{\text{PRST}}$ Partial Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{\text{PRST}}$ low. In Standard mode, $\overline{\text{FULL}}$ and $\overline{\text{PRAF}}$ will go high; $\overline{\text{EMPTY}}$ and $\overline{\text{PRAE}}$ will go low. In FWFT mode, $\overline{\text{DRDY}}$ will go low and $\overline{\text{QRDY}}$ will go high. $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ will go to the same state as Standard mode. In both modes, all data outputs will go low. Previous programmed configurations will be maintained.

WCLK Writes data into queue during low to high transitions of WCLK if $\overline{\text{WEN}}$ is activated. Synchronizes $\overline{\text{FULL}}$ / $\overline{\text{DRDY}}$ and $\overline{\text{PRAF}}$ flags. WCLK and RCLK are independent of each other.

$\overline{\text{WEN}}$ Controls write operation into queue or offset registers during low to high transition of WCLK.

$\overline{\text{LOAD}}$ During Master Reset, set $\overline{\text{LOAD}}$ low to select parallel programming or one of eight default offset values. Set $\overline{\text{LOAD}}$ high to select serial programming or one of eight default offset values. After Master Reset, $\overline{\text{LOAD}}$ controls write/read, to/from offset registers during low to high transition of WCLK/RCLK respectively for parallel programming. Use in conjunction with $\overline{\text{WEN}}$ / $\overline{\text{REN}}$. During programming of offset registers, $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ flag status is invalid. For Serial programming, $\overline{\text{LOAD}}$ is used to enable serial loading of offset registers together with $\overline{\text{SDEN}}$. Refer to Figure 9 & Table 12 for details.

PFS1 During Master Reset, select one of eight default offset values. Use in conjunction with $\overline{\text{LOAD}}$ and PFS1. Refer to Table 12 for details.

PFS0 During Master Reset, select one of eight default offset values. Use in conjunction with $\overline{\text{LOAD}}$ and PFS0. Refer to Table 12 for details.

$D_{39\text{-}0}$ 40 - bit wide input data bus.

RCLK Reads data from queue during low to high transitions of RCLK if $\overline{\text{REN}}$ is set low. Synchronizes the $\overline{\text{EMPTY}}$ / $\overline{\text{QRDY}}$ and $\overline{\text{PRAE}}$ flags. RCLK and WCLK are independent of each other.

$\overline{\text{REN}}$ Reads data from queue during low to high transitions of RCLK if $\overline{\text{REN}}$ is set to low. This also advances the Read pointer of the queue.

$\overline{\text{OE}}$ Setting $\overline{\text{OE}}$ low activates the data output drivers. Setting $\overline{\text{OE}}$ high deactivates the data output drivers (High-Z). $\overline{\text{OE}}$ does not control advancement of Read pointer.

$Q_{39\text{-}0}$ 40 - bit wide output data bus.

FWFT/SDI Selects FWFT timing or Standard timing mode during Master Reset. After Master Reset, if serial programming is selected ($\overline{\text{LOAD}}$ = high), FWFT/SDI is used as the serial data input for the offset registers. Serial data is written during the low to high transition of WCLK. Use in conjunction with $\overline{\text{SDEN}}$. In FWFT mode, $\overline{\text{DRDY}}$ and $\overline{\text{QRDY}}$ is used instead of $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$. Refer to Table 10 for all flags status. In Standard mode, $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ are used instead of $\overline{\text{DRDY}}$ and $\overline{\text{QRDY}}$. Refer to Table 9 for all flags status.

$\overline{\text{SDEN}}$ If serial programming is selected, setting $\overline{\text{SDEN}}$ and $\overline{\text{LOAD}}$ low enables serial data to be written into offset registers during the low to high transition of WCLK. During serial programming, $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ flags status is invalid. Refer to Figure 9 for details.

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Pin Functions (Continued)

$\overline{\text{RET}}$ Data previously read from the queue can be retransmitted by asserting $\overline{\text{RET}}$ pin at the low to high transition of RCLK for a retransmit operation. Retransmit initializes the Read pointer to zero. Hence, all re-reads will always start from the physical 0^{th} (Read pointer = zero), location of the queue. Refer to Diagram 7 & 8 for details.

$\overline{\text{RETZL}}$ During Master Reset, set $\overline{\text{RETZL}}$ low to select zero latency retransmit or set $\overline{\text{RETZL}}$ high to select normal latency retransmit.

$\overline{\text{FULL}}$ / $\overline{\text{DRDY}}$ In Standard mode, queue is full when $\overline{\text{FULL}}$ goes low during the low to high transition of WCLK. This prohibits further writes into the queue and prevents advancement of Write pointer. In FWFT mode, queue is full when $\overline{\text{DRDY}}$ goes high during the low to high transition of WCLK. This prohibits further writes into the queue and prevents advancement of Write pointer. Refer to Table 9 & 10 for behavior of $\overline{\text{FULL}}$ / $\overline{\text{DRDY}}$.

$\overline{\text{EMPTY}}$ / $\overline{\text{QRDY}}$ In Standard mode, queue is empty when $\overline{\text{EMPTY}}$ goes low during the low to high transition of RCLK. This prohibits further reads from the queue and prevents advancement of Read pointer. In FWFT mode, queue is empty when $\overline{\text{QRDY}}$ goes low during the low to high transition of RCLK. This prohibits further reads from the queue and prevents advancement of Read pointer. Refer to Table 9 & 10 for behavior of $\overline{\text{EMPTY}}$ / $\overline{\text{QRDY}}$.

IPAR During Master Reset, set IPAR low to select 10-bit parallel programming mode or set IPAR high to select 8-bit parallel programming mode. In 10-bit mode, 10-bit wide data input/output bus width is used for storing/fetching offset values. In 8-bit mode, 8-bit wide data input/output bus is used for storing/fetching offset values.

SFM During Master Reset, set SFM high to select Synchronous Partial Flag mode or set SFM low to select Asynchronous Partial Flag mode. In Synchronous mode, $\overline{\text{PRAF}}$ and $\overline{\text{PRAE}}$ are synchronous to WCLK and RCLK respectively. In Asynchronous mode, WCLK synchronizes the assertion of $\overline{\text{PRAF}}$ and de-assertion of $\overline{\text{PRAE}}$. RCLK synchronizes the assertion of $\overline{\text{PRAE}}$ and de-assertion of $\overline{\text{PRAF}}$.

$\overline{\text{PRAF}}$ In Synchronous mode, queue is almost full when $\overline{\text{PRAF}}$ goes low during the low to high transition of WCLK. Default (Full-offset) or programmed offset values determine the status of $\overline{\text{PRAF}}$. In Asynchronous mode, $\overline{\text{PRAF}}$ is triggered by both WCLK and RCLK. Refer to Table 9 & 10 for behavior of $\overline{\text{PRAF}}$.

$\overline{\text{PRAE}}$ In Synchronous mode, queue is almost empty when $\overline{\text{PRAE}}$ goes low during the low to high transition of RCLK. Default (Empty+offset) or programmed offset values determine the status of $\overline{\text{PRAE}}$. In Asynchronous timing mode, $\overline{\text{PRAE}}$ is triggered by both WCLK and RCLK. Refer to Table 9 & 10 for behavior of $\overline{\text{PRAE}}$.

$\overline{\text{HALF}}$ Queue is more than half full when $\overline{\text{HALF}}$ goes low during the low to high transition of WCLK. $\overline{\text{HALF}}$ goes high during low to high transition of RCLK when queue is less than half full. Refer to Table 9 & 10 for details.

$\overline{\text{AWEN}}$ Setting $\overline{\text{AWEN}}$ low causes the value on the input data bus to be written into the switching control register during the low to high transition of WCLK, provided $\overline{\text{WEN}}$ is held high at the same transition.

$\overline{\text{AREN}}$ Setting $\overline{\text{AREN}}$ low allows reading from the switching control register during the low to high transition of RCLK, provided $\overline{\text{REN}}$ is held high at the same transition.

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$\overline{LOAD}$	$\overline{WEN}$	$\overline{REN}$	$\overline{AWEN}$	$\overline{AREN}$	$\overline{SDEN}$	WCLK	RCLK	SCLK	CQV8110 CQV8100 CQV890 CQV880 CQV870 CQV860 CQV850 CQV840 Selection / Sequence
0	0	1	1	1	1	↑	X	X	Parallel write to offset registers: Empty Offset Full Offset Parallel write to registers: 1. $\overline{PRAE}$ 2. $\overline{PRAF}$
0	1	0	1	1	1	X	↑	X	Parallel read from offset registers: Empty Offset Full Offset Parallel read from registers: 1. $\overline{PRAE}$ 2. $\overline{PRAF}$
0	1	1	1	1	0	X	X	↑	Serial shift into registers: 34 bits for the CQV8110 32 bits for the CQV81000 30 bits for the CQV890 28 bits for the CQV880 26 bits for the CQV870 24 bits for the CQV860 22 bits for the CQV850 20 bits for the CQV840 1 bit for each rising WCLK edge Starting with Empty Offset (Low Byte) Ending with Full Offset (High Byte)
X	1	1	1	1	1	X	X	X	No Operation
X	1	X	0	X	X	↑	X	X	Write Switching Control Register
X	X	1	X	0	X	X	↑	X	Read Switching Control Register
1	0	X	X	X	X	↑	X	X	Write Memory
1	X	0	X	X	X	X	↑	X	Read Memory
1	1	1	1	1	X	X	X	X	No Operation

Figure 9. Programmable Flag Offset Programming Sequence

(CQV8110, CQV8100, CQV890, CQV880, CQV870, CQV860, CQV850 and CQV840)

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Device	$\overline{\text{PRAF}}$ Programming (bits)		$\overline{\text{PRAE}}$ Programming (bits)	
CQV8110	D/Q_{16-0}	Non-IPAR	D/Q_{16-0}	Non-IPAR
	D/Q_{20} & D/Q_{17-10} & D/Q_{7-0}	IPAR	D/Q_{20} & D/Q_{17-10} & D/Q_{7-0}	IPAR
CQV8100	D/Q_{15-0}	Non-IPAR	D/Q_{15-0}	Non-IPAR
	D/Q_{17-10} & D/Q_{7-0}	IPAR	D/Q_{17-10} & D/Q_{7-0}	IPAR
CQV890	D/Q_{14-0}	Non-IPAR	D/Q_{14-0}	Non-IPAR
	D/Q_{16-10} & D/Q_{7-0}	IPAR	D/Q_{16-10} & D/Q_{7-0}	IPAR
CQV880	D/Q_{13-0}	Non-IPAR	D/Q_{13-0}	Non-IPAR
	D/Q_{15-10} & D/Q_{7-0}	IPAR	D/Q_{15-10} & D/Q_{7-0}	IPAR
CQV870	D/Q_{12-0}	Non-IPAR	D/Q_{12-0}	Non-IPAR
	D/Q_{14-10} & D/Q_{7-0}	IPAR	D/Q_{14-10} & D/Q_{7-0}	IPAR
CQV860	D/Q_{11-0}	Non-IPAR	D/Q_{11-0}	Non-IPAR
	D/Q_{13-10} & D/Q_{7-0}	IPAR	D/Q_{13-10} & D/Q_{7-0}	IPAR
CQV850	D/Q_{10-0}	Non-IPAR	D/Q_{10-0}	Non-IPAR
	D/Q_{12-10} & D/Q_{7-0}	IPAR	D/Q_{12-10} & D/Q_{7-0}	IPAR
CQV840	D/Q_{9-0}	Non-IPAR	D/Q_{9-0}	Non-IPAR
	D/Q_{11-10} & D/Q_{7-0}	IPAR	D/Q_{11-10} & D/Q_{7-0}	IPAR

Table 6. Parallel Offset Register Data Mapping Table

Device	Standard Mode	FWFT Mode
CQV8110	131,072 x 40	131,073 x 40
CQV8100	65,536 x 40	65,537 x 40
CQV890	32,768 x 40	32,769 x 40
CQV880	16,384 x 40	16,385 x 40
CQV870	8,192 x 40	8,193 x 40
CQV860	4,096 x 40	4,097 x 40
CQV850	2,048 x 40	2,049 x 40
CQV840	1,024 x 40	1,025 x 40

Table 7. Maximum Depth of Queue for Standard and FWFT Mode

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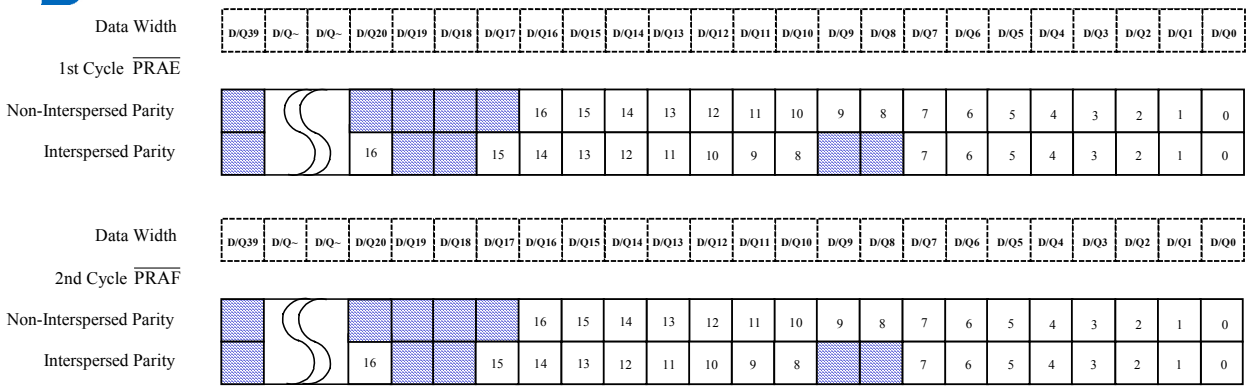

CQV8110, CQV8100, CQV890, CQV880, CQV870, CQV860, CQV850, CQV840
Parallel Offset Write/Read Cycles

# of Bits for Offset Registers
17 bits for CQV8110
16 bits for CQV8100
15 bits for CQV890
14 bits for CQV880
13 bits for CQV870
12 bits for CQV860
11 bits for CQV850
10 bits for CQV840
Note: Don't Care applies to all unused bits

Figure 10. Parallel Offset Write/Read Cycle Diagram

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CQV8110	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y(1)	H	H	H	L	H
(y+1) to 65,536	H	H	H	H	H
65,537 to [131,072-(x+1)]	H	H	L	H	H
(131,072-x) to 131,071	H	L	L	H	H
131,072	L	L	L	H	H

CQV8100	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y(1)	H	H	H	L	H
(y+1) to 32,768	H	H	H	H	H
32,769 to [65,536-(x+1)]	H	H	L	H	H
(65,536-x) to 65,535	H	L	L	H	H
65,536	L	L	L	H	H

CQV890	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y(1)	H	H	H	L	H
(y+1) to 16,384	H	H	H	H	H
16,385 to [32,768-(x+1)]	H	H	L	H	H
(32,768-x) to 32,767	H	L	L	H	H
32,768	L	L	L	H	H

CQV880	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y(1)	H	H	H	L	H
(y+1) to 8,192	H	H	H	H	H
8,193 to [16,384-(x+1)]	H	H	L	H	H
(16,384 -x) to 16,383	H	L	L	H	H
16,384	L	L	L	H	H

CQV870	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y(1)	H	H	H	L	H
(y+1) to 4,096	H	H	H	H	H
4,097 to [8,192-(x+1)]	H	H	L	H	H
(8,192 -x) to 8,191	H	L	L	H	H
8,192	L	L	L	H	H

CQV860	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y(1)	H	H	H	L	H
(y+1) to 2,048	H	H	H	H	H
2,049 to [4,096-(x+1)]	H	H	L	H	H
(4,096 –x) to 4,095	H	L	L	H	H
4,096	L	L	L	H	H

Table 8. Status Flags (Standard Mode)

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CQV850	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y(1)	H	H	H	L	H
(y+1) to 1,024	H	H	H	H	H
1,025 to [2,048-(x+1)]	H	H	L	H	H
(2,048 -x) to 2,047	H	L	L	H	H
2,048	L	L	L	H	H

CQV840	$\overline{\text{FULL}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{EMPTY}}$
0	H	H	H	L	L
1 to y(1)	H	H	H	L	H
(y+1) to 512	H	H	H	H	H
513 to [1,024-(x+1)]	H	H	L	H	H
(1,024 –x) to 1,023	H	L	L	H	H
1,024	L	L	L	H	H

NOTES:
1. See Table 12 for values x, y.

Table 8. Status Flags (Standard Mode) (Continued)

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CQV8110	$\overline{\text{DRDY}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{QRDY}}$
0	L	H	H	L	H
1 to y+1[1]	L	H	H	L	L
(y+2) to 65,537	L	H	H	H	L
65,538 to [131,073-(x+1)]	L	H	L	H	L
(131,073-x) to 131,072	L	L	L	H	L
131,073	H	L	L	H	L

CQV8100	$\overline{\text{DRDY}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{QRDY}}$
0	L	H	H	L	H
1 to y+1[1]	L	H	H	L	L
(y+2) to 32,769	L	H	H	H	L
32,770 to [65,537-(x+1)]	L	H	L	H	L
(65,537-x) to 65,536	L	L	L	H	L
65,537	H	L	L	H	L

CQV890	$\overline{\text{DRDY}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{QRDY}}$
0	L	H	H	L	H
1 to y+1[1]	L	H	H	L	L
(y+2) to 16,385	L	H	H	H	L
16,386 to [32,769-(x+1)]	L	H	L	H	L
(32,769-x) to 32,768	L	L	L	H	L
32,769	H	L	L	H	L

CQV880	$\overline{\text{DRDY}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{QRDY}}$
0	L	H	H	L	H
1 to y+1[1]	L	H	H	L	L
(y+2) to 8,193	L	H	H	H	L
8,194 to [16,385-(x+1)]	L	H	L	H	L
(16,385 -x) to 16,384	L	L	L	H	L
16,385	H	L	L	H	L

CQV870	$\overline{\text{DRDY}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{QRDY}}$
0	L	H	H	L	H
1 to y+1[1]	L	H	H	L	L
(y+2) to 4,097	L	H	H	H	L
4,098 to [8,193-(x+1)]	L	H	L	H	L
(8,193-x) to 8,192	L	L	L	H	L
8,193	H	L	L	H	L

CQV860	$\overline{\text{DRDY}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{QRDY}}$
0	L	H	H	L	H
1 to y+1[1]	L	H	H	L	L
(y+2) to 2,049	L	H	H	H	L
2,050 to [4,097-(x+1)]	L	H	L	H	L
(4,097 -x) to 4,096	L	L	L	H	L
4,097	H	L	L	H	L

Table 9. Status Flags (FWFT Mode)

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CQV850	$\overline{\text{DRDY}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{QRDY}}$
0	L	H	H	L	H
1 to y+1[1]	L	H	H	L	L
(y+2) to 1,025	L	H	H	H	L
1,026 to [2,049-(x+1)]	L	H	L	H	L
(2,049 -x) to 2,048	L	L	L	H	L
2,049	H	L	L	H	L

CQV840	$\overline{\text{DRDY}}$	$\overline{\text{PRAF}}$	$\overline{\text{HALF}}$	$\overline{\text{PRAE}}$	$\overline{\text{QRDY}}$
0	L	H	H	L	H
1 to y+1[1]	L	H	H	L	L
(y+2) to 513	L	H	H	H	L
514 to [1,025-(x+1)]	L	H	L	H	L
(1,025 -x) to 1,024	L	L	L	H	L
1,025	H	L	L	H	L

NOTES:
1. See Table 12 for values x, y.

Table 9. Status Flags (FWFT Mode) (Continued)

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$\overline{LOAD}$	PFS1	PFS0	CQV850 CQV840 Default Offsets x, y(1)
0	0	0	127
0	0	1	255
0	1	0	511
0	1	1	63
1	0	0	31
1	0	1	7
1	1	0	15
1	1	1	3

$\overline{LOAD}$	PFS1	PFS0	CQV850 CQV840 Program Mode
1	X	X	Serial
0	X	X	Parallel

$\overline{LOAD}$	PFS1	PFS0	CQV890 CQV880 CQV870 CQV860 Default Offsets x, y(1)
0	0	0	127
0	0	1	255
0	1	0	511
0	1	1	63
1	0	0	1,023
1	0	1	15
1	1	0	31
1	1	1	7

$\overline{LOAD}$	PFS1	PFS0	CQV890 CQV880 CQV870 CQV860 Program Mode
1	X	X	Serial
0	X	X	Parallel

NOTES:
1. x = $\overline{PRAF}$ offset, y = $\overline{PRAE}$ offset.

Table 10. Default Programmable Flag Offsets

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$\overline{\text{LOAD}}$	PFS1	PFS0	CQV8110 CQV8100 Default Offsets x, y[1]
0	0	0	127
0	0	1	8,191
0	1	0	16,383
0	1	1	4,095
1	0	0	1,023
1	0	1	511
1	1	0	2,047
1	1	1	255

$\overline{\text{LOAD}}$	PFS1	PFS0	CQV8110 CQV8100 Program Mode
1	X	X	Serial
0	X	X	Parallel

NOTES:
1. x = $\overline{\text{PRAF}}$ offset, y = $\overline{\text{PRAE}}$ offset.

Table 10. Default Programmable Flag Offsets (Continued)

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Timing Diagrams

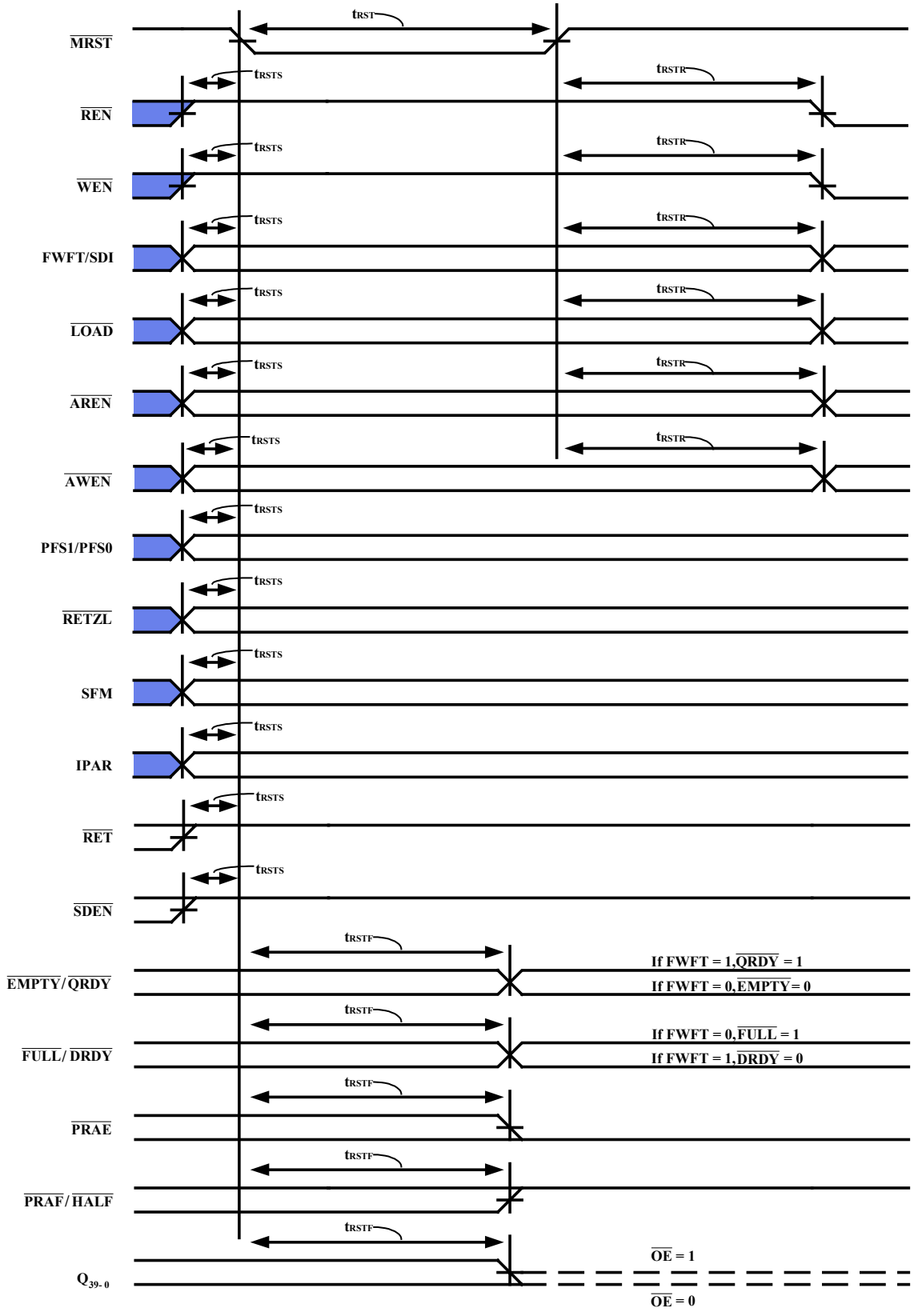

Diagram 1. Master Reset Timing

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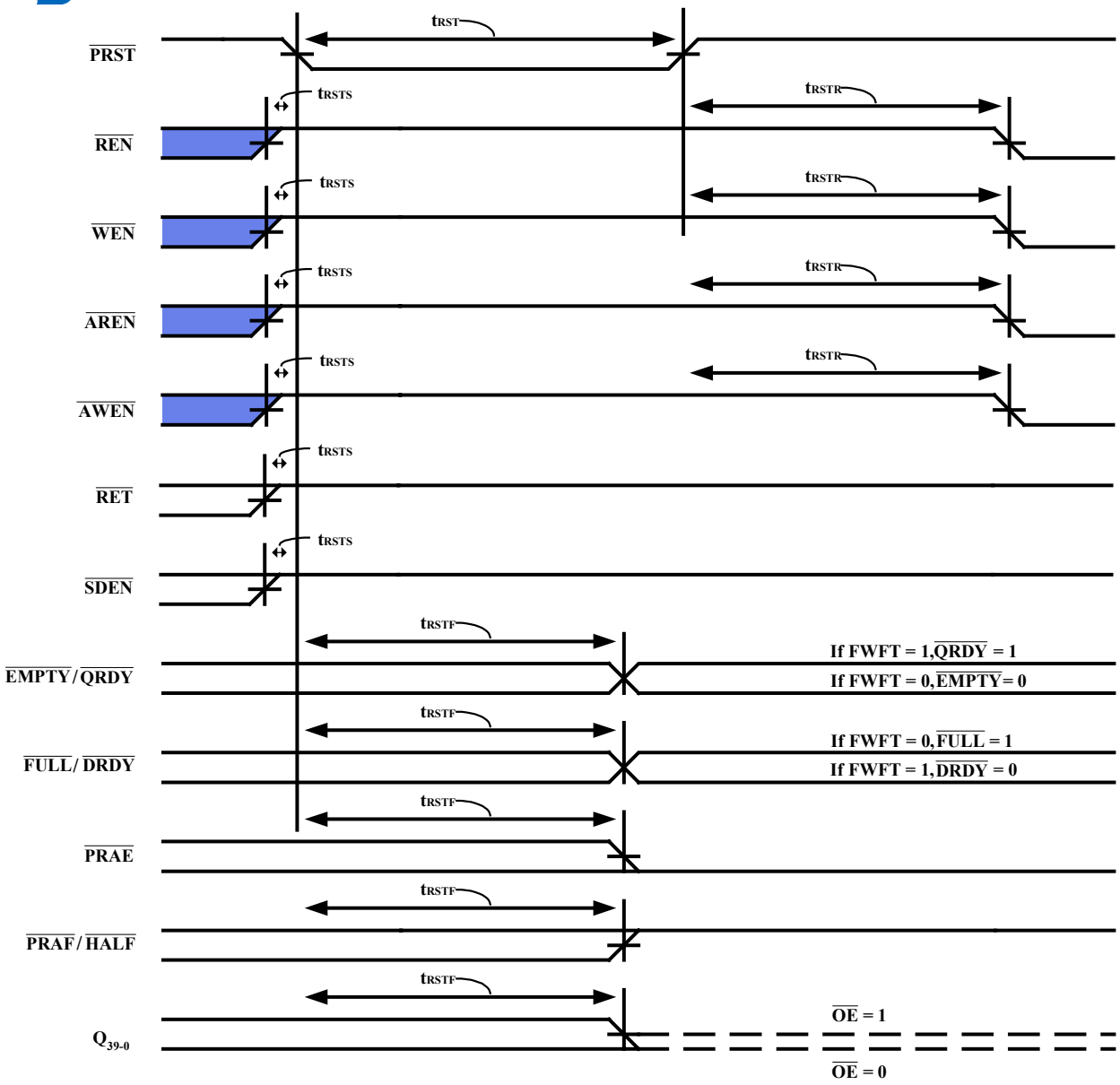

Diagram 2. Partial Reset Timing

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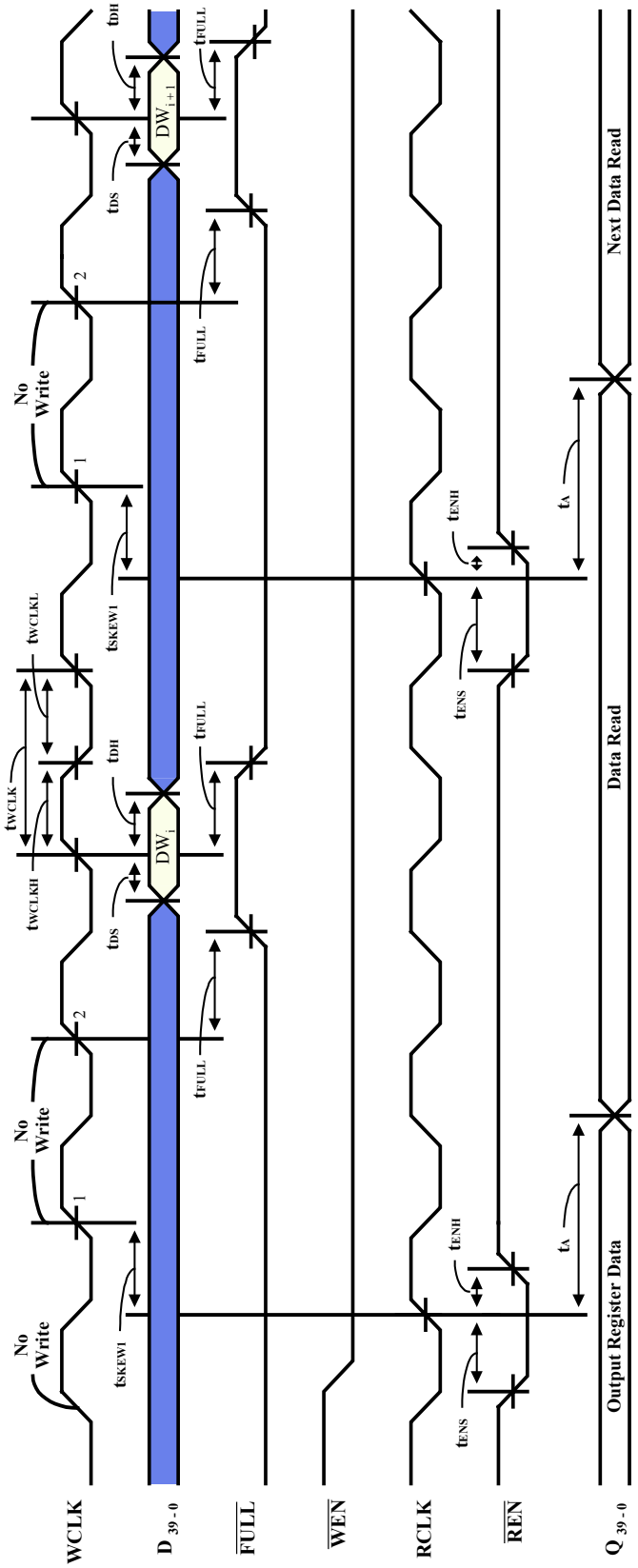

Diagram 3. Write Cycle and Full Flag Timing (Standard Mode)

NOTES:

1. If the time between a rising edge of RCLK to the rising edge of WCLK is greater than or equal to t_{SKEW1}, $\overline{FULL}$ will go high (after one WCLK cycle plus t_{FULL}). If t_{SKEW1} is not met, then $\overline{FULL}$ will assert 1 or more WCLK cycles.
2. $\overline{LOAD}$ = High, $\overline{OE}$ = Low.

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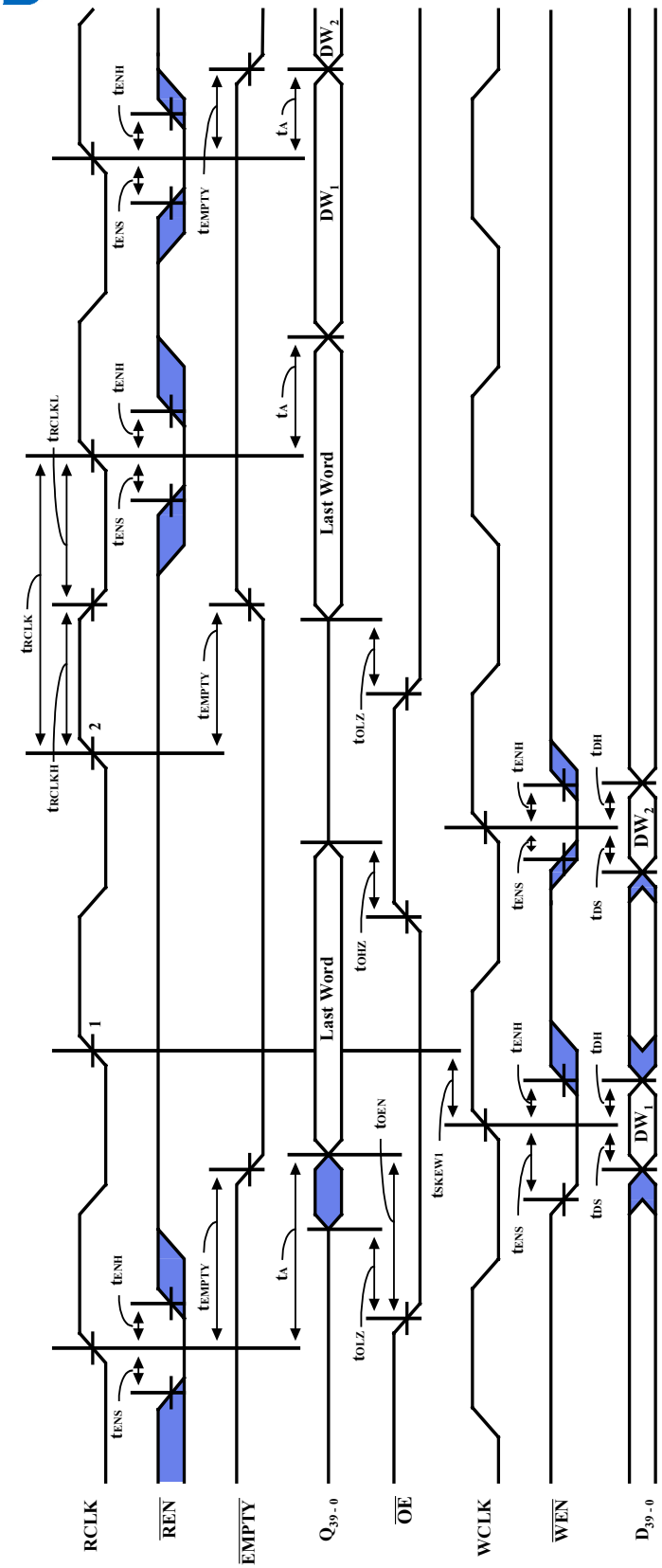

Diagram 4. Read Cycle, Empty Flag and First Data Word Latency Timing (Standard Mode)

NOTES:

1. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to t_{SKEW1}, $\overline{EMPTY}$ will go high (after RCLK cycle plus t_{EMPTY}). If t_{SKEW1} is not met, then $\overline{EMPTY}$ will assert 1 or more RCLK cycles.
2. LOAD = High.
3. First word latency: $t_{SKEW1} + t_{EMPTY} + 1 * t_{RCLK}$.

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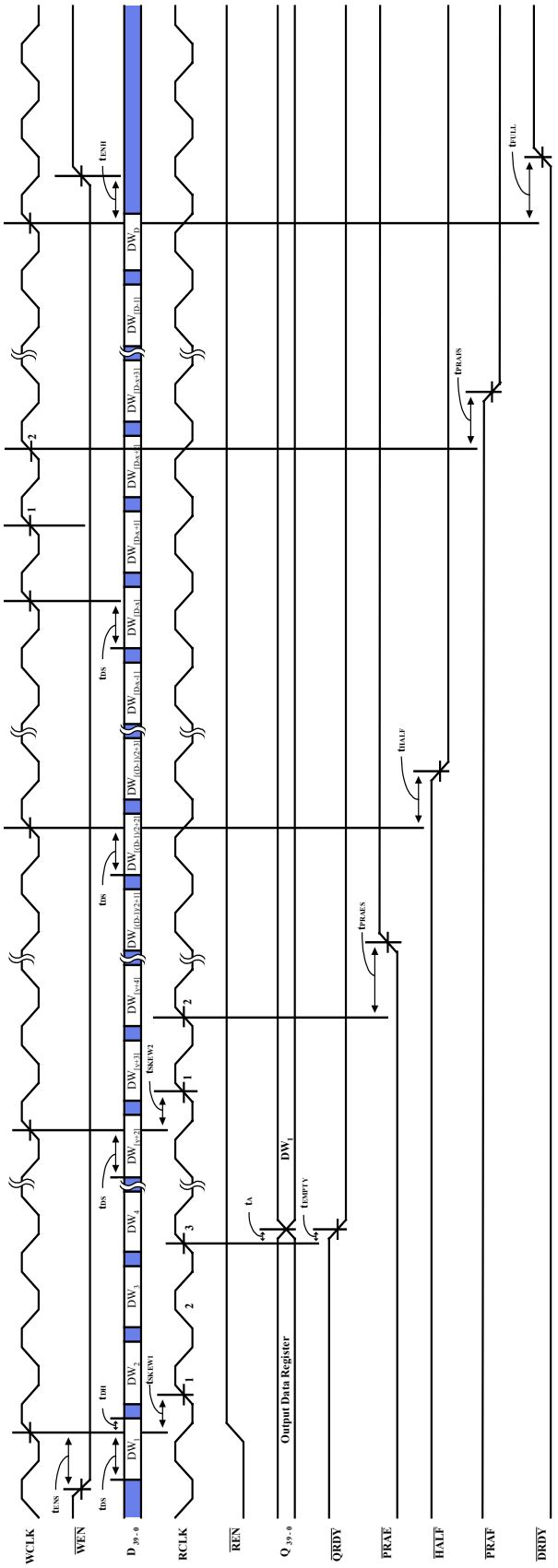

Diagram 5. Write Timing (FWFT Mode)

NOTES:

1. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to tSKEW1, $\overline{QRDY}$ will go low (after two RCLK cycle plus tEMPTY). If tSKEW1 is not met, then $\overline{QRDY}$ will assert 1 or more RCLK cycles.
2. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to tSKEW2, $\overline{PRAE}$ will go high (after one RCLK cycle plus tPRAES). If tSKEW2 is not met, then $\overline{PRAE}$ will assert 1 or more RCLK cycles.
3. $\overline{LOAD}$ = High, $\overline{OE}$ = Low.
4. y = $\overline{PRAE}$ offset, x = $\overline{PRAF}$ offset.
5. D = maximum queue depth. Please refer to Table 9 for Depth.
6. First word latency: tSKEW1 + tEMPTY + 2 * tRCLK

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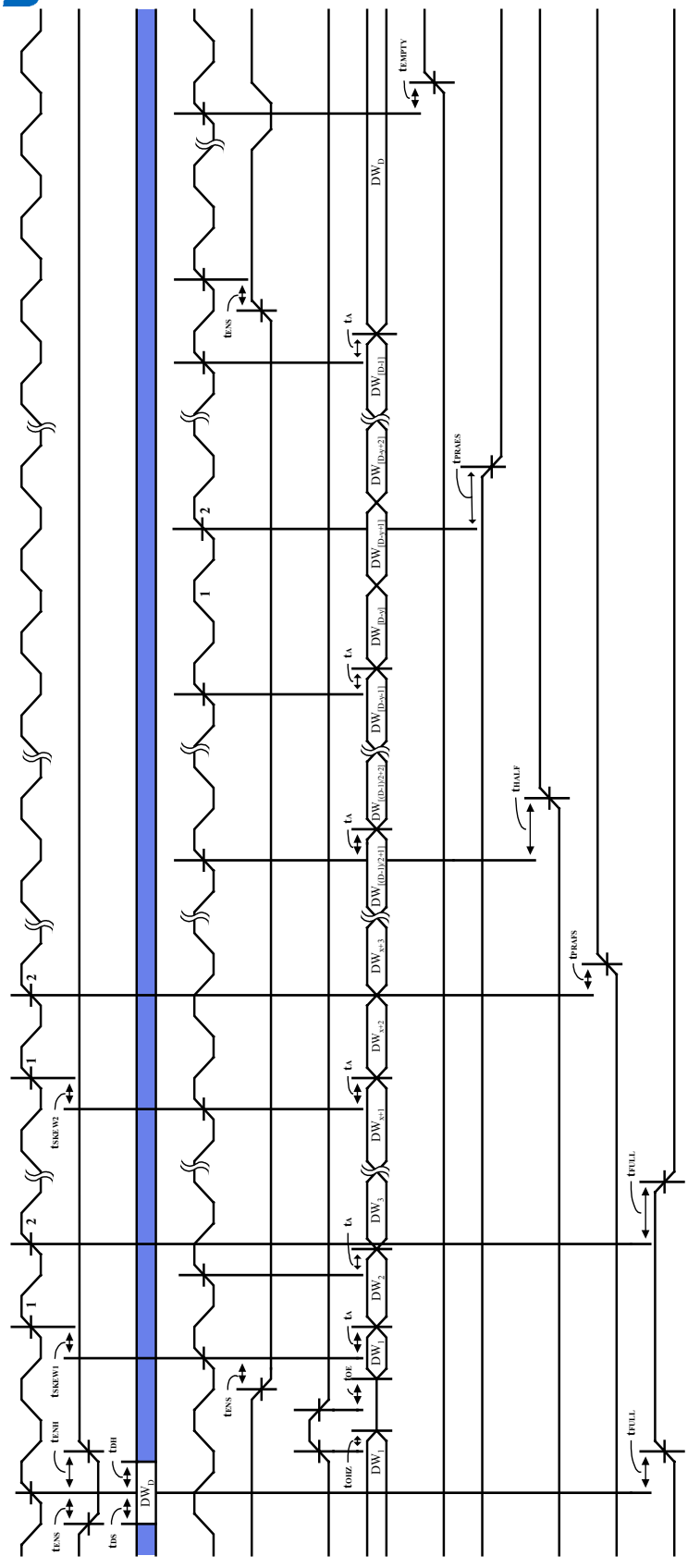

Diagram 6. Read Timing (FWFT Mode)

NOTES:

1. If the time between a rising edge of RCLK to the rising edge of WCLK is greater than or equal to t_{SKEW1}, $\overline{DRDY}$ will go low (after one WCLK cycle plus t_{FULL}) . If t_{SKEW1} is not met, then $\overline{DRDY}$ will assert 1 or more WCLK cycles.
2. If the time between a rising edge of RCLK to the rising edge of WCLK is greater than or equal to t_{SKEW2}, $\overline{PRAF}$ will go high (after one WCLK cycle plus t_{PRAFS}) If t_{SKEW2} is not met, then $\overline{PRAF}$ will assert 1 or more WCLK cycles.
3. $\overline{LOAD}$ = High
4. y = $\overline{PRAE}$ Offset, x = $\overline{PRAF}$ offset.
5. D = maximum queue depth. Please refer to Table 9 for Depth.

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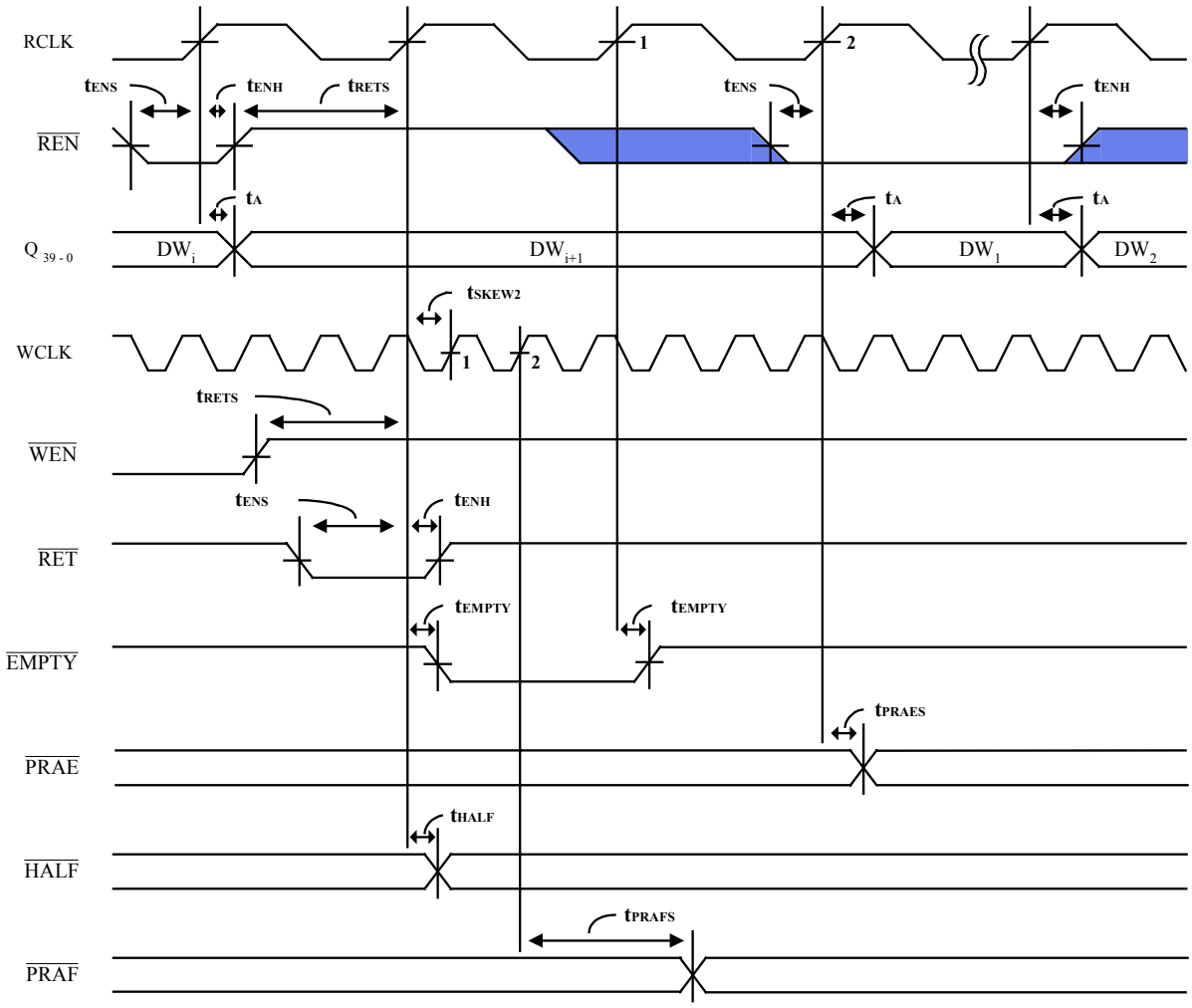

NOTES:
1. Upon completion of retransmit setup, a read operation can begin only after $\overline{\text{EMPTY}}$ returns high.
2. $\overline{\text{OE}}$ = Low.
3. DW_i = Words written to the queue after $\overline{\text{MRST}}$. Where i = 1,2,3… depth.
4. Upon reset completion, there must be more than two words written to the queue for a retransmit setup to be valid.

Diagram 7. Retransmit Timing (Standard Mode)

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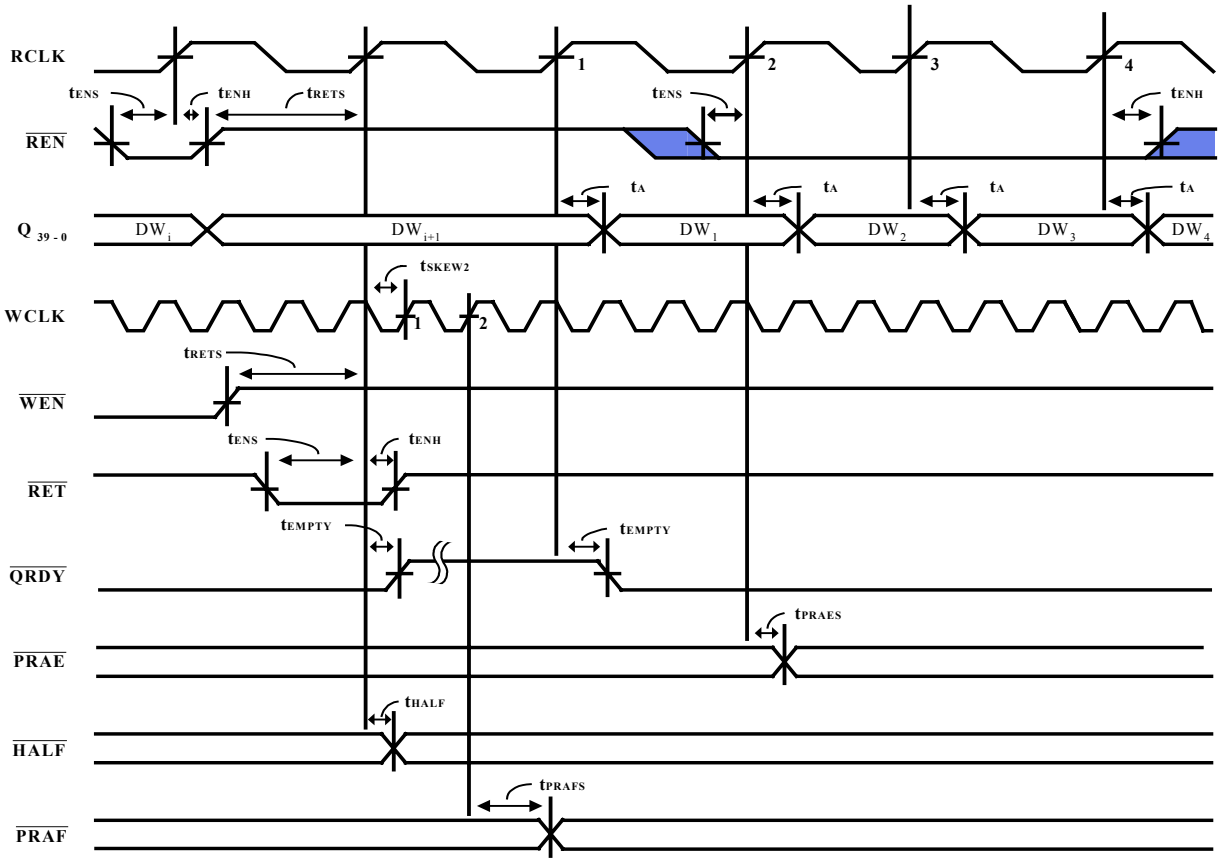

NOTES:
1. Upon completion of retransmit setup, a read operation can begin only after $\overline{QRDY}$ returns low.
2. $\overline{OE}$ = Low.
3. DW_i = Words written to the queue after $\overline{MRST}$. Where i = 1,2,3… depth.
4. Upon reset completion, there must be more than two words written to the queue for a retransmit setup to be valid.
5. Please refer to Table 9 for Depth.

Diagram 8. Retransmit Timing (FWFT Mode)

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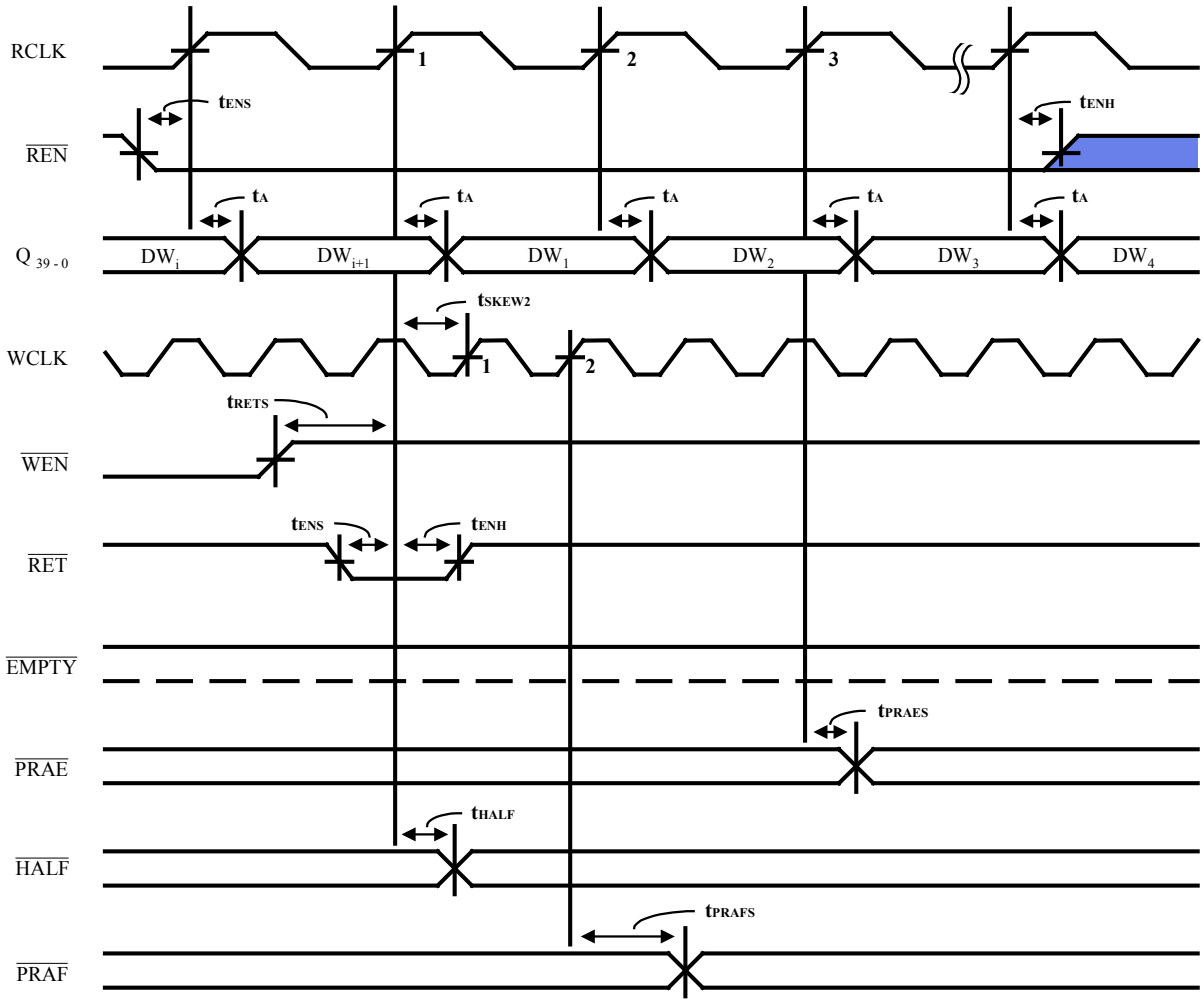

NOTES:

1. If the part is empty at the point of retransmit, the Empty Flag ($\overline{\text{EMPTY}}$) will be updated based on RCLK (Retransmit Clock cycle). Valid data will appear on the output.
2. $\overline{\text{OE}}$ = Low; enables data to be read on outputs Q_{39-0}.
3. DW_1= first word written to the queue after Master Reset; DW_2= second word written to the queue after Master Reset.
4. No more than D-2 may be written to the queue between reset (Master or Partial) and retransmit setup. Therefore, $\overline{\text{FULL}}$ will be high throughout the retransmit setup procedure. Please refer to Table 9 for Depth.
5. There must be at least two words written to zero latency retransmit from the queue before a retransmit operation can be invoked.
6. $\overline{\text{RETZL}}$ is set Low during $\overline{\text{MRST}}$.

Diagram 9. Zero Latency Retransmit Timing (Standard Mode)

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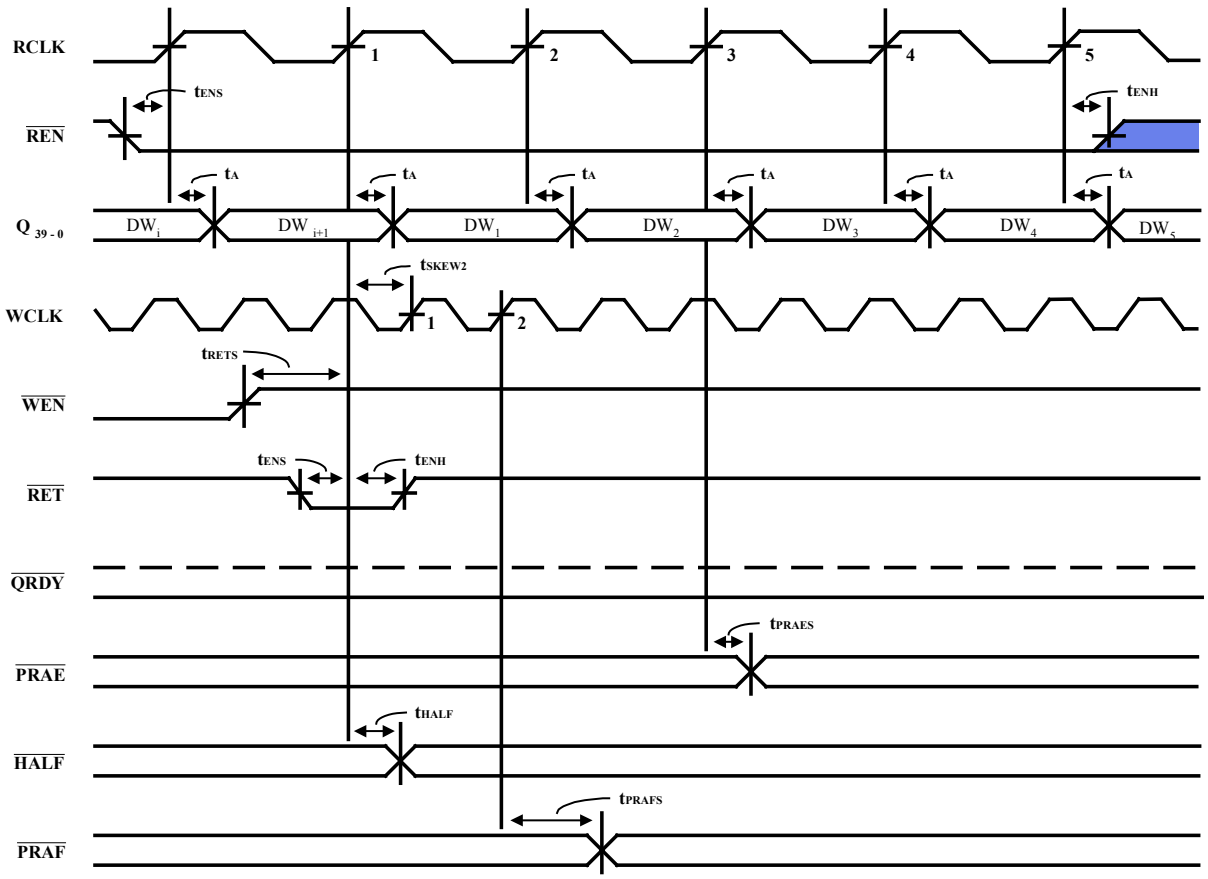

NOTES:

1. If the part is empty at the point of retransmit, the output ready flag ($\overline{\text{QRDY}}$) will be updated based on RCLK (Retransmit Clock cycle). Valid data will appear on the output.
2. No more than D-2 words may be written to the queue between reset (Master or Partial) and retransmit setup. Therefore, $\overline{\text{DRDY}}$ will be low throughout the retransmit setup procedure. Please refer to Table 9 for Depth.
3. $\overline{\text{OE}}$ = Low.
4. DW_1, DW_2, DW_3 = first, second and third words written to the queue after Master Reset.
5. There must be at least two words written to the queue before a retransmit operation can be invoked.
6. $\overline{\text{RETZL}}$ is set low during $\overline{\text{MRST}}$.

Diagram 10. Zero Latency Retransmit Timing (FWFT Mode)

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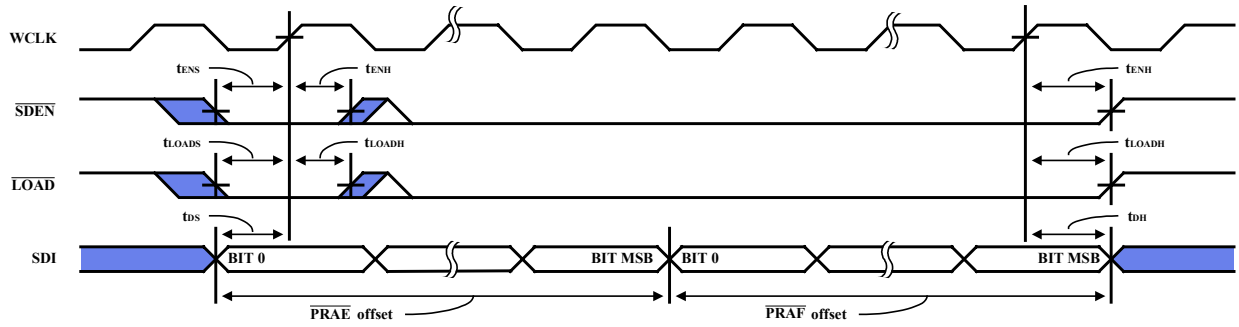

*Refer to Table 11

Diagram 11. Serial Loading of Programmable Flag Registers (Standard and FWFT Mode)

	CQV8110	CQV8100	CQV890	CQV880	CQV870	CQV860	CQV850	CQV840
MSB	16	15	14	13	12	11	10	9

Table 11. Reference Table for Diagram 11

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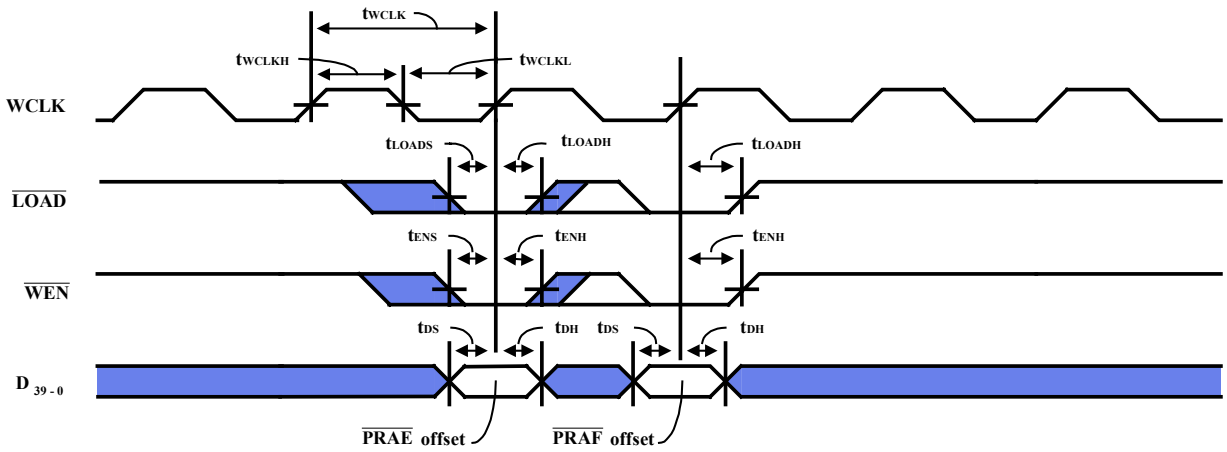

Diagram 12. Parallel Loading of Programmable Flag Registers (Standard and FWFT Mode)

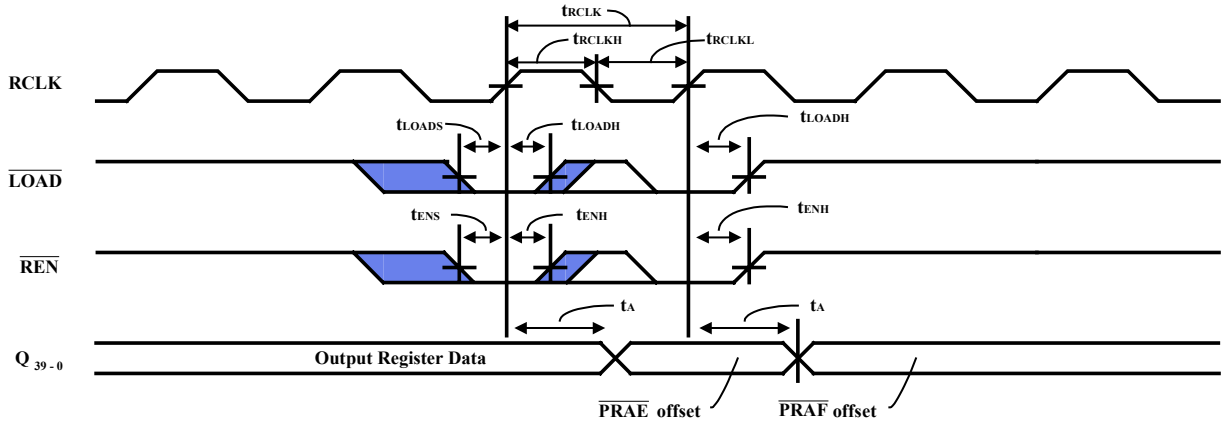

Diagram 13. Parallel Read of Programmable Flag Registers (Standard and FWFT Mode)

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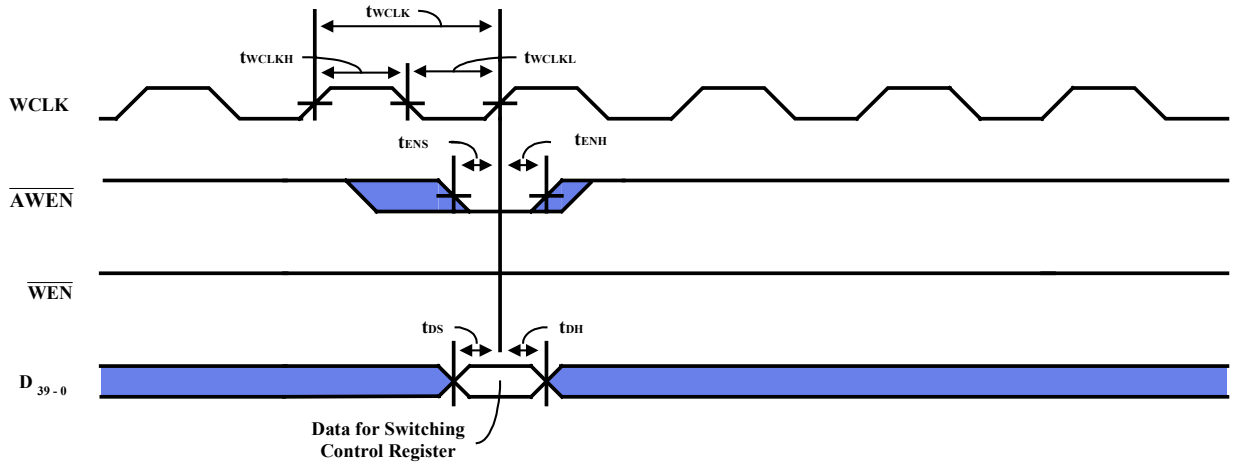

Diagram 14. Programming the Switching Control Register

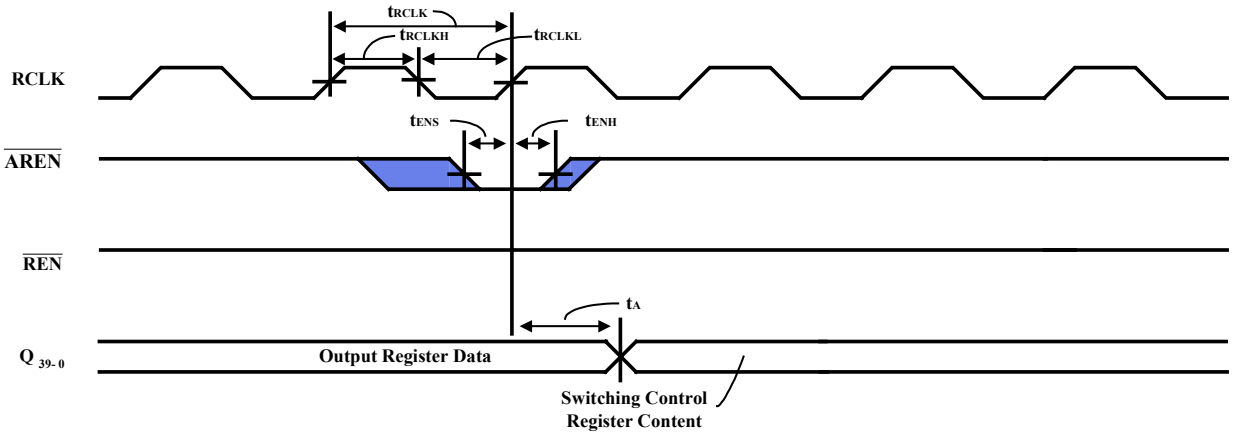

Diagram 15. Reading the Switching Control Register

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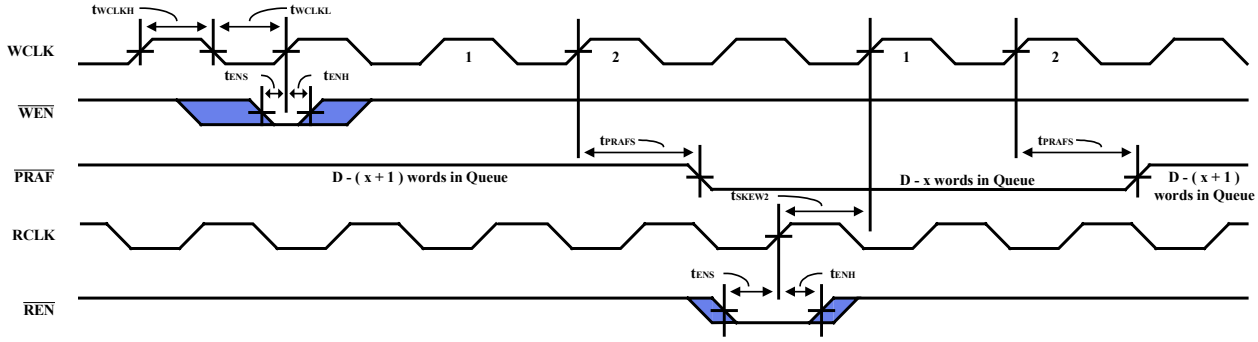

NOTES:

1. x = $\overline{\text{PRAF}}$ offset.
2. D = maximum queue depth. Please refer to Table 9 for Depth.
3. If the time between a rising edge of RCLK to the rising edge of WCLK is greater than or equal to tSKEW2, $\overline{\text{PRAF}}$ will go high (after on WCLK cycle plus tPRAFS). If tSKEW2 is not met, then $\overline{\text{PRAF}}$ will assert 1 or more WCLK cycles.
4. $\overline{\text{PRAF}}$ synchronizes to the rising edge of WCLK only.

Diagram 16. Synchronous Programmable Almost-Full Flag Timing (Standard and FWFT Mode)

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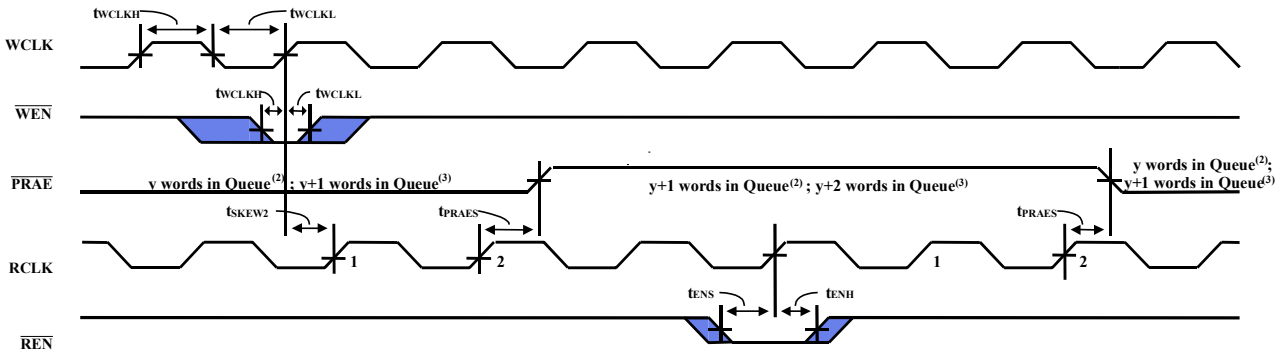

NOTES:

1. y = $\overline{\text{PRAE}}$ offset.
2. For Standard Mode.
3. For FWFT Mode.
4. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to t_{SKEW2}, $\overline{\text{PRAE}}$ will go high (after one RCLK cycle plus t_{PRAES}). If t_{SKEW2} is not met, then $\overline{\text{PRAE}}$ will assert 1 or more RCLK cycles.
5. $\overline{\text{PRAE}}$ synchronizes to the rising edge of RCLK only.

Diagram 17. Synchronous Programmable Almost-Empty Flag Timing (Standard and FWFT Mode)

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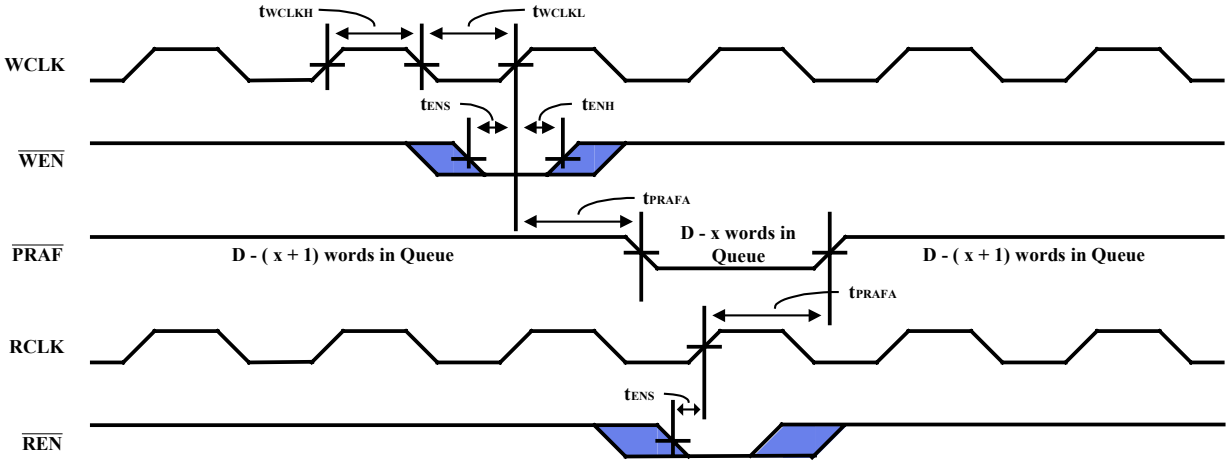
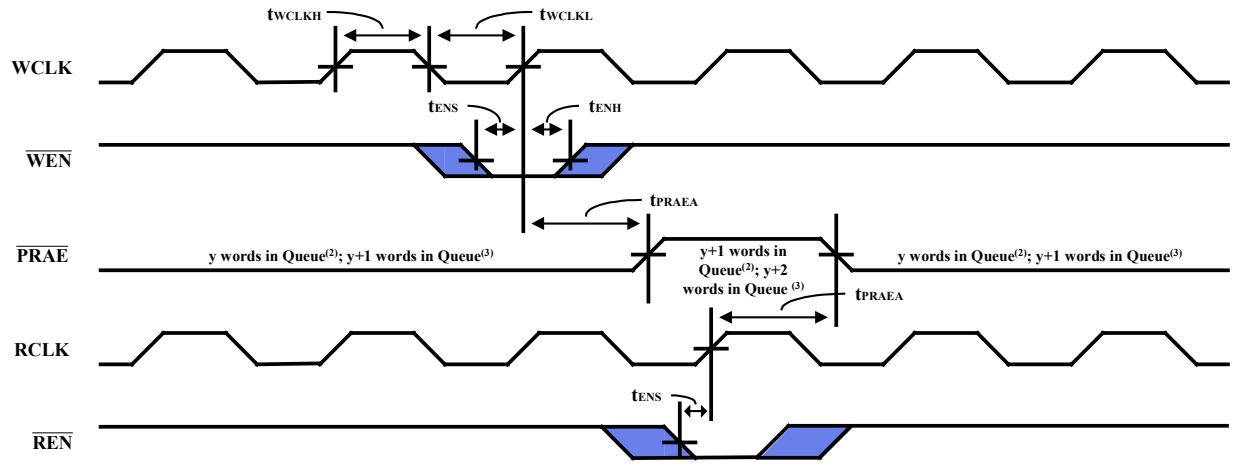


NOTES:
1. x = $\overline{\text{PRAF}}$ offset.
2. D = maximum queue depth. Please refer to Table 9 for Depth.
3. $\overline{\text{PRAF}}$ is asserted to low on WCLK transition and reset to high on RCLK transition.
4. Select this mode by setting SFM low during Master Reset.

Diagram 18. Asynchronous Programmable Almost-Full Flag Timing (Standard and FWFT Mode)



NOTES:
1. y = $\overline{\text{PRAE}}$ offset.
2. For Standard Mode.
3. For FWFT Mode.
4. $\overline{\text{PRAE}}$ is asserted to low on RCLK transition and reset to high on WCLK transition.
5. Select this mode by setting SFM low during Master Reset.

Diagram 19. Asynchronous Programmable Almost-Empty Flag Timing (Standard and FWFT Mode)

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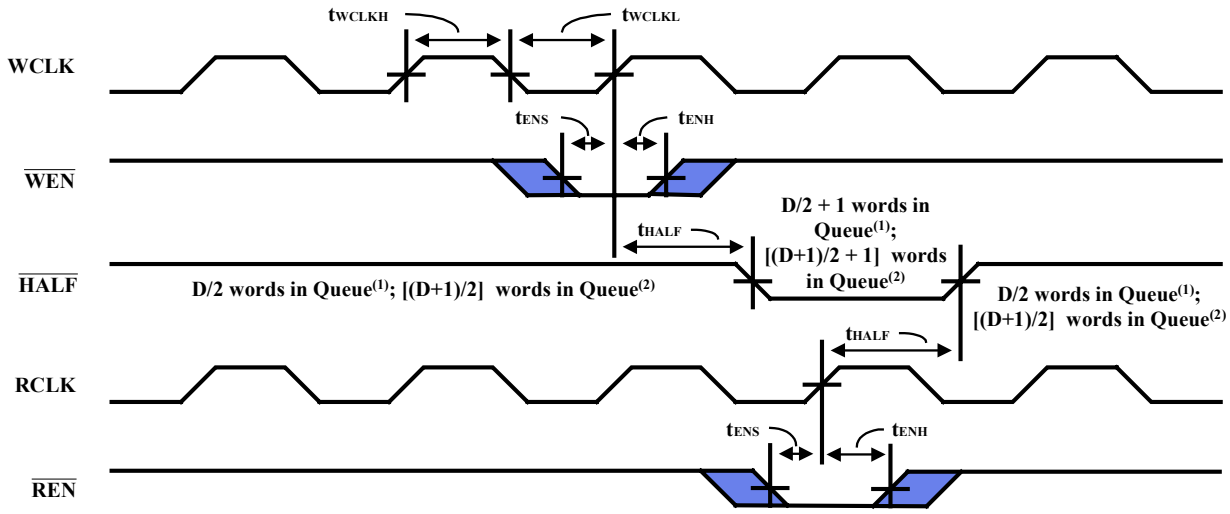

NOTES:
1. For Standard Mode.
2. For FWFT Mode.
3. Please refer to Table 9 for Depth.

Diagram 20. Half-Full Flag Timing (Standard and FWFT Mode)

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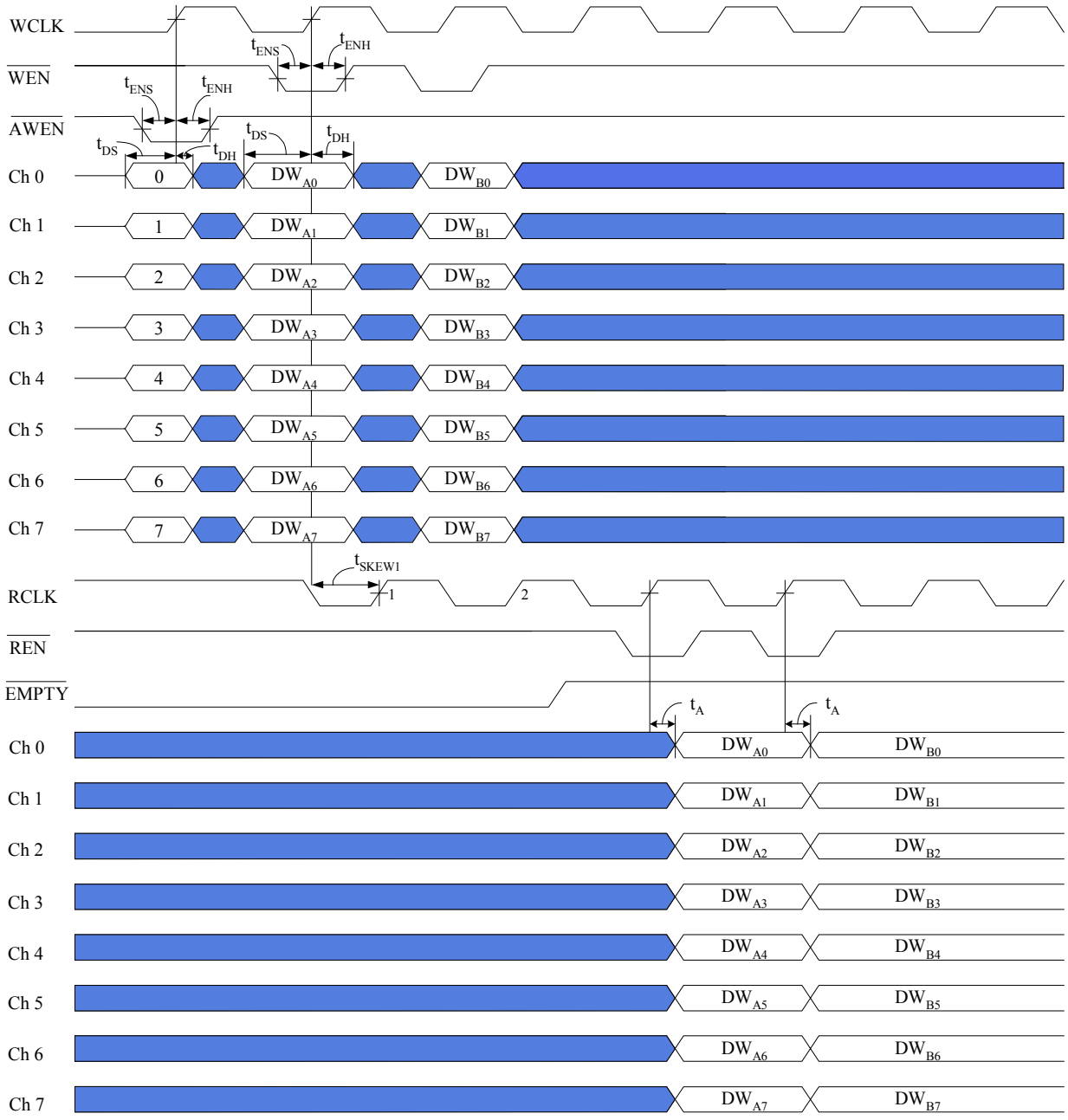

NOTES:

1. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to t_{SKEW11}, $\overline{EMPTY}$ will go high (after RCLK cycle plus t_{EMPTY}). If t_{SKEW1} is not met, then $\overline{EMPTY}$ will assert 1 or more RCLK cycles.

Diagram 21. Unicast Mode

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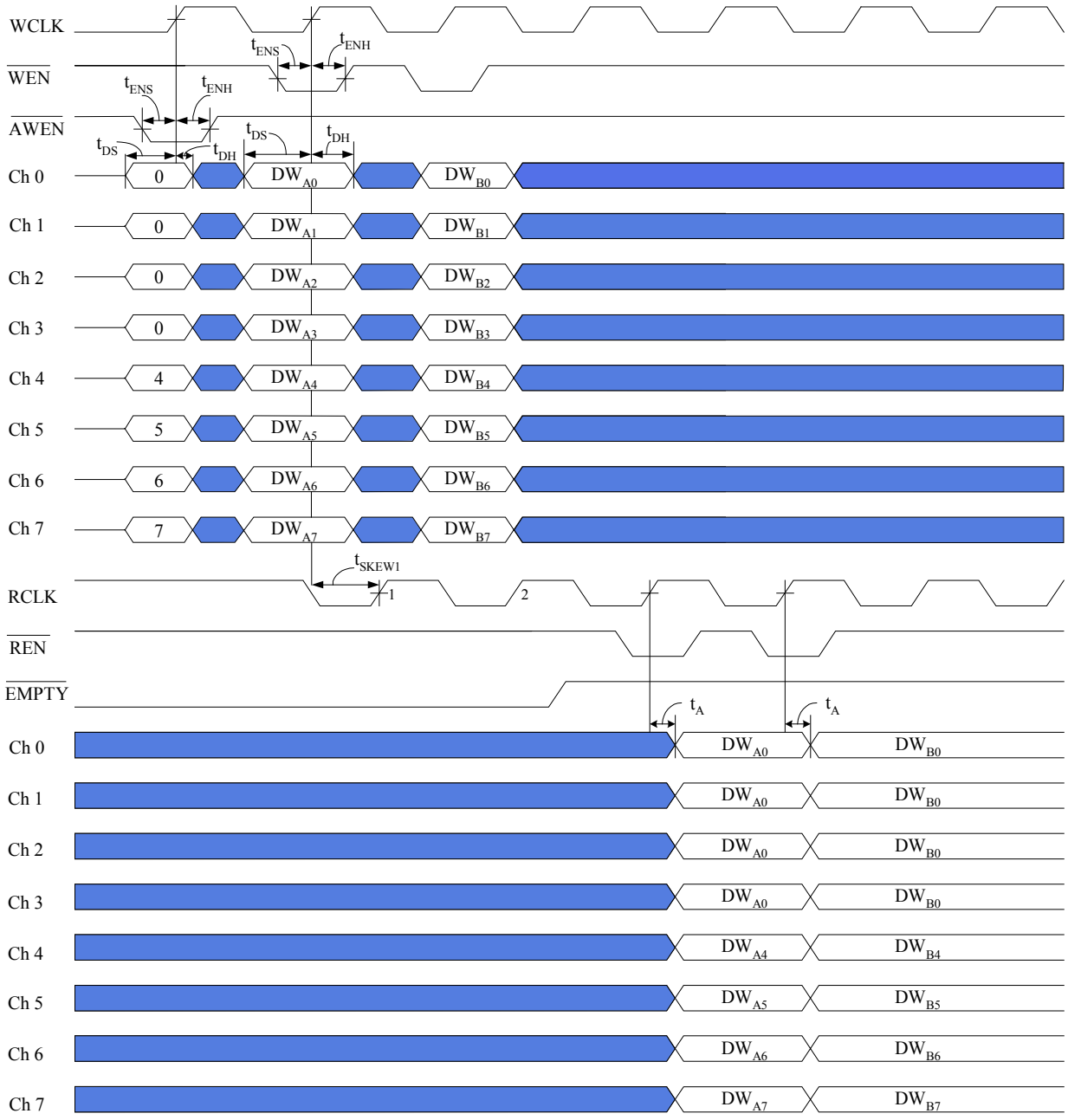

NOTES:

1. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to t_{SKEW11}, $\overline{EMPTY}$ will go high (after RCLK cycle plus t_{EMPTY}). If t_{SKEW1} is not met, then $\overline{EMPTY}$ will assert 1 or more RCLK cycles.

Diagram 22. Multicast Mode

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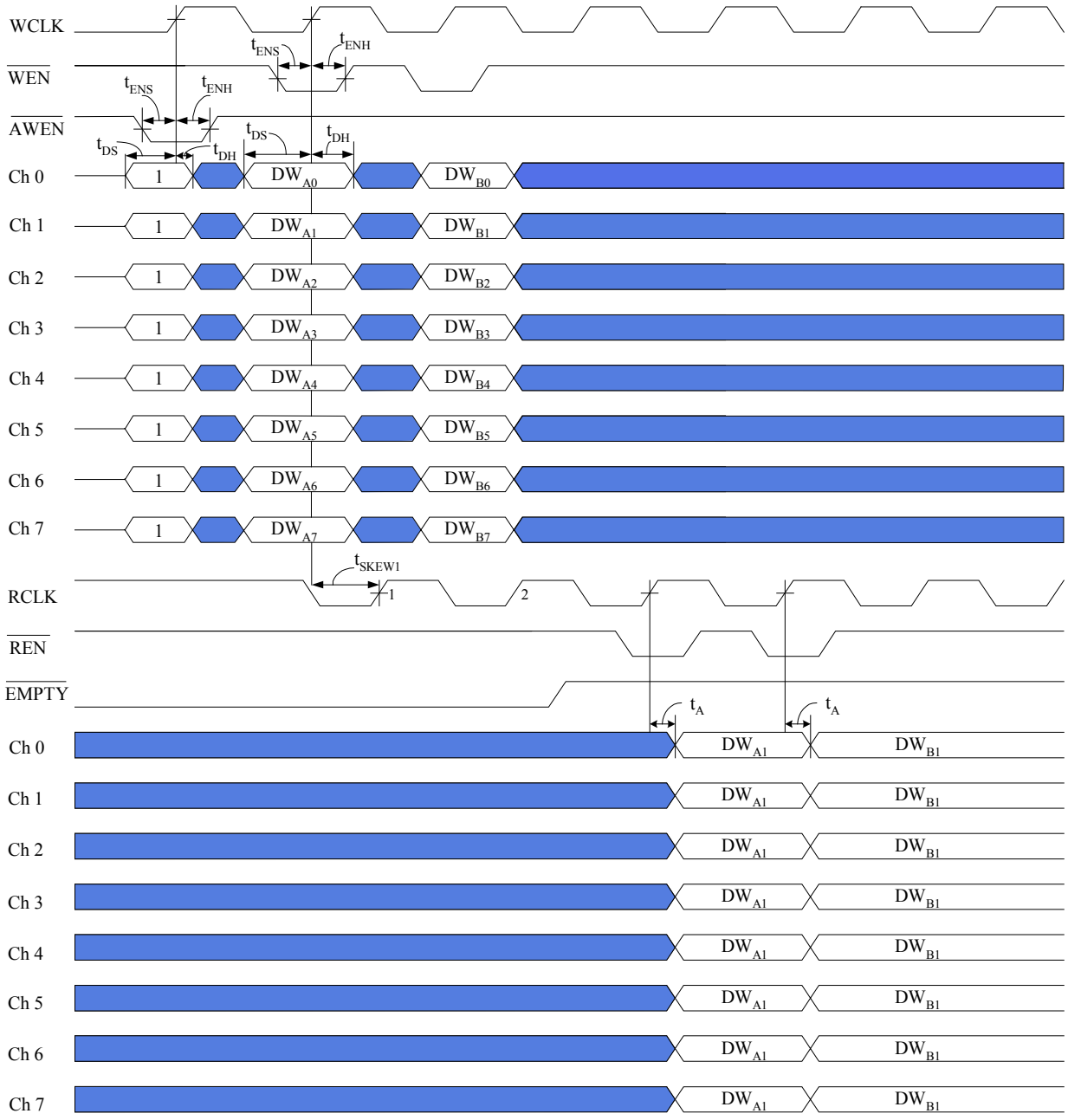

NOTES:

1. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to t_{SKEW11}, $\overline{EMPTY}$ will go high (after RCLK cycle plus t_{EMPTY}). If t_{SKEW1} is not met, then $\overline{EMPTY}$ will assert 1 or more RCLK cycles.

Diagram 23. Broadcast Mode

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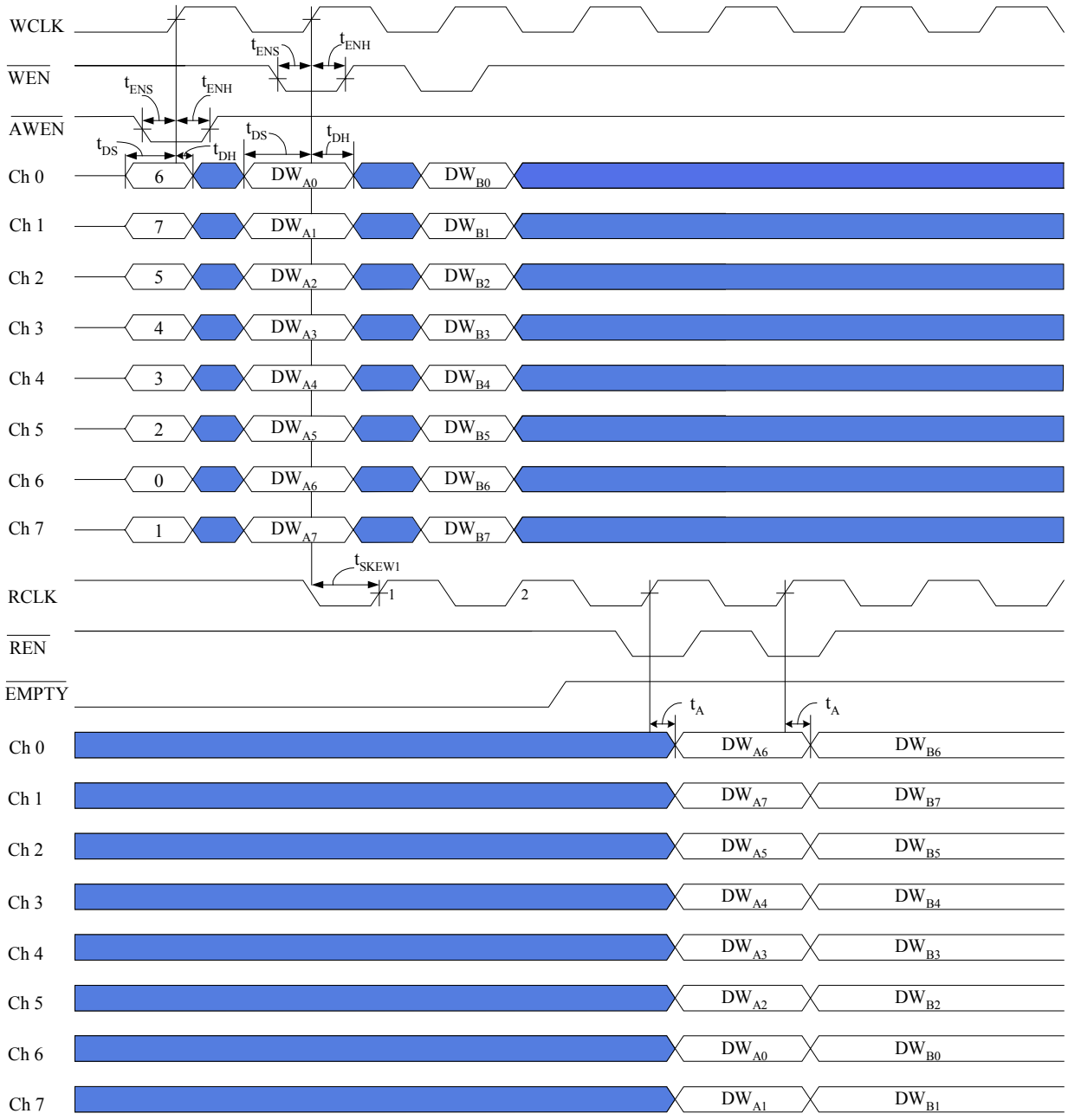

NOTES:

1. If the time between a rising edge of WCLK to the rising edge of RCLK is greater than or equal to t_{SKEW11}, $\overline{EMPTY}$ will go high (after RCLK cycle plus t_{EMPTY}). If t_{SKEW1} is not met, then $\overline{EMPTY}$ will assert 1 or more RCLK cycles.

Diagram 24. Switching Mode

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Order Information:

HBA Device Family	Device Type	Power	Speed (ns) *	Package**	Temperature Range
XX	XXXXX	X	XX	XX	X
CQ	**V8110** (131,072 x 40)	**L**ow	**6** – 166 MHz	**PF**	Blank – Commercial (0°C to 70°C)
	V8100 (65,536 x 40)		**7-5** – 133 MHz		**I** – Industrial (-40° to 85°C)
	V890 (32,768 x 40)		**10** – 100 MHz		
	V880 (16,384 x 40)		**15** – 66 MHz		
	V870 (8,192 x 40)				
	V860 (4,096 x 40)				
	V850 (2,048 x 40)				
	V840 (1,024 x 40)				

***Speed –** 6ns available only in Commercial temp (0°C to 70°C)
****Package** – 144 - pin Plastic Thin Quad Flat Pack (TQFP)

Example:

CQV880L6PF (16k x 40, 6ns, Commercial temp)
CQV870L10PFI (8k x 40, 10ns, Industrial temp)

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