PHYSICAL UNDERSTANDING OF THE EFFECT OF INTERFACE TRAPS AND GRAIN BOUNDARY STATES ON THE ELECTRICAL CHARACTERISTICS OF P-TYPE POLYSILICON NANOWIRES FABRICATED BY DEPOSITION AND SPACER ETCH TECHNIQUE FOR BIOSENSORS

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Submitted to the

Department of Electrical and Electronic Engineering
Faculty of Sciences and Engineering
East West University

In Partial Fulfillment of the Requirements for the Degree of
Bachelor of Science in Electrical and Electronic Engineering
(B.Sc. in EEE)

Summer, 2013

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Abstract

This thesis investigates the effects of interface traps and p-type polysilicon grain boundary defects on the electrical characteristics of p-type polysilicon nanowires (NWs). It is observed that acceptor-like interface trap states affect the leakage current of the NW whereas donor-like interface traps affect both subthreshold slope and drive current of NW. Defects inside polysilicon also exhibits some important trend. Acceptor-like tail states do not affect the NW electrical characteristics whereas acceptor-like Gaussian states affect the leakage current. However, donor-like defects both in tail like and deep level Gaussian like distribution affect NW subthreshold characteristics and drive current. These physical understandings of different types of defects are used to calibrate p-type polysilicon NW fabricated by deposition and etch technique which allowed us to extract different types of defects. This knowledge is very important to explain the p-type polysilicon NW biosensor behavior which has been recently shown to be the only viable route for mass manufacture of NW biosensors.

Acknowledgements

First of all, we are grateful to Almighty Allah for granting us such an opportunity to work with this research.

We would like to express our sincere thanks and gratitude to our research supervisor Dr. Mohammad Mojammel Al Hakim, Chairperson and Associate professor, Department of Electrical and Electronic Engineering, East West University, Dhaka, Bangladesh for continuous support, motivation and guidance in the development of this research. It gives us a great impression to have had the opportunity to work with him throughout our research.

We would also like to thank all the faculty members of Department of Electrical and Electronic Engineering for their supports and untiring effort in the management of quality education.

And we would like to thank our parents for blessing and our friends, well wishers who helped us in the completion of this research.

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

Page

LIST OF TABLES

Page

Chapter 1

Introduction

1.1 Motivation and Objective

Over the past decades, semiconductor nanowires attracted quite a lot of attractors due to their unique electrical characteristics suitable for biochemical sensors [1-4]. The reason of interest is due to label free high sensitivity detection of Biomolecules [5-10] without expensive optical components [11-17]. The ultra-high sensitivity is due to their smaller size and large surface to volume ratio enables single charge at the surface of the nanowires to deplete or accumulate entire cross section area of nanowires [18-19].

There are two major approach for Si NWs biosensors fabrication namely bottom-up and top-down. Bottom-up approach is a simple and cheap process usually done using metal-catalytic associated nanowire growth. This process is followed by an integration step such as electric field or fluid-flow-assisted nanowire positioning between lithographically defined source and drain electrodes. Such a non CMOS device fabrication process is not at all suitable for mass production of nanowires [20]. Top-down approach is attractive for nanowire fabrication due to location control nanowire definition. To fabricate Si NWs on silicon-on-insulator (SOI) substrates using top down approach several researchers have used nano pattering techniques such as deep-UV [21] lithography (steppers) and electron beam lithography [22-23]. This has the great advantages of CMOS compatibility, but a serious disadvantage is high cost due to advanced lithography technology needed for fabrication. In advanced lithography technology, expensive light sources and optics are required which increase the cost of fabrication.SOI wafer's wet etch has also been researched for creating triangular nanowires but wet etching is unfavorable by industry, because it does not provide a clear route of manufacturing. Recently, top-down approaches for nanowire fabrication reported which uses of thin film technology and the spacer etch technique [24-26]. This approach is particularly attractive because it can produce nanoscale dimensions polysilicon nanowires by using conventional lithography that are widely available in industry in combination with standard deposition and spacer etch techniques. However, in this approach defined nanowires are usually amorphous and/ or polysilicon depending on the deposition and annealing conditions.

Polysilicon nanowires are usually composed of grain boundaries and defects inside the material where may significantly affect its conduction properties. In addition, grain boundaries usually segregate doping which results in the reduction of the activated dopant concentration. Depending on the process conditions the surface polysilicon nanowires may contain trap states which may also affect its electrical characteristics eventually affecting biosensor properties if fabricated on polysilicon nanowires. So far several works of the biosensors fabrication using polysilicon nanowire have been reported [27-30]. An excellent defection limit of 10fM in presence of 100,000 excess non targeted proteins has also been reported using polysilicon nanowires [31].

Silicon nanowire based biosensors are actually based on the conductance charge upon attachment of the Biomarkers which is equivalent to the application of gate voltages in conventional MOSFETS. Nanowires are recently in significant attraction for the application as simple Si-NWs are shown to exhibit transistor like behavior [32]. Sub-threshold regions of nanowires are imperative for sensors application as large conductance charge can be done upon attachment of biomolecules in a properly biased nanowire. However, sub-threshold characteristics of polysilicon NWs are expected to be different from single crystal Si NWs as conduction is significantly affected by the presence of the grain boundary defects. So far no work has been reported in the literature studying the effects of grain boundary defects and interface traps on the electrical characteristics of polysilicon NWs.

In this work we investigate for the first time the effect of grain boundary defects and interface traps on the conduction properties of polysilicon NW. Influence of different types of defects inside the polysilicon and in the insulator-Si interface states are studied in detail to gain a profound physical understanding of the polysilicon NW conduction properties.

The simulated results are calibrated with the polysilicon NWs electrical characteristics [31] to find out the range of grain boundary trap states and interface states that can be expected of nanowires are fabricated using deposition and etch method as reported in [31]. These results are very important for thin film based NW biosensor fabricate which has been reported as the only mass-manufacturable platform for biosensor fabrication.

1.2 Organization / Thesis Outline

Chapter 1 provides the importance, motivation and outline of this research.

Chapter 2 provides the necessary background theory to describe the carrier trapping mechanism at grain boundaries. Carrier trapping leads to the formation of the potential barriers that are limiting mechanism in carrier transport through polysilicon films. The model derived assumes a mono-energetic trap level, however this is not realistic so we finish by discussing the inclusion of a continuum of trap states across the energy band gap. Therefore we go on to look at the implementation of carrier emission/absorption process from deep trap sates in our numerical simulation tools.

Chapter 3 describes the simulation methodology, device structure and the required models for device simulation.

Chapter 4 describes the effect of grain boundaries and interface states on the electrical characteristics of p-type polysilicon nanowires. As effect of different types interface states and grain boundary defects are studied in detail to gain physical understanding of p-type polysilicon nanowire behavior. This knowledge is used to calibrate experimentally observed p-type polysilicon nanowire characteristics and to extract the range of interface states and grain boundary defects that can be expected if nanowires are fabricated using deposition and spacer etch technique.

Chapter 5 summarizes results of this work and finally chapter 6 describes limitation of this work and possible future venues for improvement.

Chapter 2

Carrier Transport in Polysilicon Films

2.1 Electrical Properties of Polysilicon Films

A polysilicon film is composed of small crystallites joined together by grain boundaries, where the angle between the adjoining crystallites is often large. Inside each crystallite the atoms are arranged in a periodic manner hence behaves like a small single crystal. The grain boundary itself is a complex structure, usually consisting of a few atomic layers of disordered atoms and a large number of defects due to incomplete atomic bonding. Several models have been proposed to explain the electrical behavior of polysilicon films. The most well-known being the competing theories of carrier trapping and segregation. In the segregation theory, it was proposed that dopant atoms can segregate to the grain boundary because of their lower energy in the disordered GB region, and therefore do not contribute to the conduction process. This would mean that the number of carriers free for conduction would be significantly less than in a, similarly doped, single crystal silicon film. The main failing of segregation theory is that it does not explain the temperature dependence of resistivity in moderately doped polysilicon films, which is thermally activated and displays a negative temperature coefficient. The competing carrier trapping theory was first proposed by Kamins [33] and then later developed into a comprehensive theory of carrier transport by Seto [34]. It has successfully explained most of the electrical properties of polysilicon for the special case where the depletion region extends throughout the entire crystallite. Baccarani *et al*. [35] published a series of results that Seto's approximation of a monovalent trap energy level was valid. Throughout this work Seto's theory is used as the conceptual basis for explaining conduction phenomena in polysilicon.

2.2 Seto's Carrier Trapping Theory

It is known that there are a large number of defects due to incomplete atomic bonding at the grain boundary. These defects in the grain boundary are locations where it is possible for carriers to become trapped and immobilized. This results in the traps themselves, and therefore the grain boundary becoming electrically charged. To satisfy charge neutrality an

oppositely charged depletion layer of finite width forms on either side of the GB. As a consequence the energy bands are bent at the GB creating a notch or barrier, which acts to impede carrier transport through the film. The trapping of carriers would therefore, decrease both the carrier concentration and the mobility of the material.

2.2.1 Carrier Trapping at Grain Boundaries

In Seto's model a number of assumptions were made to simplify his analysis.

1. The polysilicon film is composed of identical crystallites with a grain size of $L(cm)$. In a real polysilicon film there can be large variations in the size and orientation of the grains.
2. There is only one type of impurity atom present and they are full ionized and uniformly distributed with a concentration of $N(cm^{-3})$. Minority carriers and their associated traps are not considered in the analysis.
3. Inside the crystallites the single-crystal band structure of silicon is applicable. Therefore he is assuming that the structure inside each crystallite is perfect and defect free, which is not necessarily true.
4. The grain boundary is of negligible thickness compared to the grain size L with $N_T(cm^2)$ of traps located at trap energy E_t with respect to the intrinsic Fermi level. In a real polysilicon film the traps energies are distributed across the energy gap of the band structure. Although Baccarani *et al*. [35] concluded that a mono-energetic approximation of the trap states was sufficient to successfully model the behavior of a polysilicon film.

The resulting energy band structure and charge distribution for a polysilicon film with two grain boundaries is shown in Fig. 2.1. All the mobile carriers in the region of $\left(\frac{1}{2}L - l\right)\ cm$ from the grain boundary are trapped by the trapping states resulting in a depletion of a potential barrier in the band structure. In this analysis is considered sufficient to treat the problem in one dimension. Under this assumption Poisson's equation becomes

$$\frac{d^2V}{dx^2} = \frac{qN}{\epsilon}, l < |x| < \frac{1}{2}L \qquad (2.1)$$

where ϵ is the dielectric permittivity of polysilicon. Integrating equation (2.1) twice and applying the boundary conditions that $V(x)$ is continuous and $\frac{dV}{dx} = 0$ when $x = l$ gives us

$$V(x) = \frac{qN}{2\epsilon}(x - l)^2 + V_{VO}, l < |x| < \frac{1}{2} \qquad (2.2)$$

where V_{VO} is the potential of the valence band edge at the center of the crystallite. Throughout the calculation the intrinsic Fermi level is taken to be at zero energy and energy is positive towards the valence band.

There are two cases that we need to consider relating to the doping concentration.

1. $N < \frac{N_T}{L}$ and
2. $N > \frac{N_T}{L}$

where we define a critical doping concentration $N^* = \frac{N_T}{L}$

Below critical doping concentration $N < \frac{N_T}{L}$

Considering first of all the case when $N < \frac{N_T}{L}$. This condition implies that the crystallite is completely depleted of carriers and the traps are partially filled so that $l = 0$ and (2.2) becomes

$$V(x) = V_{VO} + \frac{qN}{2\epsilon}x^2 \qquad (2.3)$$

The potential barrier height V_B is the different between $V(0)$ and $V\left(\frac{1}{2}L\right)$, therefore

$$V_B = \frac{qL^2N}{8\epsilon}, N < \frac{N_T}{L} \qquad (2.4)$$

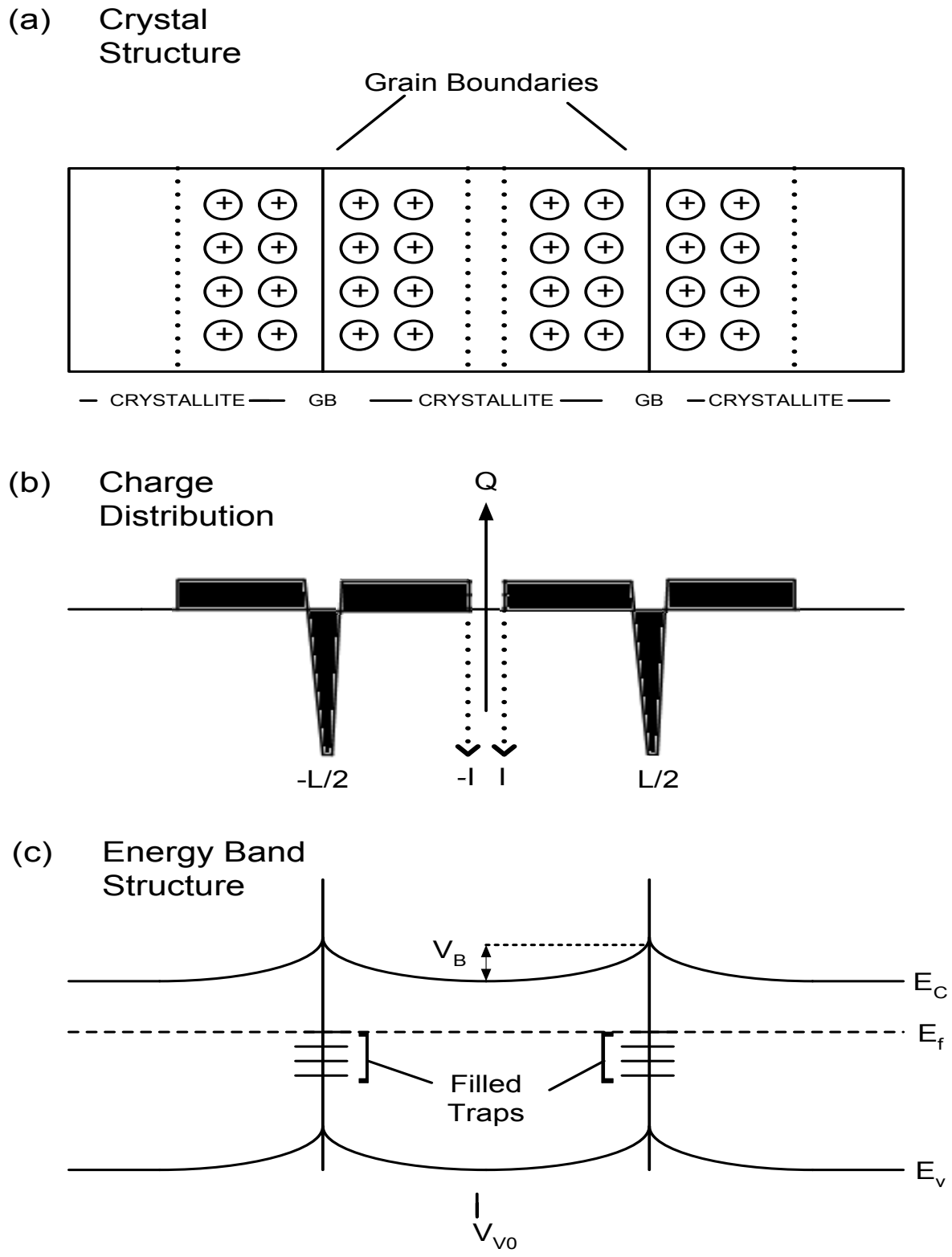

Figure 2.1: (a) The simplified model of the crystallite structure in the polysilicon film showing a single crystallite separated from the two adjoining crystallites by grain boundaries (b) The charge distribution in the structure, showing the negatively charged GB and the surrounding positively charged depletion layer (c) Energy band structure with potential barriers forming at the grain boundaries.

Above the critical doping concentration $N > \frac{N_T}{L}$

In Seto's model the energy of the grain boundary traps is assumed to be deep enough, that they are completely filled, when the dopant concentration exceeds the critical ue $N^* = \frac{N_T}{L}$. As we increase the dopant concentration above this value, the number of trapped carriers remains constant at the value N_T, and the added carriers act to form neutral regions within the grains, as seen in Fig. 2.2. This reduces the depletion region width, but to satisfy charge neutrality the value of charge in the depletion regions width, but to satisfy charge neutrality the value of charge in the depletion region remains constant, albeit in a smaller area. This result in the potential barrier height receding. The width of the depletion region decreases according to the relation

$$x_d = \frac{N_T}{2N} \tag{2.5}$$

Therefore the barrier height when $N > \frac{N_T}{L}$ is found to be

$$V_B = \frac{qN}{2\epsilon} x_d^2 = \frac{qN}{2\epsilon}\left(\frac{N_T}{2N}\right)^2 = \frac{qN_T^2}{8\epsilon N} \tag{2.6}$$

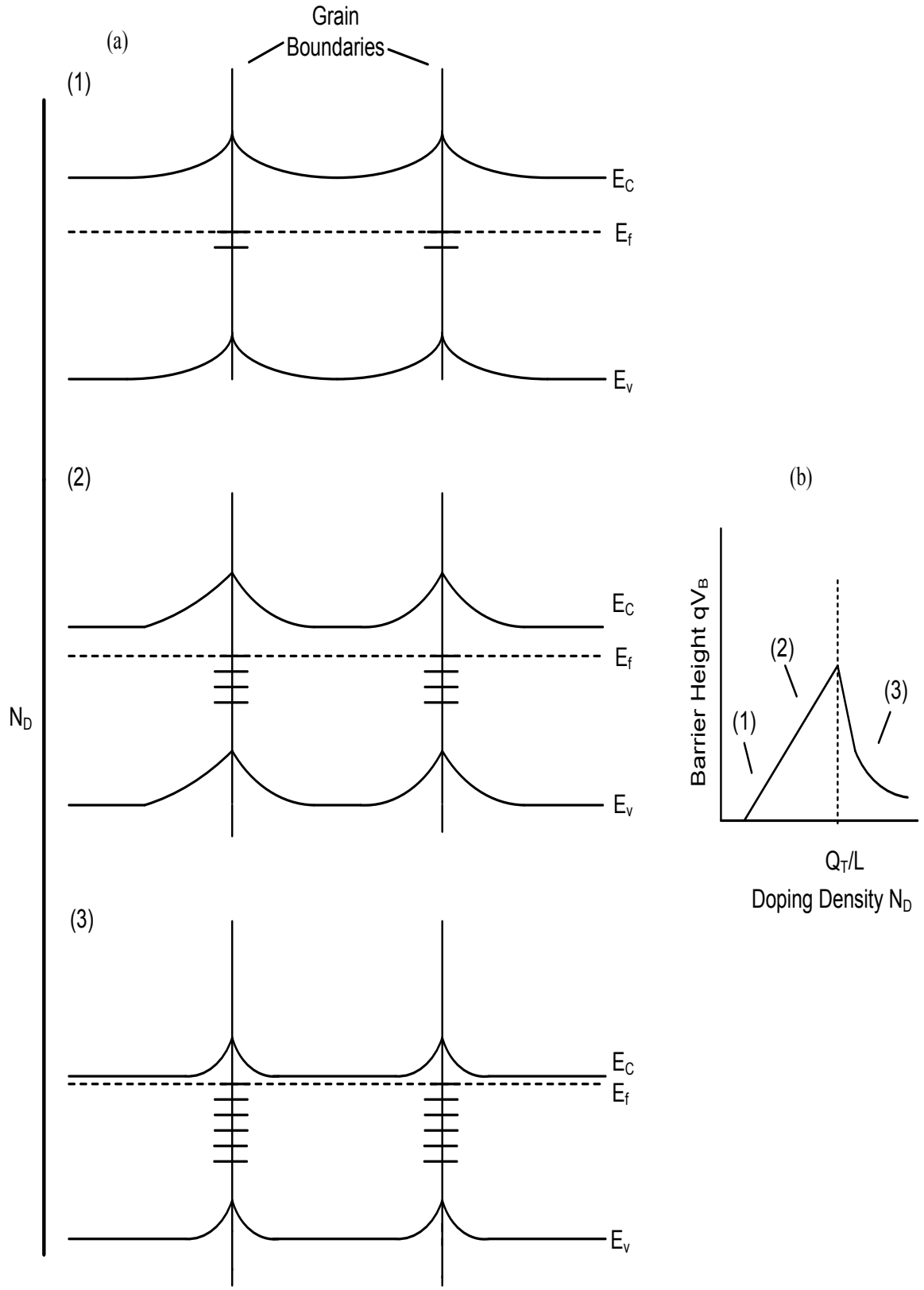

Figure 2.2: (a) As the doping density is increased, the trap states at the grain boundary become filled, increasing the barrier height. When the doping density is increased beyond the critical value N^*, the free carriers reduce the depletion width and the barrier height recedes, (b) barrier height increases linearly as a function of N until reaching the critical value, beyond which it decreases rapidly as a function of $1/N$.

Thus, as shown in Fig. 2.2 as the dopant concentration is increased in the film, firstly the potential barrier increase as a function of N, and then above the critical doping concentration N^* it decreases rapidly as a function of $\frac{1}{N}$.

2.2.2 Carrier Transport in Polysilicon Films

It is assumed that carrier transport, in moderately doped polysilicon films, is dominated by thermionic transport over the barriers. The reasoning being, that even at moderate doping concentration of found around 1×10^{17} cm^{-3} the barrier width is still tens of nanometers wide. Tunnelling is not significant for barriers of this width. At high doping concentrations the barrier is narrow enough that tunnelling may contribute to the current flow, however the barrier height at these concentrations may be low enough for it to be no longer a dominant factor in inhibiting carrier transport.

The thermionic-emission current density J can be written as

$$J = qnv_c exp\left[-\frac{q}{kT}(V_B - V)\right] \qquad (2.7)$$

where n is the free-carrier density, $v_c = \sqrt{\frac{kT}{2\pi m^*}}$ is the collection velocity, V_B is the barrier height with no applied bias, and V is the applied bias across the depletion region.

Under an applied bias the current flow is one direction increases while carrier transport in the other direction decreases. Therefore we must consider current flow in both the forward and reverse directions. The net current density given by; $J = J_F - J_R$. With $V \approx \frac{1}{2}V_G$, where V_G is the bias across one grain boundary.

$$J_F = qnv_c exp\left[-\frac{q}{kT}\left(V_B - \frac{1}{2}V_G\right)\right] \qquad (2.8)$$

$$J_R = qnv_c exp\left[-\frac{q}{kT}\left(V_B - \frac{1}{2}V_G\right)\right] \qquad (2.9)$$

The net current density under applied bias then becomes

$$J = qnv_c exp\left[-\frac{qV_B}{kT}\right]\left[exp\left(\frac{qV_G}{2kT}\right) - exp\left(-\frac{qV_G}{2kT}\right)\right] \qquad (2.10)$$

$$J = 2qnv_c exp\left(-\frac{qV_B}{kT}\right) sinh\left(\frac{qV_G}{2kT}\right) \quad (2.11)$$

We can obtain a linear relationship between current and applied voltage if we make the following simplification for low applied voltages

$$sinh\left(\frac{qV_G}{2kT}\right) \approx \left(\frac{qV_G}{2\mathrm{k}T}\right) \quad (2.12)$$

Therefore

$$J = \frac{q^2 nv_c}{kT}\left[exp\left(-\frac{qV_B}{kT}\right)\right] V_G \quad (2.13)$$

We can now obtain an expression for the conduction $\sigma = \frac{J}{\epsilon} = \frac{JL}{V_G}$

$$\sigma = \frac{q^2 nv_c L}{kT} exp\left(-\frac{qV_B}{kT}\right) \quad (2.14)$$

Thus condition in polysilicon is an activated process with activation energy of approximately qV_B, which depends on the dopant concentration and the grain size. Many analytical models of polysilicon nanowire operation in the subthreshold and turn-on regions have been developed based on Seto's theory [36-40]. So far we have developed an analytical model that is valid in one dimension. However in short channel field effect transistors a two dimensional analysis is necessary to adequately described the device operation. Therefore, we need to use 2D numerical device simulation to realistically study the effect of the GB, in short channel polysilicon nanowires.

2.3 Numerical Simulation of Polysilicon Devices

The trend in the semiconductor industry towards MOSFETs of ever decreasing gate lengths has increase the demand for accurate numerical device simulation technologies. As devices enter the sub-micron regime, complex 2D effects begin to determine the device behavior in the subthreshold regime, and therefore 2D device simulation is needed to provide insight and predictive analysis. The classical Drift-Diffusion (DD) model has been extensively studied for almost forty years, since Gummel *et al*. reported on the one-dimensional numerical simulation of a silicon bipolar transistor [41]. Even as the MOSFET enters the deca-

nanometer regime, where ballistic and quantum mechanical effects can play significant roles in carrier transport, DD modeling is still one of the most practical and powerful tools in FET design. With some modifications (such as the inclusion of momentum and energy balance equations) it can still provide reasonable accuracy and importantly great computational efficiency, compared to more elaborate techniques, such as practical based ensemble Monte-Carlo simulations.

In our simulation studies of the device, we use commercial simulator ATLAS [42] from SILVACO international. ATLAS uses the basic device modeling equation for DD modeling. The basic semiconductor equation begin with Poisson's equation which describes the relationship between the electrostatic potential ψ to the space charge density ρ

$$\nabla.(\varepsilon\nabla\psi) = -\rho \qquad (2.15)$$

where ε is the local permittivity.

The carrier continuity equation for both electrons and holes are defined in terms of the current densities $\overrightarrow{J_n}$, $\overrightarrow{J_p}$ and the generation and recombination rates for electrons and holes (G_n, G_p and R_n, R_p) respectively.

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla.\overrightarrow{J_n} + G_n - R_n \qquad (2.16)$$

$$\frac{\partial p}{\partial t} = \frac{1}{q}\nabla.\overrightarrow{J_p} + G_p - R_p \qquad (2.17)$$

The electron and hole current densities $\overrightarrow{J_n}$ and $\overrightarrow{J_p}$ are then expressed in terms of their respective quasi-Fermi potentials ϕ_n and ϕ_p.

$$\overrightarrow{J_n} = -q\mu_n\nabla\phi_n \qquad (2.18)$$

$$\overrightarrow{J_p} = -q\mu_p\nabla\phi_{\mathrm{p}} \qquad (2.19)$$

where μ_n and μ_p are the electron and hole mobilities respectively.

The carrier concentration are expressed in the following quasi-Boltzmann form in terms of both quasi-fermi potentials ϕ_n and ϕ_p and the intrinsic potential ψ

$$n = n_i ex\, p\left[\frac{\psi - \phi_n}{V_T}\right] \tag{2.20}$$

$$p = n_i ex\, p\left[\frac{\psi - \phi_p}{V_T}\right] \tag{2.21}$$

where V_T is the thermal voltage ($V_T = k_B T/q$) and n_i is the intrinsic carrier concentration.

2.3.1 Modeling Deep Trap Emission and Absorption with Shockley-Read-Hall Statistics

We now include the carrier trapping mechanisms, via the deep trap states at the grain boundary. The model used was originally developed for carrier emission-absorption processes from the donors and acceptors in heterojunction structures [43-44]. However it is equally applicable to silicon devices. By using the derived expressions we then modify the basic device transport equations accordingly.

We start by defining two types of trap that exchange charge with the conduction and valance bands through the emission and recombination of electrons. At the grain boundary these would exist in the forbidden energy gap as a result of incomplete or dangling bonds in the semiconductor lattice.

Firstly we define donor-like traps as positively charged when empty and neutral when filled by electron. Secondly we define acceptor-like traps to be negative when filled by an electron but otherwise neutral. Therefore traps above the Fermi-level are acceptor-like and those below are donor-like. This is illustrated along with the possible capture and emission processes in Fig 2.3.

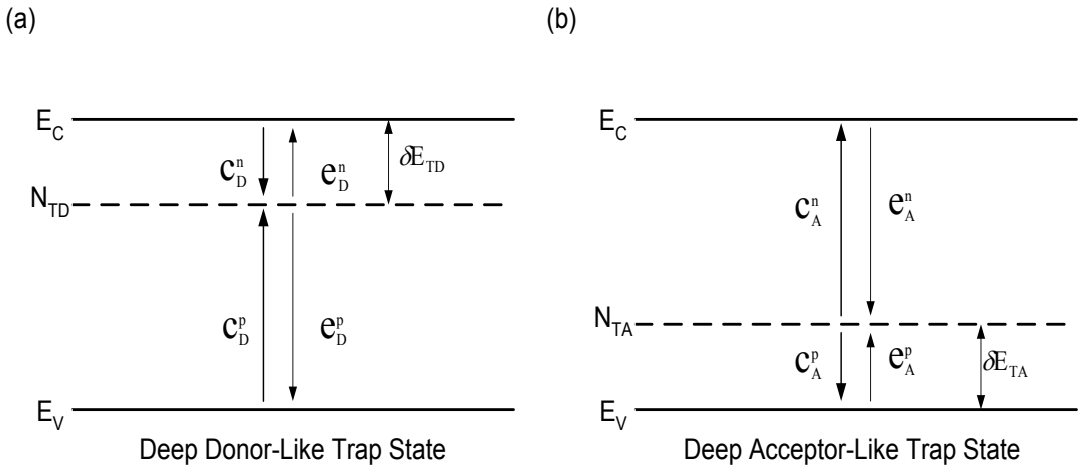

Figure 2.3: An illustration of the possible capture and emission processes from trap states deep in the energy band gap for (a) donor-like traps and (b) acceptor-like traps

The energies of donor-like (E_{TD}) and acceptor-like (E_{TA}) traps are expressed as

$$\Delta E_{TA} = \psi + E_C - \delta E_{TA} \tag{2.22}$$

$$\Delta E_{TD} = \psi + E_V - \delta E_{TD} \tag{2.23}$$

The time evolution of the density of carriers at the deep levels is given by the following rate equations [45];

$$\frac{\partial}{\partial t}(N_{TD} - N_{TD}^{+}) = C_D^n N_{TD}^{+} n - e_D^n (N_{TD} - N_{TD}^{+}) - C_D^p (N_{TD} - N_{TD}^{+}) p - e_D^p N_{TD}^{+} \tag{2.24}$$

$$\frac{\partial}{\partial t}(N_{TA} - N_{TA}^{-}) = C_A^p N_{TA}^{-} p - e_A^p (N_{TA} - N_{TA}^{-}) - C_A^n (N_{TA} - N_{TA}^{-}) n - e_A^n N_{TA}^{-} \tag{2.25}$$

where the carrier emission rates e_D^n, e_D^p, e_A^n, e_A^p are related to the carrier capture rates C_D^n, C_D^p, C_A^n, C_A^p by the relations;

$$e_D^n = C_D^n n_1^D \tag{2.26}$$

$$e_D^p = C_D^p p_1^D \tag{2.27}$$

$$e_A^n = C_A^n n_1^A \tag{2.28}$$

$$e_A^p = C_A^p p_1^A \tag{2.29}$$

where n_1^D, p_1^D, n_1^A, p_1^A are given by the following;

$$n_1^D = n_i g_D exp\left[\frac{\Delta E_{TD}}{k_B T/q}\right] \quad (2.30)$$

$$p_1^D = n_i g_D exp\left[\frac{-\Delta E_{TD}}{k_B T/q}\right] \quad (2.31)$$

$$n_1^A = n_i g_A exp\left[\frac{\Delta E_{TA}}{k_B T/q}\right] \quad (2.32)$$

$$p_1^A = n_i g_A exp\left[\frac{-\Delta E_{TA}}{k_B T/q}\right] \quad (2.33)$$

In Eq. 2.30-2.33, g_D and g_A are the degeneracies of the deep donor-like and acceptor-like trap states. A steady state-solution for the concentration of trapped charge at the GB can found from the Eq. 2.24 and 2.25. This gives us;

$$N_{TD}^+ = \frac{n_1^D/C_D^p + p/C_D^n}{(n+n_1^D)/C_D^p + (p+p_1^D)/C_D^n} N_{TD} \quad (2.34)$$

$$N_{TA}^- = \frac{n_1^A/C_A^p + p/C_A^n}{(n+n_1^A)/C_A^p + (p+p_1^A)/C_A^n} N_{TA} \quad (2.35)$$

The additional charge at the grain boundary alters the electrostatic potential by appearing as additional charge terms on the right hand side of Poisson's equation. So Eq. 2.15 then becomes;

$$\nabla.(\varepsilon\nabla\psi) = -q(N_D^+ + N_{TD}^+ - N_A^- - N_{TA}^- - n + \mathrm{p}) \quad (2.36)$$

where N_D^+ and N_A^- are the concentrations of ionized shallow donors and acceptors.

In addition, there is induced electron-hole recombination, and therefore there is a change in the current distribution through an additional generation/recombination terms on the right hand side of Eq. 2.16 and 2.17. This gives us the following expressions;

$$q\frac{\partial n}{\partial t} = \nabla.\overrightarrow{J_n} + G + R - C_D^n N_{TD}^+ n - e_D^n(N_{TD} - N_{TD}^+) - C_A^n(N_{TA} - N_{TA}^-)n - e_A^n N_{TA}^- \quad (2.37)$$

$$q\frac{\partial p}{\partial t} = \nabla.\overrightarrow{J_p} + G + R - C_A^p\,(N_{TD} - N_{TD}^+)p - e_A^p N_{TD}^+ - C_A^p N_{TA}^- n - e_A^p(N_{TA} - N_{TA}^-) \qquad (2.38)$$

where, G and R are the conventional semiconductor generation and recombination terms respectively. If we solve for the steady state (i.e. $\frac{\partial n}{\partial t} = 0$ and $\frac{\partial p}{\partial t} = 0$) then the Eq. 2.37 and 2.38 reduce to the following current continuity equations;

$$\nabla.J_n = -(G - R - R_{TD} - R_{TA}) \qquad (2.39)$$

$$\nabla.J_p = (G - R - R_{TD} - R_{TA}) \qquad (2.40)$$

where R_{TD} and R_{TA} are the recombination rates through the donor-like and acceptor-like trap states and are given by;

$$R_{TD} = \frac{np - n_1^D p_1^D}{(n + n_1^D)/C_D^p + (p + p_1^D)/C_D^n} N_{DD} \qquad (2.41)$$

$$R_{TA} = \frac{np - n_1^A p_1^A}{(n + n_1^A)/C_A^p + (p + p_1^A)/C_A^n} N_{DA} \qquad (2.42)$$

The expression given by Eq. 2.36, 2.39 and 2.40 are discretised onto a two-dimensional finite difference mesh lattice and then numerically solved in an iterative way using the standard Gummel's scheme [43,46].

2.3.2 Continuous Trap-State Density Distribution Model

So far we have assumed that the acceptor-like and donor-like trap states are mono-energetic; that is they exist at only one energy level in the forbidden gap. For a more accurate simulation, a continuum of trap states distributed across the energy band gap can be defined, using the commercial device simulator ATLAS. To do this we again modify the space charge term Q_T representing trapped charge. This is given by

$$-p = q(p - n + N_D^+ - N_A^-) + Q_T \qquad (2.43)$$

$$Q_T = q(p_T - n_T) \qquad (2.44)$$

where, N_D^+ and N_A^- are the ionized donor and acceptor concentrations respectively and p_T and n_T are the trapped hole and electron concentrations respectively.

Again we assume that the trap states consist of both donor-like and acceptor-like states, distributed across the forbidden energy gap. We can write the total density of states as

$$g(E) = g_D(E) + g_A(E) \qquad (2.45)$$

where $g_D(E)$ is the total density of donor-like trap states and $g_A(E)$ is the total density of acceptor-like trap states. Attempts to experimentally measure the continuum of trap states at the grain boundary in Polysilicon films, suggest that both, donor-like and acceptor-like states, consist of two components. Firstly, an exponential Tail distribution which intercepts the adjacent energy band at its maximum value and decays rapidly toward the centre ($g_{TA}(E)$ for acceptor and $g_{TD}(E)$ for donors). Secondly a Gaussian distribution of traps located deep in the energy gap ($g_{GA}(E)$ for acceptors and g_{GD} for donors). These terms are expressed as;

$$g_{TA}(E) = N_{TA} exp\left[\frac{E - E_C}{W_{TA}}\right] \qquad (2.46)$$

$$g_{TD}(E) = N_{TD} exp\left[\frac{E - E_C}{W_{TD}}\right] \qquad (2.47)$$

$$g_{GA}(E) = N_{GA} exp\left[-\left[\frac{E_{GA} - E}{W_{GA}}\right]^2\right] \qquad (2.48)$$

$$g_{GD}(E) = N_{GD} exp\left[-\left[\frac{E_{GD} - E}{W_{GD}}\right]^2\right] \qquad (2.49)$$

where N_{TA} and N_{TD} are the trap state densities at the point of intercept with the conduction band (acceptor-like) and valence band (donor-like) respectively and W_{TA}, W_{TD} are the characteristic decay energies, defining how rapidly the distribution decays towards the centre of the band gap. For the Gaussian type states; N_{GA} and N_{GD} are the total density of trap states, W_{GA} and W_{GD} are the characteristic decay energies defining the spread of the Gaussian and finally, E_{GA} and E_{GD} are the position of the Gaussian peaks in the energy band gap. All quantities are for acceptor-like and donor-like trap respectively as denoted in the subscript.

For clarification, the role of these quantities is illustrated by the example distribution shown in Fig. 2.4.

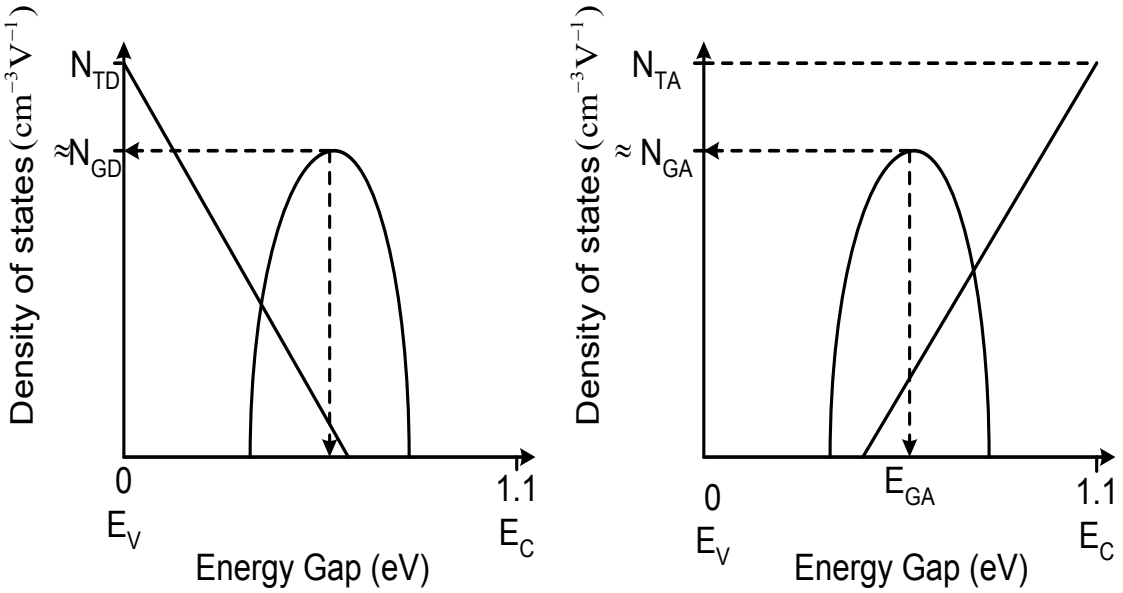

Figure 2.4: An illustration of a possible (a) acceptor-like and (b) donor-like distribution of trap states across the energy band gap and how they relate to the model parameters.

To calculate the trapped charge we perform a numerical integration of the product of the trap density and its occupation probability over the forbidden energy gap. This gives

$$n_T = \int_{E_V}^{E_C} g_A(E) f_A(E,n,p) dE \qquad (2.50)$$

$$p_T = \int_{E_V}^{E_C} g_D(E) f_D(E,n,p) dE \qquad (2.51)$$

for trapped electrons and hole respectively, where f_A and f_D are the occupation probability for acceptor-like and donor-like traps.

If we them assume that the capture cross section for Gaussian and Tail states are equal, then the occupation probabilities are then given by

$$f_A = \frac{v_n \sigma_{ae} n + v_p \sigma_{ah} p_t}{v_n \sigma_{ae} (n + n_t) + v_p \sigma_{ah} (p + p_t)} \qquad (2.52)$$

$$f_D = \frac{v_n \sigma_{de} n + v_p \sigma_{dh} p_t}{v_n \sigma_{de} (n + n_t) + v_p \sigma_{dh} (p + p_t)} \qquad (2.53)$$

Where σ_{ae}, σ_{ah} and σ_{de}, σ_{dh} are the electron and hole capture cross sections for acceptor-like and donor-like traps respectively. The effective electron and hole concentrations, n_t and p_t are defined as

$$p_t = n_i exp\left[\frac{E_i - E}{kT}\right] \tag{2.54}$$

$$n_t = n_i exp\left[\frac{E - E_i}{kT}\right] \tag{2.55}$$

where n_i, is the intrinsic carrier concentration, E is the trap energy level, E_i is the intrinsic fermi level and T is the lattice temperature.

The Shockley-Read-Hall recombination/generation rate [45, 47] per unit time is modified to include the multiple trap levels and is given by;

$$U_{n,p} = \int_{E_V}^{E_C} \left(\frac{v_n v_p \sigma_{ae} \sigma_{ah} (np - n_i^2) g_A(E)}{v_n \sigma_{ae} (n + n_t) + v_p \sigma_{ah} (p + p_t)} + \frac{v_n v_p \sigma_{de} \sigma_{dh} (np - n_i^2) g_D(E)}{v_n \sigma_{de} (n + n_t) + v_p \sigma_{dh} (p + p_t)} \right) dE \tag{2.56}$$

Chapter 3

Methodology

3.1 Device Feature and Simulation Models

The investigation of p-type polysilicon nanowire transistors were done with the help of numerical commercial simulator SILVACO [48], installed on a VLSI lab of East West University. A p-type polysilicon nanowire transistor with 10 μm channel length and 100 nm channel thickness was created on 500 nm n-type Si substrate with substrate doping density 1×10^{16} cm^{-3}. The 10 nm thickness aluminum material used as back gate (Fig. 3.1). A 500 nm thickness of nitride layer were also employed between the polysilicon and silicon layer at the back. There was 10 nm thickness layer of oxide used above on the polysilicon layer. In the polysilicon nanowire, two heavily doped regions on the two sides of the channel were employed to ensure ohmic contacts on the source/drain regions with doping density of 1×10^{20} cm^{-3}. Here, the channel doping was p-type where the channel doping density was 6×10^{16} cm^{-3}. To contact source, drain and gate the aluminum electrode was chosen with schottky barrier height of 0 eV for a perfect ohmic contact. This structure exactly matches polysilicon nanowire biosensor which was fabricated in Southampton nano fabrication center [31]. The DC electrical characteristics of these nanowires were characterized at Southampton which was used to calibrate our simulation.

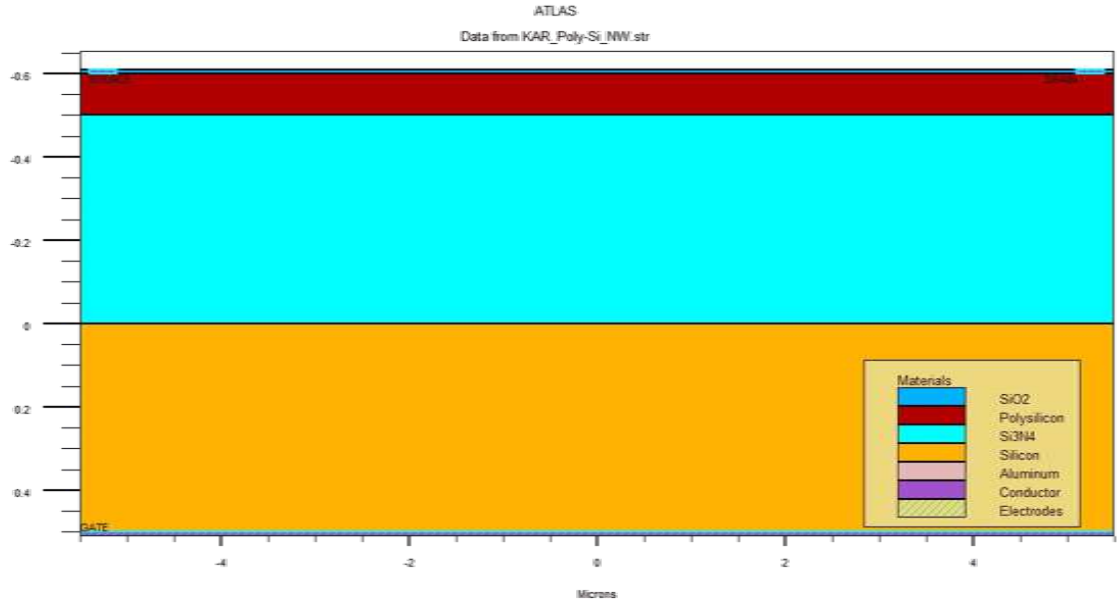

Figure 3.1: Schematic of the simulated p-type silicon nanowire transistor.

In this research work we used constant mobility model for polysilicon NWs simulation because TFT module in ATLAS is compatible with constant low field mobility model only. Use of other mobility model overwrites constant low field model and gives inaccurate results. Constant low field mobility model is independent of doping concentration, carrier densities and electric field. It does account for lattice scattering due to temperature according to:

$$\mu_{n0} = MUN\left(\frac{T_L}{300}\right)^{-TMUN} \tag{3.1}$$

$$\mu_{p0} = MUP\left(\frac{T_L}{300}\right)^{-TMUP} \tag{3.2}$$

where T is the lattice temperature. The low field mobility parameters: `MUN`, `MUP`, `TMUN` and `TMUP` can be specified in the `MOBILITY` statement with the defaults as shown in Table 3.1.

Table 3.1: Default mobility model values for polysilicon

Statement	Parameter	Defaults	Unit
MOBILITY	MUN	1000	cm^2 / V.s
MOBILITY	MUP	500	cm^2 / V.s
MOBILITY	TMUN	1.5	-
MOBILITY	TMUP	1.5	-

However we have used MUN=14 cm^2 / V.s and MUP=6 cm^2 / V.s as experimentally extracted mobility of similar polysilicon nanowires were within the range of 6 cm^2 / V.s to 12 cm^2 / V.s considering variation of polysilicon nanowire width and height after fabrication [31].

Fermi-Dirac (FERMI) carrier statistics model was used to account for certain properties of very highly doped (degenerate) materials.

In this model the probability $f(\varepsilon)$ that an available electron state with energy ε is occupied by an electron is**:**

$$f(\varepsilon) = \frac{1}{1 + exp\left(\frac{\varepsilon - E_F}{kT_L}\right)} \tag{3.3}$$

where E_F is a spatially independent reference energy known as the Fermi level and k is Boltzmann'sconstant.

In the limit that $\varepsilon - E_F >> kT_L$ Equation (3.3) can be approximated as:

$$f(\varepsilon) = exp\left(\frac{E_F - \varepsilon}{kT_L}\right) \tag{3.4}$$

Statistics based on the use of equation (3.4) are referred to as Boltzmann statistics [49][50]. The use of Boltzmann statistics instead of Fermi-Dirac statistics makes subsequent calculations much simpler. The use of Boltzmann statistics is normally justified in semiconductor device theory, but Fermi-Dirac statistics are necessary to account for certain properties of very highly doped (degenerate) materials. In ATLAS we used Fermi-Dirac statistics by specifying the parameter FERMIDIRAC on the MODEL statement.

The Shockley-Read-Hall (SRH) model was used for recombination phenomenon within the device. The carrier emission and absorption process (or Phonon transitions) occur in the presence of a trap (or defect) within the forbidden gap of the semiconductor. The theory of two steps process which was first proposed by Shockley and Read [45] and then by Hall [47]. The Shockley-Read-Hall recombination is modeled as follows:

$$R_{SRH} = \frac{pn - n_{ie}^2}{TAUPO\left[n + n_{ie}\,exp\left(\frac{ETRAP}{kT_L}\right)\right] + TAUNO\left[p + n_{ie}\,exp\left(\frac{-ETRAP}{kT_L}\right)\right]} \tag{3.5}$$

where $ETRAP$ is the difference between the trap energy level and the intrinsic Fermi level, T_L is the lattice temperature in degrees Kelvin and $TAUNO$ and $TAUPO$ are the electron and hole lifetimes. This model is activated with the SRH parameter of the MODELS statement. The electron and the hole lifetime parameters $TAUNO$ and $TAUPO$ are user definable on the MATERIAL statement. The default values for carrier lifetimes are shown in Table 3.2. Materials other than silicon will have different defaults and full descriptions of these are given in Table 3.3.

Table 3.2: Default parameters for equation 3.5

Statement	Parameter	Defaults	Units
MATERIAL	ETRAP	0	V
MATERIAL	TAUNO	1.0×10^{-7}	s
MATERIAL	TAUPO	1.0×10^{-7}	s

Table 3.3: Default parameters of polysilicon recombination parameters for equations 3.5

Material	TAUNO (s)	TAUPO (s)	NSRHN (cm^{-3})	NSRHP (cm^{-3})
Polysilicon	1.0×10^{-7}	1.0×10^{-7}	5.0×10^{16}	5.0×10^{16}

To account bandgap narrowing effects, BGN model was used. In the presence of heavy doping, greater than $10^{18}cm^{-3}$, experimental work has shown that the pn product in silicon becomes doping dependent [51]. As the doping level increases, a decrease in the bandgap separation occurs, where the conduction band is lowered by approximately the same amount as the valence band is raised. In ATLAS this is simulated by a spatially varying intrinsic concentration n_{ie} defined according to the equation 3.6:

$$n_{ie}^2 = n_i^2 \left(\frac{\Delta E_g}{kT}\right) \tag{3.6}$$

Bandgap narrowing effects in ATLAS are enabled by specifying the BGN parameter of the MODELS statement. These effects may be described by an analytic expression relating the variation in bandgap, ΔE_g to the doping concentration, N. The expression used in ATLAS is from Slotboom and de Graaf [52]:

$$\Delta E_g = BGN.E \left\{ ln\frac{N}{BGN.N} + \left[\left(ln\frac{N}{BGN.N} \right)^2 + BGN.C \right]^{\frac{1}{2}} \right\} \tag{3.7}$$

The parameters $BGN.E, BGN.N$ and $BGN.C$ may be user defined on the `MATERIAL` statement and have the defaults shown in Table 3.4.

Table 3.4: Default parameters of Slotbooms bandgap narrowing model for equation 3.7

Statement	Parameter	Defaults	Units
MATERIAL	BGN.E	9.0×10^{-3}	V
MATERIAL	BGN.N	1.0×10^{17}	cm^{-3}
MATERIAL	BGN.C	0.5	-

Polysilicon is a disorder material which contains a large number of defects states within the band gap of the material and interface. To accurately simulate the polysilicon NWs with defects in ATLAS; the continuous defect density of states (DOS) used. The defect states as a combination of exponentially decaying band Tail states and Gaussian distribution of mid gap states [53-54] shown in Fig. 3.2 which theory described in chapter 2. In our work we have used continuous defect density of states (DOS) for p-type polysilicon nanowire simulation.

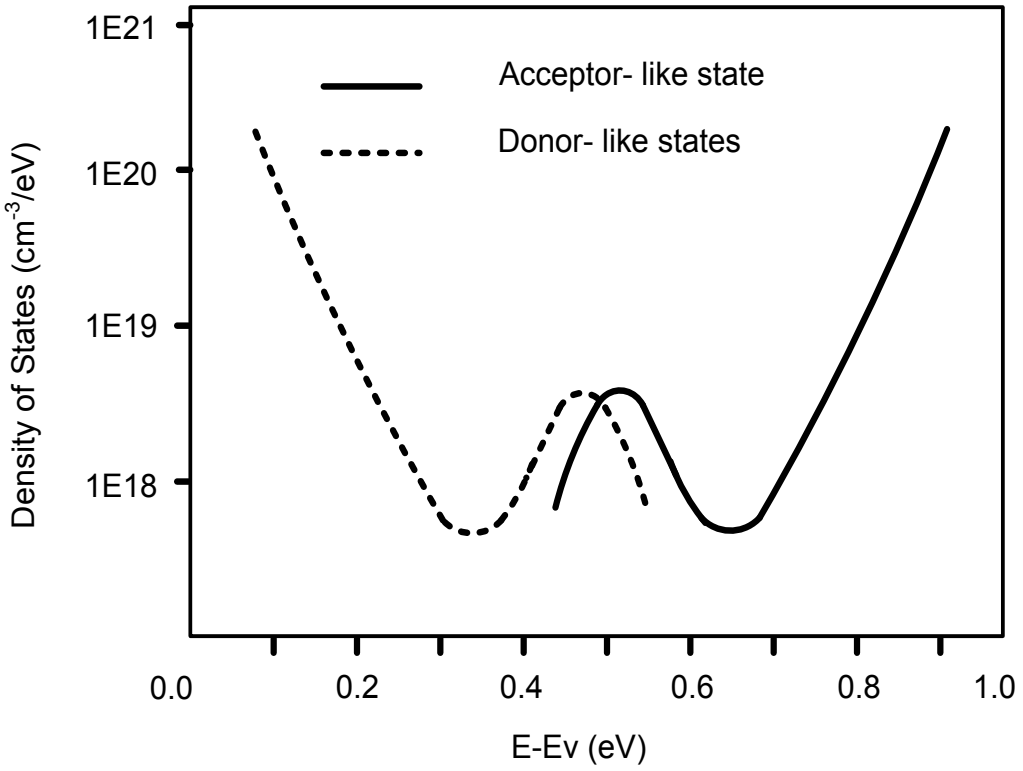

Figure 3.2: The distribution of acceptor and donor-like trap states across forbidden energy gap.

In polysilicon devices interface trap levels capture carriers, which slow down the switching speed of any device. The capture cross sections are used to define the properties of each trap. In ATLAS the INTTRAP command activates interface defect traps at discrete energy levels within the bandgap of the semiconductor shown in Fig. 3.3. We used discrete interface trap levels for simulation as it significantly reduces run time.

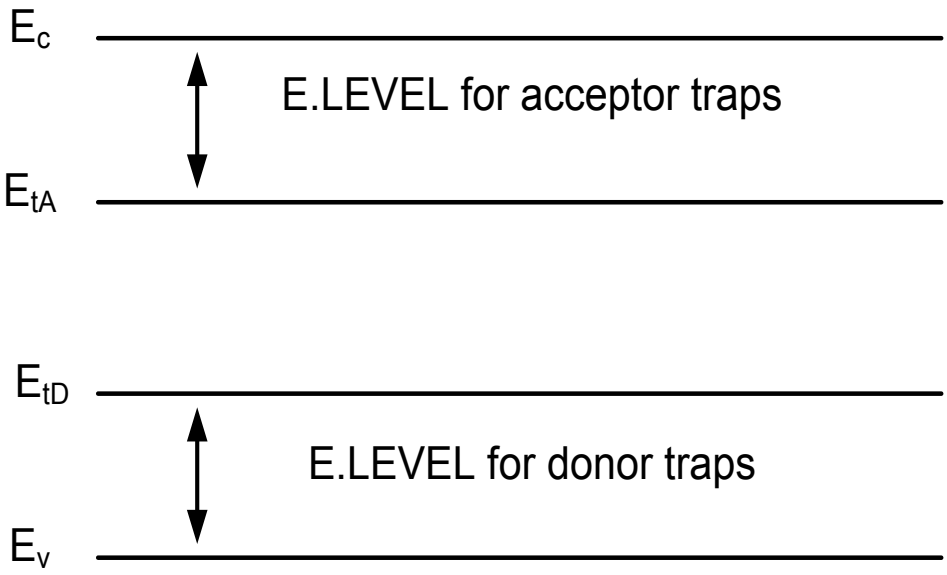

Figure 3.3: The trap energy level for acceptor and donor-like traps in reference of conduction and valance band edges.

3.2 Simulation Profile

This section is illustrating basic approaches for polysilicon NWs simulation. For device simulation SILVACO ATLAS usually faces convergence problem, hence the simulation run time are increased. For this reason, the entire first and most important task is to define the `MESH` of the device structure, because the device performance is depended on the mesh. The coarser mesh leads the fast simulation and the finer mesh leads the accuracy of the device performance. For accuracy the finer mesh are create at every interface symmetrically and the coarser mesh are created elsewhere in order to reduce simulation run time. Once the mesh is specified, every part of it must be assigned a material type. This is done with `REGION` statements. After defining the region and materials, need to specify the `ELECTRODE` to contact with semiconductor materials. Once the electrode is specified the most important parts of the device is doping profiles such as source, drain, gate and body are needed to define. When the doping profiles are specified then the device is ready to simulation. The simulation is performed to check the structure, mesh and doping profile. Once the structure, mesh and doping profile are satisfactory shown in Fig. 3.4, again the device simulation is performed with appropriate models `FERMI`, `SRH`, `BGN` which are discussed in section 3.1and numerical solving method `GUMMEL`, `NEWTON` for accuracy of device simulation. The simulation was also performed with and without interface and grain boundary defects.

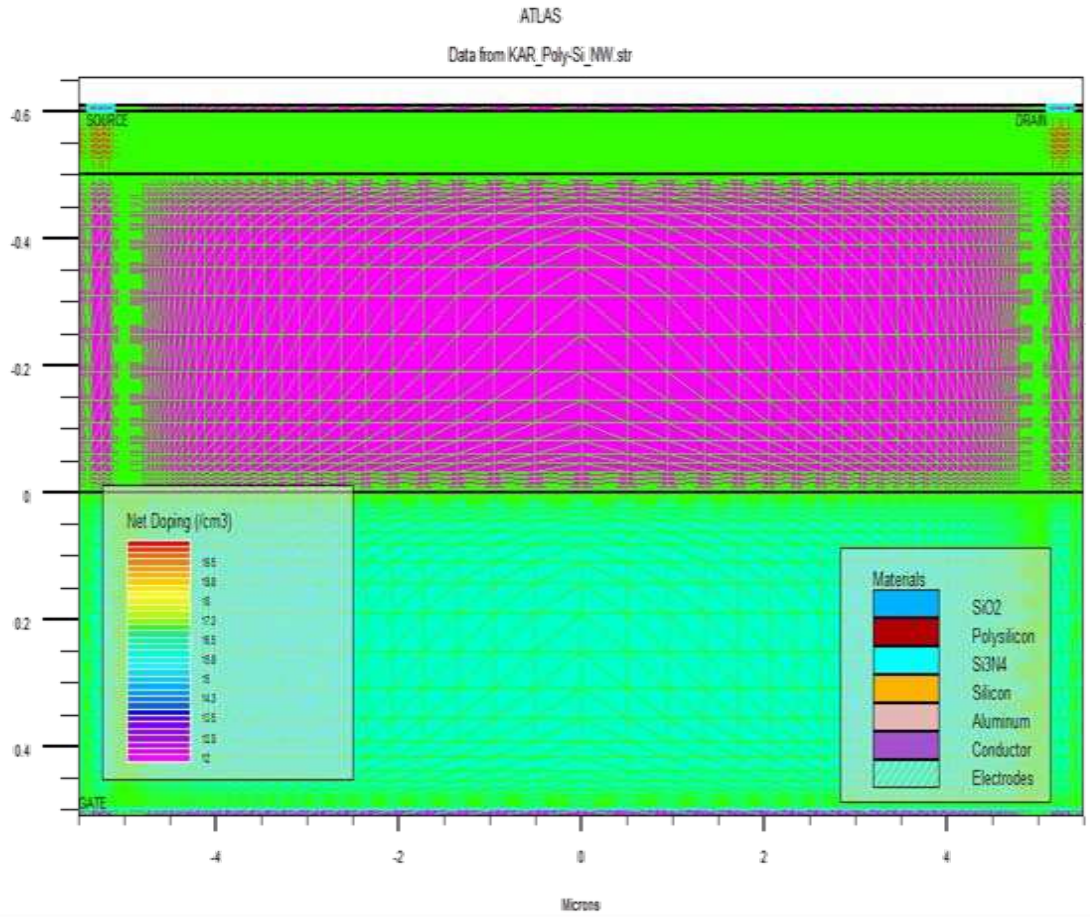

Figure 3.4: Doping profile of simulated p-type polysilicon NWs.

In ATLAS simulation a special bias point solving method was used to get the convergence because it was found that the simulation faced difficulty in solving at the initial desired bias points. Hence the initial bias was to 0.005V then 0.05V, finally set the desired bias point for simulation. For each drain biasing point the I_{DS}-V_{GS} curve was generated for V_G, varying from 5V to -20V with decrement 0.25V and for each gate biasing point the I_{DS}-V_{DS} curve was generated for V_D, varying from 0V to 20V with increment 0.25V.

Chapter 4

Results and Findings

This chapter describes the effects of different types of defects states inside the grain boundary and in the interface on the electrical characteristics of p-type polysilicon nanowire. Physical understanding of the effect of different types of grain boundary defects and interface states (donor and acceptor types) and their distribution profile on the electrical behavior of the p-type polysilicon NW is achieved by investigating each type of defects individually. This knowledge is used to calibrate experimental p-type polysilicon NWs electrical characteristics to find out the types and order of the defects that can be expected in p-type polysilicon NW biosensors if fabricated by deposition and etch technique.

4.1 Polysilicon Nanowire without Defect

The p-type polysilicon device is like a single crystal Si device without considering any defect of the material. This section shows the p-type polysilicon nanowire electrical characteristics without any defect of the material.

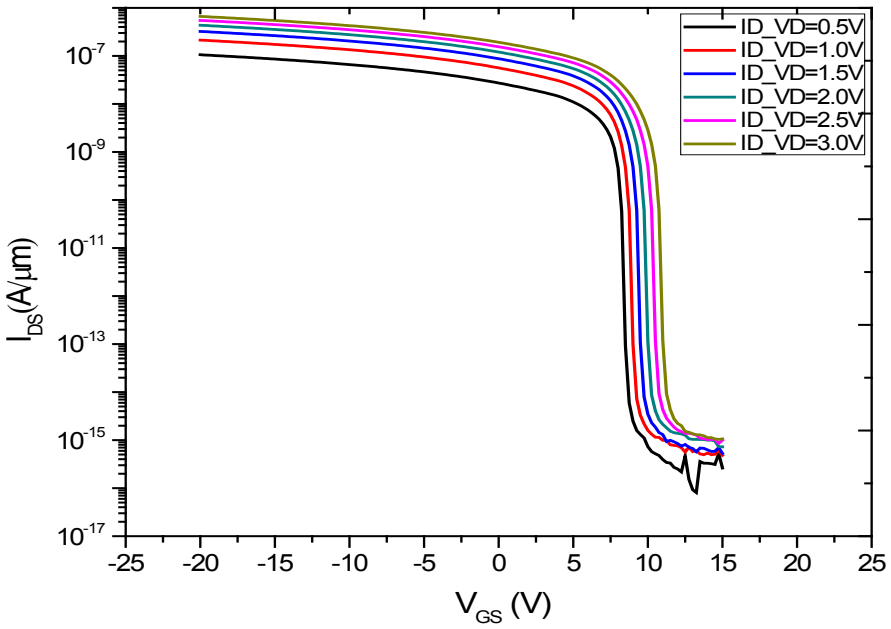

Figure 4.1: I_{DS}-V_{GS} (Log Scale) of p-type polysilicon NWs without considering material defects.

The Fig. 4.1 shows subthreshold characteristics of the p-type polysilicon NWs without any grain boundaries or interface states. The $(I_{DS} - V_{GS})$ curve illustrated for different drain voltage without considering any defects while using Si underneath the nitride as back-gate. The reason for such simulation is that the experimental data is available at this condition.

No significant degradation of subthreshold slope is observed with increasing drain bias with values of 181.72 mV/decade to 183.80 mV/decade for applied drain voltage of 0.5 V to 3.0 V. This result does not explain the results of the fabricated p-type polysilicon nanowire as reported in [31] where subthreshold slopes are around 2.3-3.0 V/decade.

To investigate the reason behind the degraded p-type polysilicon nanowire characteristics is introduced in NWs by incorporating different types of defects in simulation.

4.2 Effect of Interface Trap States

Interface states are usually created during nanowire fabrication due to the generation of surface roughness during dry etch and also due to the lattice mismatch between two material interfaces. The nanowire device under consideration has a nitride layer underneath it. In addition a 10 nm oxide layer was also grown on the top of the nanowire by oxidation for biomolecule attachment through silanization. As a result, accumulations of interface states are expected in these nanowires. However, literature supports that depending on the process conditions interface states may capture positive or negative charges. The type of charges in our considered nanowire is not known and hence, we first study the effect of both types of interface states for p-type polysilicon understanding and for calibration.

4.2.1 Effect of Acceptor-like Interface Trap States

To study the effect of acceptor-like interface states acceptor like states are created on between the polysilicon and silicon-dioxide layer also in between the polysilicon and nitride layer underneath the nanowire. The densities of acceptor-like interface states are varied from 1×10^{10} cm^{-2} to 5×10^{14} cm^{-2}. Fig. 4.2 shows p-type polysilicon nanowires subthreshold characteristics at different values of acceptor like interface states for a drain bias of 0.5V. During this measurement n-type silicon region underneath the nanowire and nitride was used as gate.

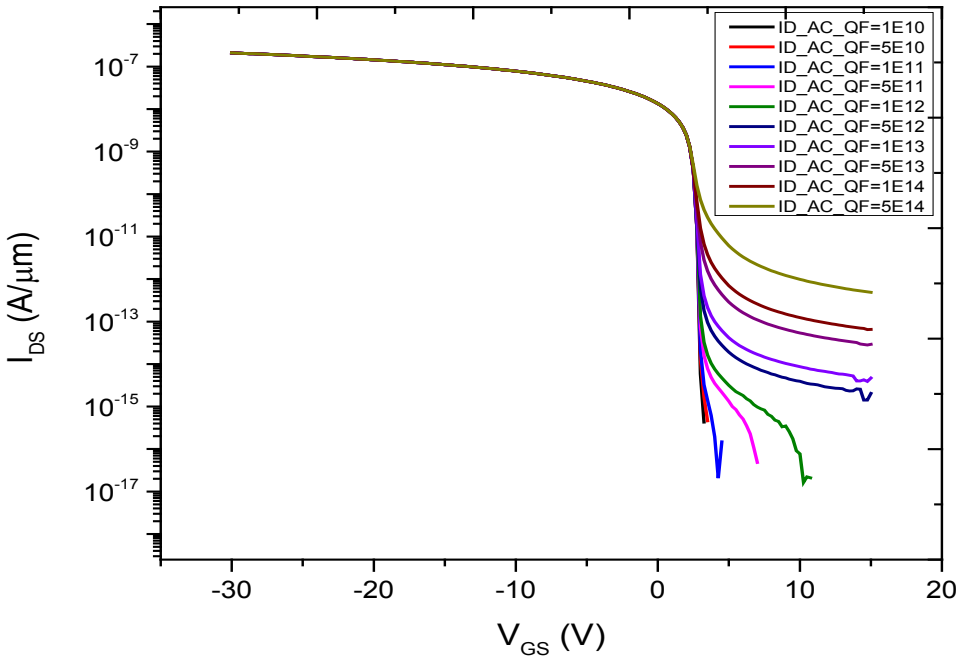

Figure 4.2: Effect of acceptor-like interface trap states.

It is observed that variation of acceptor-like interface trap density does not affect neither drive current nor the subthreshold characteristic. However, it can be seen that acceptor like interface states significantly affect the leakage current of the device. Here Leakage current is increased from 3.87×10^{-16} A/μm to 4.86×10^{-13} A/μm as the density of the acceptor state is increased from 1×10^{10} cm^{-2} to 5×10^{14} cm^{-2}.

4.2.2 Effect of Donor-like Interface Trap States

Fig. 4.3 shows p-type polysilicon nanowires subthreshold characteristics at different values of donor like interface states for a drain bias of 0.5V. During this measurement n-type silicon region underneath the nanowire and nitride was used as gate. It can be seen that the variation of donor-like interface states does not affect the leakage current at all. However, it can be seen that donor-like interface states significantly affects drive current and the subthreshold characteristic.

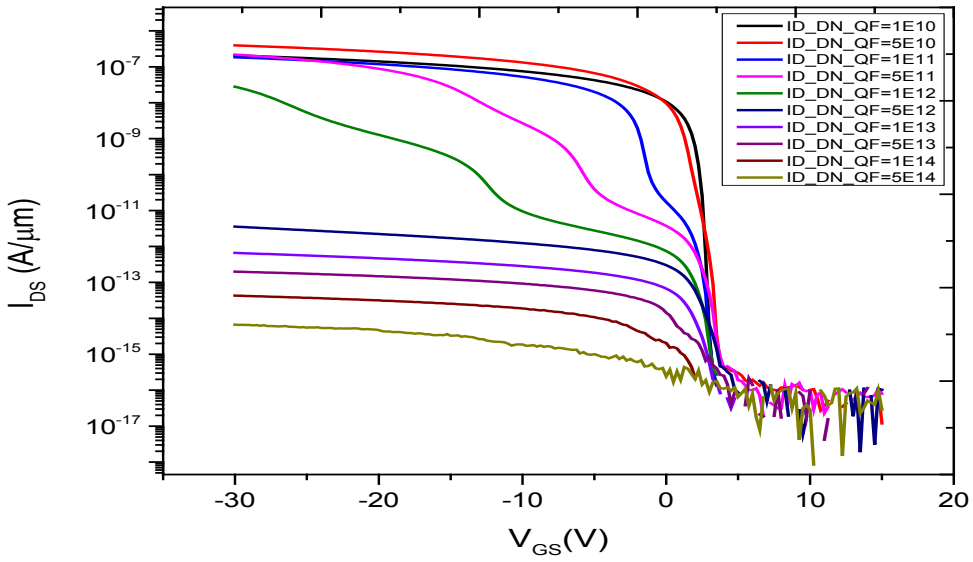

Figure 4.3: Effect of donor-like interface trap states.

The sub-threshold slope increases from 158.95 mV/decade to 3.79 V/decade for an increase of density of donor like interface states from 1×10^{10} cm^{-2} to 5×10^{14} cm^{-2}. Similarly the drive current decrease from 2.07×10^{-7} A/μm to 1.55×10^{-14} A/μm as donor density increases from 1×10^{10} cm^{-2} to 5×10^{14} cm^{-2}.

4.3 Effect of Grain Boundary / Trap States in Polysilicon Channel Region

Polysilicon materials usually composed of lots of grain boundary states. These states are accurately taken care of if a continuous defect state within the band gap of the material is considered. The continuous density of states (DOS) composed of four types of distribution. Among them two tail bands contain donor-like and acceptor-like states. There are also two deep level bands (Gaussian distribution) for acceptor-like and donor-like grain boundary trap states.

4.3.1 Effect of Tail Distributions

Fig. 4.4 shows the p-type polysilicon NWs subthreshold characteristics at different values of acceptor-like tail state distribution. During the simulation other parameters are re-mained constant such as N_{GA}=2.5×10^{16} cm^{-3}; N_{TD}=2×10^{17} $cm^{-3}eV^{-1}$; N_{GD}=2.5×10^{16} cm^{-3}. The donor-like poly-oxide and poly-nitride interface states are kept constant at 1×10^{11} cm^{-2} with two discrete energy levels at E=0.19 eV and E=0.39 eV. The N_{TA} was varied from 5×10^{12} cm^{-}

$^{3}eV^{-1}$ to 5×10^{20} $cm^{-3}eV^{-1}$ and it is seen that N_{TA} does not affect the neither subthreshold slope nor the drive current of the NW. Only a trivial change of leakage current is noticed.

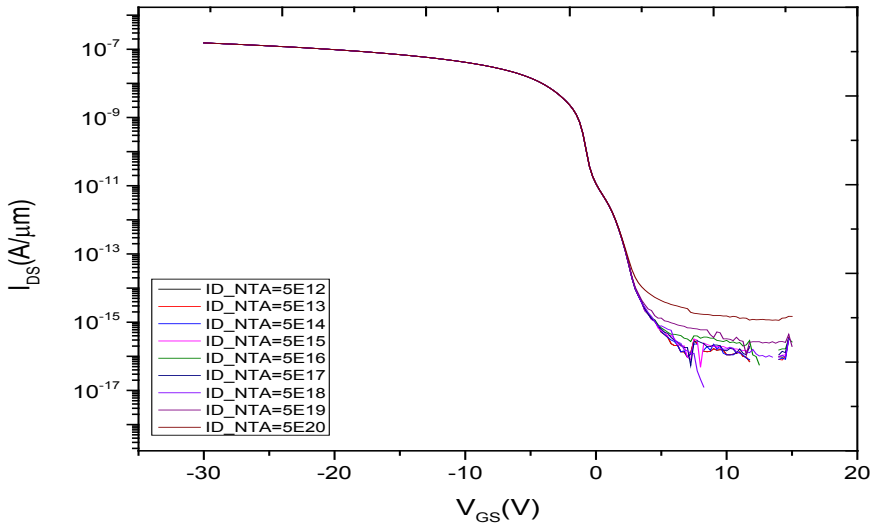

Figure 4.4: Effect of acceptor-like tail distributions (N_{TA}).

Fig. 4.5 shows the subthreshold slope characteristics of the p-type polysilicon NWs for the donor-like tail distribution. During this simulation other parameters value are remained constant such as N_{TA}=5×10^{17} $cm^{-3}eV^{-1}$; N_{GA}=2.5×10^{16} cm^{-3}; N_{GD}=2.5×10^{16} cm^{-3}. The poly-oxide and poly-nitride interface states are kept constant at 1×10^{11} cm^{-2} with two discrete energy levels at E=0.19 eV and E=0.39 eV.

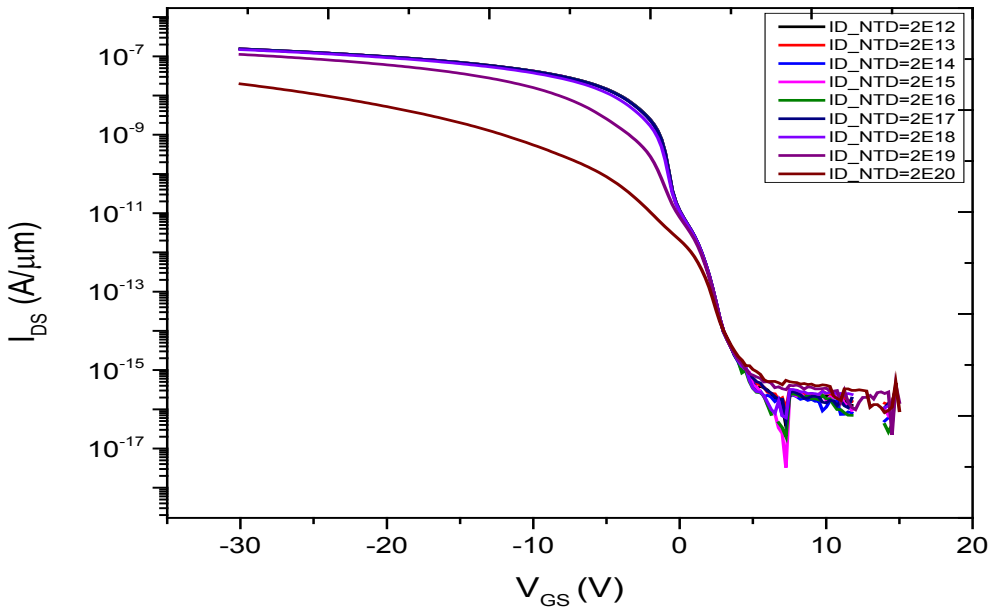

Figure 4.5: Effect of donor-like tail distributions (N_{TD}).

It can be seen that donor like tail states has effect on both subthreshold slope and drive current. Subthreshold slope increases from 0.72 V/decade to 0.94 V/decade for the increase of N_{TD} from 2×10^{12} $cm^{-3}eV^{-1}$ to 2×10^{20} $cm^{-3}eV^{-1}$ but it does not effect on leakage current. In addition drive current also decreases from 1.54×10^{-7} A/µm to 1.64×10^{-8} A/µm for the increase of N_{TD} from 2×10^{12} $cm^{-3}eV^{-1}$ to 2×10^{20} $cm^{-3}eV^{-1}$.

4.3.2 Effect of Gaussian Distributions

To understand the Gaussian like defect distribution effect, Fig. 4.6 shows the p-type polysilicon NWs subthreshold characteristics at different values of acceptor-like Gaussian state distribution. The density of acceptor-like Gaussian states (N_{GA}) was varied from 2.5×10^{12} cm^{-3} to 2.5×10^{20} cm^{-3} while keeping other parameters constant such as N_{TA}=5×10^{17} $cm^{-3}eV^{-1}$; N_{TD}=2×10^{17} $cm^{-3}eV^{-1}$; N_{GD}=2.5×10^{16} cm^{-3}. The poly-oxide and poly-nitride interface states was donor-like with the density of 1×10^{11} cm^{-2} which comprised of two discrete energy levels at E=0.19 eV and E=0.39 eV.

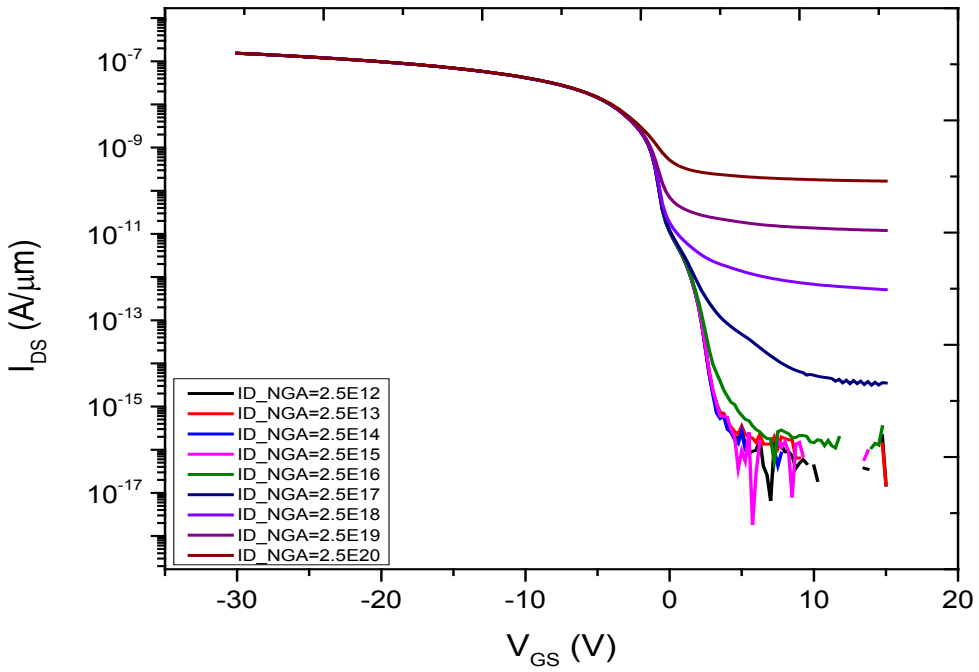

Figure 4.6: Effect of acceptor-like Gaussian distributions (N_{GA}).

It is observed that the variation of N_{GA} effects only the leakage current. For the increase of N_{GA} from 2.5×10^{12} cm^{-3} to 2.5×10^{20} cm^{-3} the leakage current increases from 1.51×10^{-17} A/µm to 5.08×10^{-13} A/µm. It does not have any effect on the subthreshold slope and the drive current.

Fig. 4.7 shows the p-type polysilicon NWs subthreshold characteristics at different values of donor-like Gaussian state distribution. The density of donor-like Gaussian states (N_{GD}) was varied from 2.5×10^{12} cm^{-3} to 2.5×10^{20} cm^{-3}. During this simulation the other parameters were kept constant with values of N_{TA}=5×10^{17} cm^{-3}eV^{-1}; N_{TD}=2×10^{17} cm^{-3}eV^{-1}; N_{GA}= 2.5×10^{16} cm^{-3}. The poly-oxide and poly-nitride interface states of donor-like with the density of 1×10^{11} cm^{-2} which comprised of two discrete energy levels at E=0.19 eV and E=0.39 eV.

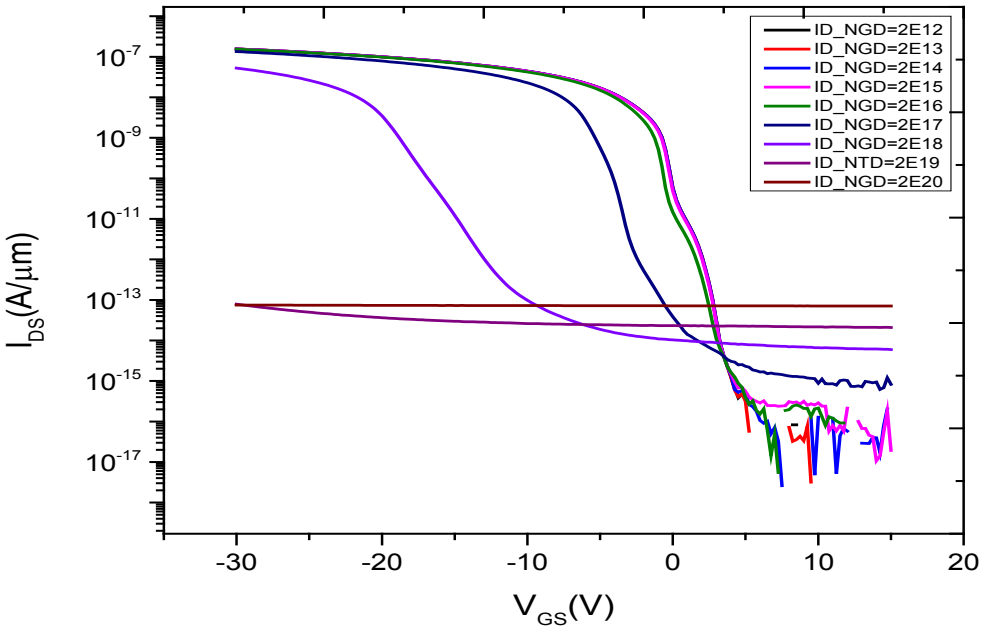

Figure 4.7: Effect of donor-like Gaussian distributions (N_{GD}).

From the Fig. 4.7, it can be seen that Gaussian like deep states has significant effects on both subthreshold slope and drive current. Subthreshold slope increases from 0.65 V/decade to 28.97 V/decade for the increase of N_{GD} from 2×10^{12} cm^{-3} to 2×10^{18} cm^{-3} but it does not affect the leakage current. In addition drive current decreases from 1.56×10^{-7} A/μm to 5.27×10^{-8} A/μm for the increase of N_{GD} from 2×10^{12} cm^{-3} to 2×10^{18} cm^{-3}. From the Fig 4.7 it is also observed that for the value of N_{GD} from 2×10^{19} cm^{-3} to 2×10^{20} cm^{-3} NW does not at all work as transistor and the drive current remain constant around 7.8×10^{-14} A/μm.

The results of Fig. 4.4 to Fig. 4.7 show that the Gaussian like donor state and acceptor state distribution in p-type polysilicon NWs has more effect on the electrical characteristics than of the p-type polysilicon NWs tail like donor state and acceptor state distribution.

4.4 Calibration with Fabricated Polysilicon Nanowire and Extraction of Defect State Distribution

Fig. 4.2 to Fig. 4.7 shows some significant effects of different types of defect states on the p-type polysilicon nanowire. Acceptor like interface trap states are found to affect the leakage current of the nanowire whereas donor like interface traps are found to affect both sub-threshold slope and drive current of nanowire.

Defects inside polysilicon also exhibited some important trend. Acceptors like tail states have no effect on the nanowire electrical characteristics whereas acceptor like Gaussian states significantly affects leakage current. However, donor like defects both in tail like and deep level Gaussian like distribution affect nanowire subthreshold characteristics and drive current. However the effects of donor like Gaussian states are more prominent then tail like states. The aforementioned effects of different types of defects on p-type polysilicon nanowires are used to calibrate nanowires fabricated by deposition and etch as reported in [31]. Throughout our simulation we have created exactly same dimension of polysilicon nanowire and substrate structure like [31]. As fabrication of nanowires were done in class 10 environment it is well known that interface trap density will be around 10^{11} cm^{-2}. In addition [31] reports that nanowires were depleted due to surface states and hence, it is reasonably expected that interface traps would be donor like for p-type polysilicon nanowires. As a result in our simulation we have used donor like interface traps. For grain boundary traps acceptor like states are varied to match leakage current level where as donor like states are varied to match sub-threshold and drive characteristics.

Fig. 4.8 compares simulated transfer characteristics of p-type polysilicon nanowires with experimental results for different drain voltage (V_D=0.5V, 1V, 1.5V and 2V) with the body doping of 6×10^{16} cm^{-3} which is similar to the experimental results [31].

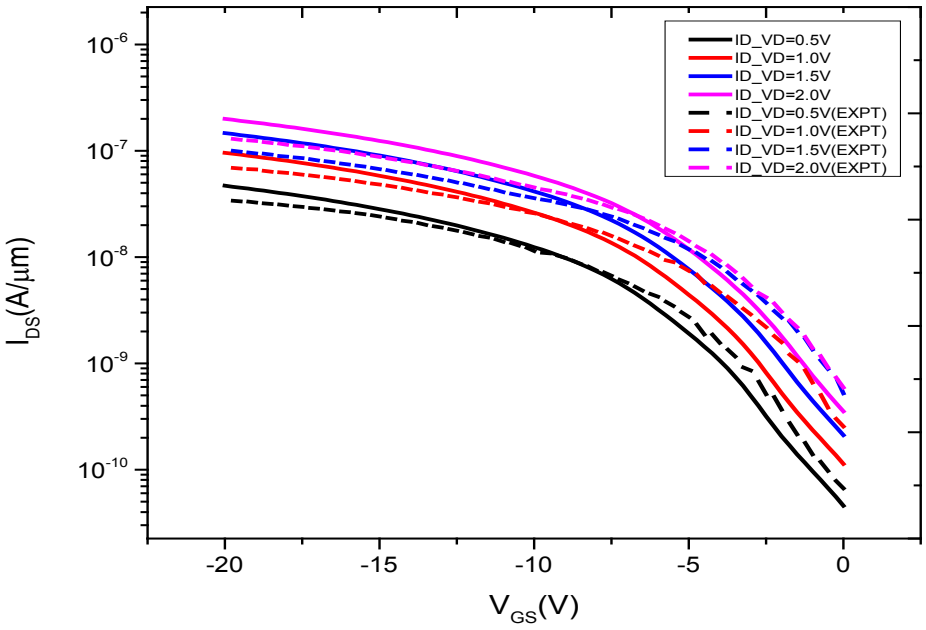

Figure 4.8: I_{DS}-V_{GS} calibration of simulation and experimental data.

It can be seen that quite a good agreement has been achieved. The drive current of the simulated polysilicon nanowire are quite similar with the fabricated polysilicon nanowire and subthreshold characteristics are also comparable with the experimental results. Such a calibration has allowed us to extract polysilicon nanowires defect states which was fabricated by deposition and etch technology.

The extracted parameters are summarized below

Table 4.1: Trap states distribution parameters and device parameters used for simulation

Device Parameter	**Symbol (Units)**	**Value**
Channel Length	$L(\mu m)$	10
Channel Width	$W(\mu m)$	0.1
Oxide Thickness	$t_{ox}(nm)$	10
Polysilicon Thickness	$t_{si}(nm)$	100
Nitride Thickness	$t_{nitride}\ (nm)$	500
Silicon Thickness (n-type)	$t_{silicon}\ (nm)$	500
Back Gate Thickness	$t_{backgate}\ (nm)$	10
Source and Drain Dopant Density	$p^{+}(cm^{-3})$	1×10^{20}
Polysilicon Doping Density	$p^{+}(cm^{-3})$	6×10^{16}

Silicon Substrate Doping Density	$n^{+}(cm^{-3})$	1×10^{16}
Capture Cross Section of Electrons in Acceptor –like States	$\sigma_{ae}(cm^{2})$	1×10^{-16}
Capture Cross Section of Holes in Acceptor –like States	$\sigma_{ah}(cm^{2})$	1×10^{-14}
Capture Cross Section of Electrons in Donor –like States	$\sigma_{de}(cm^{2})$	1×10^{-14}
Capture Cross Section of Holes in Donor –like States	$\sigma_{dh}(cm^{2})$	1×10^{-16}
Density of Acceptor-like Tail States	$N_{TA}(cm^{-3}eV^{-1})$	2×10^{19}
Density of Donor-like Tail States	$N_{TD}(cm^{-3}eV^{-1})$	1.12×10^{18}
Density of Acceptor-like Gaussian States	$N_{GA}(cm^{-3})$	1×10^{18}
Density of Donor-like Gaussian States	$N_{GD}(cm^{-3})$	1×10^{17}
Decay Energy for Acceptor-like Tail States	$W_{TA}(eV)$	0.05
Decay Energy for Donor-like Tail States	$W_{TD}(eV)$	0.05
Decay Energy for Acceptor-like Gaussian States	$W_{GA}(eV)$	0.1
Decay Energy for Donor-like Gaussian States	$W_{GD}(eV)$	0.1
Energy of Gaussian for Acceptor-like States	$E_{GA}(eV)$	0.51
Energy of Gaussian for Acceptor-like States	$E_{GD}(eV)$	0.51
Capture Cross Section of the Trap for Electrons at Interface	$\sigma_{n}(cm^{2})$	1×10^{-14}
Capture Cross Section of the Trap for Holes at Interface	$\sigma_{p}(cm^{2})$	1×10^{-16}
Density of Donor-like Interface Trap States	$D_{it}(cm^{-2})$	1.18×10^{11}
Degeneracy Factor		1

The Table 4.1 describes all and shows that the result $(I_{DS} - V_{GS})$ matches for all V_{DS} (0.5V, 1V, 1.5V and 2V) and the result $(I_{DS} - V_{DS})$ matches for all V_{GS} (0.0V, -5V, -10V, -15V and -20V).

Chapter 5

Conclusion

We have investigated the effect of interface traps and p-type polysilicon grain boundary defects on the electrical characteristics of p-type polysilicon nanowires (NWs). It has been observed that acceptor-like interface trap states affect the leakage current of the NW whereas donor-like interface traps affect both subthreshold slope and drive current of NW. Defects inside polysilicon also exhibited some important trend. Acceptor-like tail states have not affected the NW electrical characteristics whereas acceptor-like Gaussian states have significantly affected the leakage current. However, donor-like defects both in tail like and deep level Gaussian like distribution have affected NW subthreshold characteristics and drive current. These physical understandings of different types of defects are used to calibrate p-type polysilicon NW fabricated by deposition and etch technique which allowed us to extract different types of defects. This knowledge is very important to explain the p-type polysilicon NW biosensor behavior which has been recently shown to be the only viable route for mass manufacture of NW biosensors.

The extracted parameters are shown below.

Table 5.1: Trap states distribution parameters and device parameters used for simulation

Device Parameter	Symbol (Units)	Value
Channel Length	$L(\mu m)$	10
Channel Width	$W(\mu m)$	0.1
Oxide Thickness	$t_{ox}(nm)$	10
Polysilicon Thickness	$t_{si}(nm)$	100
Nitride Thickness	$t_{nitride}\ (nm)$	500
Silicon Thickness (n-type)	$t_{silicon}\ (nm)$	500
Back Gate Thickness	$t_{backgate}\ (nm)$	10
Source and Drain Dopant Density	$p^{+}(cm^{-3})$	1×10^{20}
Polysilicon Doping Density	$p^{+}(cm^{-3})$	6×10^{16}
Silicon Substrate Doping Density	$n^{+}(cm^{-3})$	1×10^{16}

Capture Cross Section of Electrons in Acceptor -like States	$\sigma_{ae}(cm^2)$	1×10^{-16}
Capture Cross Section of Holes in Acceptor -like States	$\sigma_{ah}(cm^2)$	1×10^{-14}
Capture Cross Section of Electrons in Donor -like States	$\sigma_{de}(cm^2)$	1×10^{-14}
Capture Cross Section of Holes in Donor -like States	$\sigma_{dh}(cm^2)$	1×10^{-16}
Density of Acceptor-like Tail States	$N_{TA}(cm^{-3}eV^{-1})$	2×10^{19}
Density of Donor-like Tail States	$N_{TD}(cm^{-3}eV^{-1})$	1.12×10^{18}
Density of Acceptor-like Gaussian States	$N_{GA}(cm^{-3})$	1×10^{18}
Density of Donor-like Gaussian States	$N_{GD}(cm^{-3})$	1×10^{17}
Decay Energy for Acceptor-like Tail States	$W_{TA}(eV)$	0.05
Decay Energy for Donor-like Tail States	$W_{TD}(eV)$	0.05
Decay Energy for Acceptor-like Gaussian States	$W_{GA}(eV)$	0.1
Decay Energy for Donor-like Gaussian States	$W_{GD}(eV)$	0.1
Energy of Gaussian for Acceptor-like States	$E_{GA}(eV)$	0.51
Energy of Gaussian for Acceptor-like States	$E_{GD}(eV)$	0.51
Capture Cross Section of the Trap for Electrons at Interface	$\sigma_n(cm^2)$	1×10^{-14}
Capture Cross Section of the Trap for Holes at Interface	$\sigma_p(cm^2)$	1×10^{-16}
Density of Donor-like Interface Trap States	$D_{it}(cm^{-2})$	1.18×10^{11}
Degeneracy Factor		1

It is expected that the deposition etch method based on polysilicon now may have following conclusion of p-type polysilicon traps and interface states.

Chapter 6

Limitation of the Work

- We have performed 2D simulation of p-type polysilicon NW but in reality NWs are three dimensional. For nanowire electrical characteristics to be evaluated accurately, it is somehow imperative to do 3D simulation due to the confined dimension in NWs.
- We have assumed discrete trap levels for interface states, by continuous trap states distribution would be more accurate.
- In NWs due to confined dimension lattice energy effect would be more prominent. So energy balance model might give more accurate results and extraction of the defect states.

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