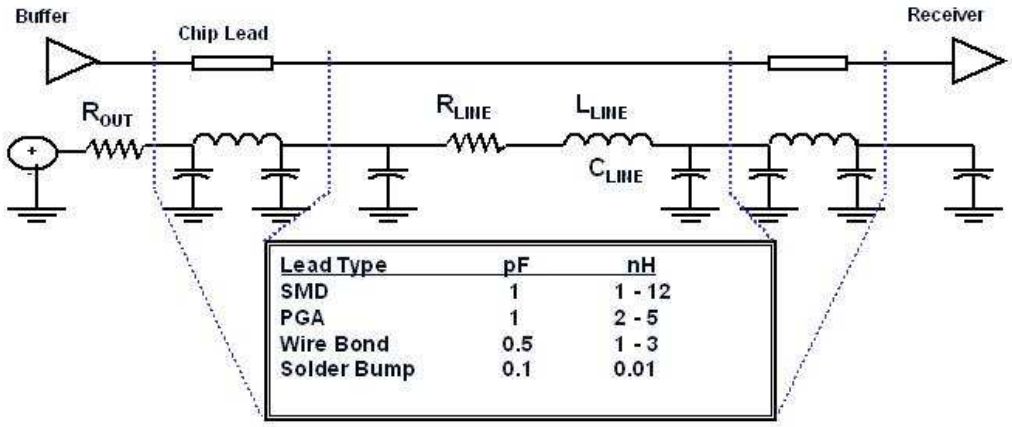
Die Improves System Design Parameters

Designers of space constrained systems face the challenge of determining how to incorporate an increasing number of functional needs into reduced spaces in a timely and cost effective manner. For many portable and small form factor applications, silicon packaging has become the major size-limiting element of the design layout. The conversion from standard semiconductor packaging to unpackaged die provides the designer a more efficient use of the limited substrate space. Use of unpackaged die also results in improved electrical performance, better signal integrity and the potential for reducing thermal resistance.

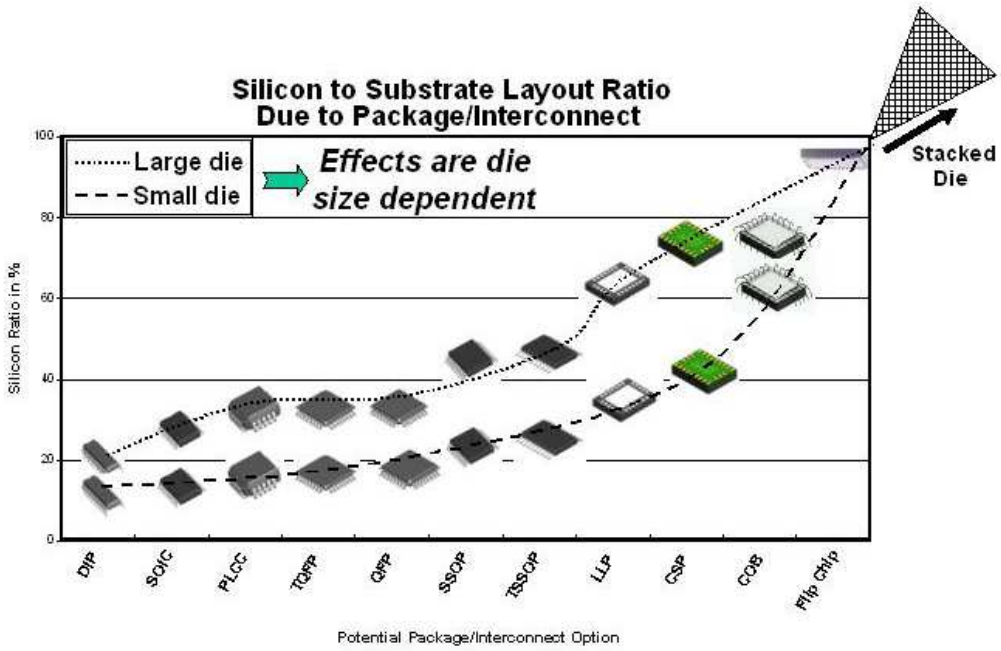
The implementation rate of unpackaged die is rapidly increasing due to both form factor needs and system performance requirements. The main application drivers in the migration from packaged die to COB or flip chip die include:

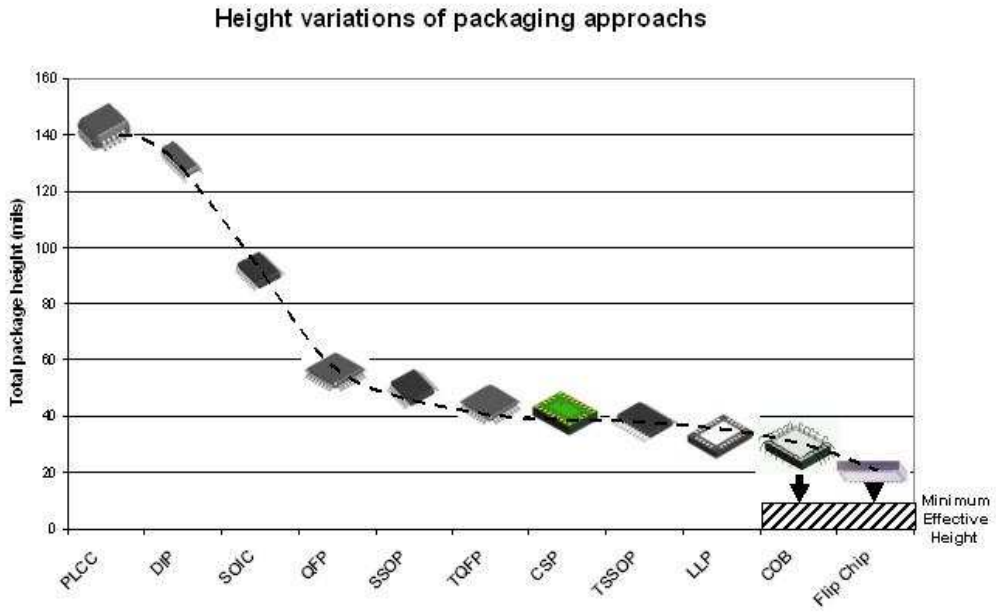
Electrical performance
The lower inductance and capacitance of the unpackaged die is important in analog, RF and power applications. Signal propagation and power/ground distributions are also improved.



Lead Type	pF	nH
SMD	1	1 - 12
PGA	1	2 - 5
Wire Bond	0.5	1 - 3
Solder Bump	0.1	0.01

Size and weight
The improvement in size and weight with the use of unpackaged die will vary based on the current package outline employed. Flip chip can reduce the functional footprint to 10% to 30% of the current space requirement. Unpackaged die can also reduce height of the overall solution.





Reliability
The reduced number of interconnects between active silicon and the substrate with die use leads to improved reliability. The typical package has three connection points vs. two for wire bonds and a single joint with flip chip.

Improved integration
Use of existing silicon functions can provide a low cost, low risk path for the designer to realize higher level integration without more extravagent system-on-chip (SOC) solutions. By taking advantage of existing unpackaged die products and high density substrates to create system-in-package (SiP) solutions reduced design time can also be achieved.

Lower cost of ownership
The lower cost of ownership with unpackaged die resuts from smaller substrate area, improved assembly, easing of system test, improved equipment utilization, reduced rework and increased product value from the size, weight and performance improvements. The cost effectiveness will be most notable in high volume applications due to the density, material and yield factors. In addition, unpackaged die costs are typically on par or lower than the package equivalent.

These unpackaged die advantages will result in higher levels of integration utilizing existing mature products leading to increased functionality per square area at reduced costs. Performance improvements will also be realized at no additional cost penalty. Integrating die for SiP solutions can provides a benefit over both standard package solutions and SOC solutions. As design to market cycle time requirements continue to shorten, unpackaged die and SiP solutions finds greater utility in meeting the manufacturer needs.