박 사 학 위 논 문

Doctoral Thesis

SAR ADC를 위한 전력효율향상 알고리즘

Power Efficient Algorithms for SAR ADCs

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Power Efficient Algorithms for SAR ADCs

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Abstract

Two asynchronous successive approximation register (SAR) analog-to-digital converters (ADCs) with power efficient algorithms are presented. For the first ADC, straightforward digital-to-analog converter (DAC) control removes the switch-back operation in traditional SAR ADC and saves DAC switching power consumption. The metastable-then-set (MTS) algorithm further reduces power consumption by finishing the conversion when the metastability is detected. Interference between two asynchronous ADCs sharing a common reference is minimized by the flag-synchronization method. For the other 10b SAR ADC, three virtually divided sub-DACs have a 0.5 LSB over-range between stages owing to additional decision phases incorporating DAC rearrange only. These redundancies make it possible to guarantee 10b linearity with a 37% speed enhancement under a 4b-accurate DAC settling condition at MSB decision. This algorithm is called as multistep addition-only digital error correction (ADEC). Two ADCs have been implemented in a CMOS 0.13μm technology and operate under 1.2V supply. At a sampling rate of 17.5MS/s and 40MS/s, the chips achieve a peak SNDR of 51.3dB and 50.6dB, respectively. The measured total power dissipation is 438μW and 550μW, and their FOMs are 79fJ/conv.step and 42fJ/conv.step.

Contents

List of Figures

List of Tables

1.Introduction

This chapter composed of two sections will introduce general SAR ADC information. In the section 1.1, trends in a SAR ADC will be described. In the last section 1.2, the operation and features of a conventional SAR ADC will be explained.

1.1 Trends in a SAR ADC

Recently, many ingenious circuit techniques assisted by high-speed deep-submicron CMOS processes have made SAR ADCs a very popular type of architecture for many applications, as those advanced techniques and technologies enhance the conversion speed

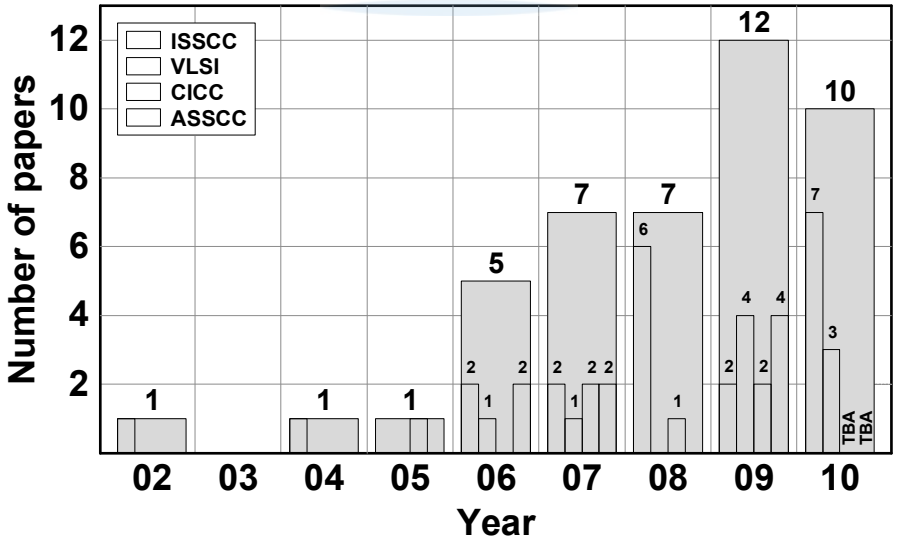


Fig. 1-1. Number of papers at major conferences held during the last 10 years

with excellent power efficiency. These reasons make SAR ADCs be chosen to many ADC designers. How many papers are published at major conferences and what trends do they show? SAR ADC papers at major conferences were surveyed to understand above-mentioned questions as shown in Fig. 1-1.

In 2002 and 2004, the authors in the Infineon presented non-binary and time-interleaving SAR ADCs. Many ADC designers who saw SAR ADC's bright future through two papers tried to research on SAR ADCs. Starting from 2006 when five papers are published, 7-12 papers are published every year. As many as six papers presented in 2008, especially, and, in this year, 2010 ten papers are already published. By now, the total 44 papers are written. Given this tendency, the outlook of a SAR ADC is very promising for the next a few years.

The all organizations writing the 11 papers at ISSCC are listed up in table 1-1. Many companies are investing in SAR ADC, and this fact says that the SAR ADC is worth the investment.

Company (11)		**University (10)**	
Infineon	3	MIT	2
IMEC	2	UC, Berkeley	1
TI	1	Twente	1
Nortel	2	Pavia	1
Analog	1	Texas, Austin	1
Toshiba	1	Carnegie Mellon	1
Fujitsu	1	UIUC	2
		National Chen -Kung	1

Table 1-1. Organization list of 11 papers at ISSCC

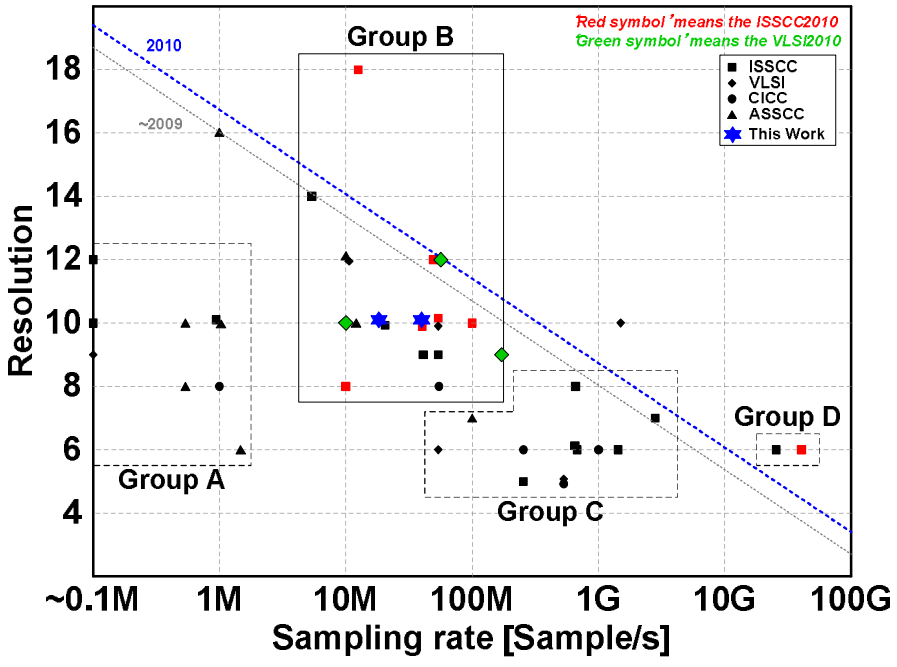


Fig. 1-2. Resolution vs. sampling rate plot about selected 44 papers

The Fig. 1-2 shows the resolution vs. sampling rate plot about recent 44 papers which can be categorized by four groups. The group A consists of applications: sensor networks and bio-medical, and the group B is made up of ADCs for video and DTV applications which can be substituted for pipeline or delta-sigma ADCs. Group C is suitable for UWB, SERDES, OFDM-based receiver, and magnetic recording. Finally, the SAR ADCs in Group D are used for optical communications. The research on group B of the four groups is the liveliest, whose direction will be high resolution 12b SAR ADC. The dashed gray diagonal line indicates the state-of-the-art universal measurement of ADC performances (P), as written in Eq. 1-1, about papers published 2009 before, and the dashed blue one indicates the 'P' about papers published in 2010. [99.JSAIC.Walden]

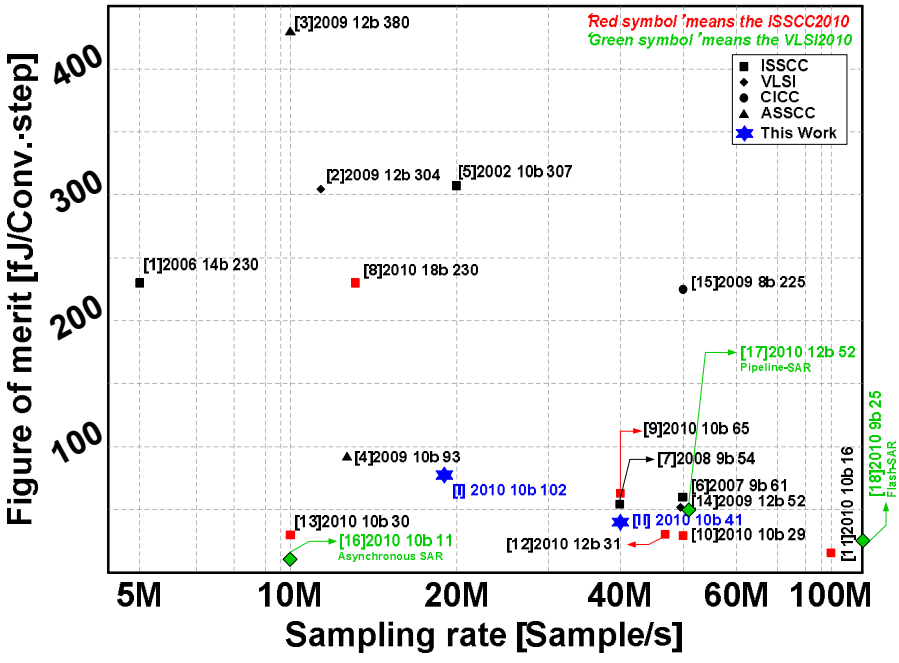


Fig. 1-3. FOMs about ADCs of group B

$$P=2^{ENOB}\cdot f_S \qquad \text{(Eq. 1-1)}$$

Exceeding the blue 'P' line, several ADCs are not a pure SAR, but a hybrid-architecture which has more than 2 A/D conversion algorithm to compensate the drawbacks of a conventional SAR ADC, and many researchers are studying on the research about fusion architectures such as a pipelining ADC of SAR ADC and a time-interleaving SAR ADC.

The FOM (figure-of-merit) formula is written using P including power consumption as Eq. 1-1. The FOMs are calculated for all papers in the group B, and the results are shown in Fig. 1-3. FOMs of the total 18 papers are recorded below 400fJ/conv.step and 12 ADCs of them have the FOM below 100fJ/conv.step.

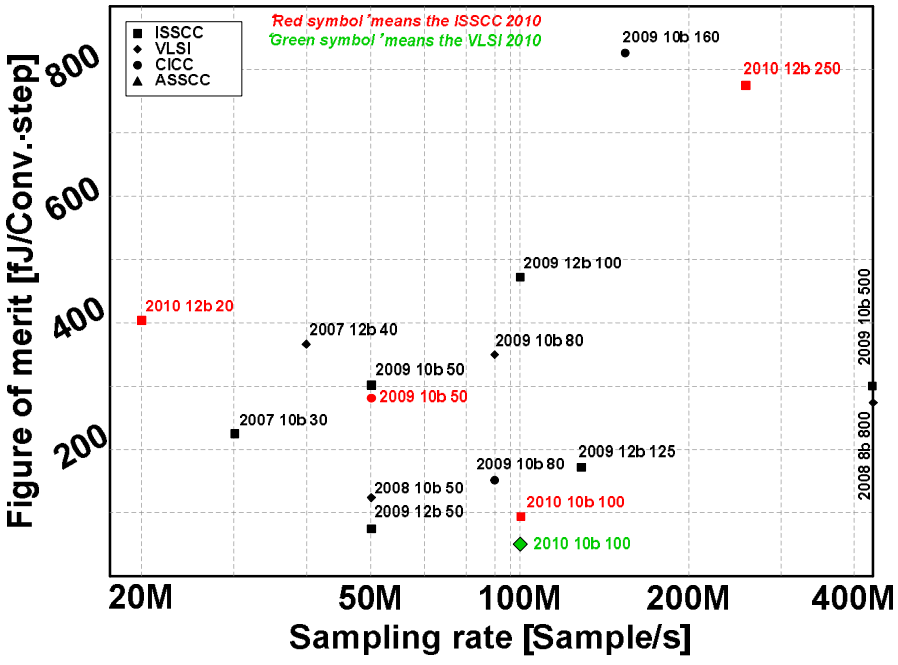


Fig. 1-4. FOMs about recent pipeline ADCs

$$FOM=\frac{Power}{2^{ENOB}\cdot\min(f_S,\,2\cdot f_{ERBW})} \qquad \text{(Eq. 1-2)}$$

To compare FOMs of SAR ADCs with those of pipeline ADCs, recent 18 pipeline ADC papers are selected according to speed and resolution: 10 ~ 500MS/s and 8 ~ 12b. Most FOMs are higher than 100fJ/conv.step as shown in Fig. 1-4. However, the 12b 100MS/s ZCBC pipeline ADC at the VLSI2010 has the state-of-the-art FOM (52fJ/conv.step). In the Fig. 1-5, the FOMs of SAR and pipeline ADCs are plotted at once. Most red symbols are distributed at a relatively low FOM and sampling speed.

Although it is true that SAR algorithm was only considered slow but efficient in the 1990's and early 2000's, nowadays most SAR ADCs surveyed are designed between 1 and

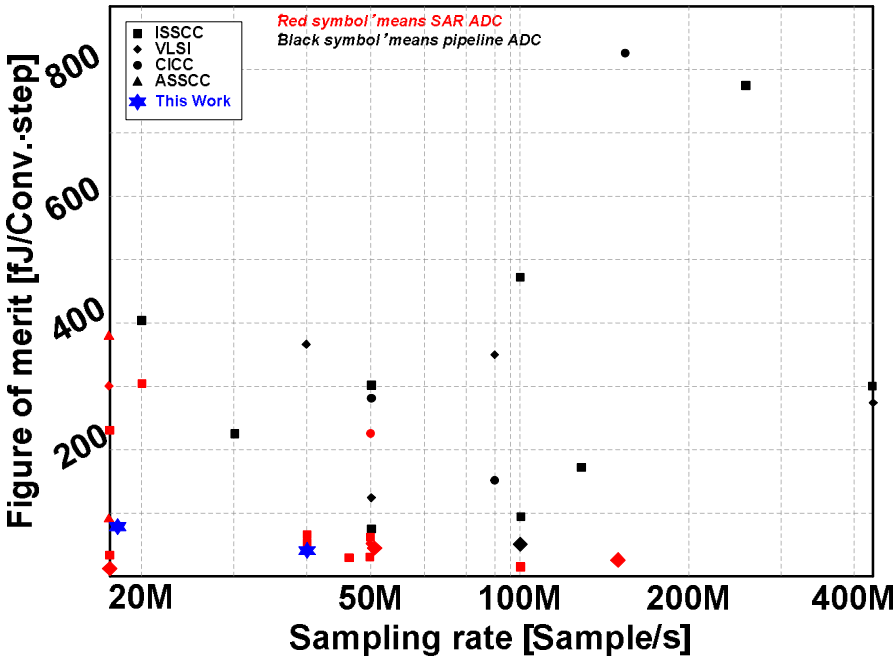


Fig. 1-5. Comparison FOMs of SAR ADCs with those of pipeline ADCs

100MS/s and even up to 40GS/s. These moderate sampling speed and power efficiency shown in FOMs are the reasons why a SAR ADC is attractive.

List of surveyed pipeline ADCs
[1] A 16b 250MS/s IF-Sampling Pipelined A/D Converter with Background Calibration, ISSCC2010
[2] A 10b 100MS/s 4.5mW Pipelined ADC with a Time Sharing Technique, ISSCC2010
[3] A 1.4V Signal Swing Hybrid CLS-Opamp/ZCBC Pipelined ADC Using a 300mV Output Swing Opamp, ISSCC2010
[4] A 130mW 100MSPS Pipelined ADC with 69dB SNDR Enabled by Digital Harmonic Distortion Correction, ISSCC2009
[5] A 50MSPS 9.9mW Pipelined ADC with 58dB SNDR in 0.18μm CMOS Using Capacitive Charge-Pumps, ISSCC2009
[6] A 12b 50MSPS Fully Differential Zero-Crossing-Based ADC Without CMFB, ISSCC2009
[7] A 10b 500MHz 55mW CMOS ADC, ISSCC2009
[8] A 16b 125MSPS 385mW 78.7dB SNR CMOS Pipeline ADC, ISSCC2009
[9] A 4.7mW 0.32mm^2 10b 30MSPS Pipelined ADC Without a Front-End SH in 90nm CMOS, ISSCC2007
[10] Comparator-based switched-capacitor circuits for scaled CMOS technologies, ISSCC2006
[11] A dual-channel 10b 80MSPS pipeline ADC with 0.16mm^2 area in 65nm CMOS, VLSI2009
[12] A 1.2V 30mW 8b 800MSPS time-interleaved ADC in 65nm CMOS, VLSI2008
[13] A 9.4-bit, 50-MSPS, 1.44-mW pipelined ADC using dynamic residue amplification, VLSI2008
[14] A 90nm CMOS 0.28mm^2 1V 12b 40MSPS ADC with 0.39pJ Conversion-Step, VLSI2007
[15] A 9.43-ENOB 160MSPS 1.2V 65nm CMOS ADC based on multi-stage amplifiers, CICC2009
[16] A 10b 50MSPS opamp-sharing pipeline AD with current-reuse OTAs, CICC2009
[17] A 10mW 9.7ENOB 80MSPS pipeline ADC in 65nm CMOS process without any special mask requirement and with single 1.3V supply, CICC2009
[18] A Zero-Crossing Based 12b 100MS/s Pipelined ADC with Decision Boundary Gap Estimation Calibration, VLSI2010

Table 1-2. Paper list of recent pipeline ADCs used for calculating a FOM

1.2 Conventional SAR ADC

1.2.1 Operation

This section will describe the operation of SAR ADC showing the DAC switching status every phases. A block diagram of a SAR ADC is shown in Fig. 1-6. Here are the main blocks such as capacitor DAC with built-in S/H function, SAR logics (switching logics and SAR controller), and comparator.

From Fig. 1-7 to Fig. 1-11, the operation of a 4b conventional SAR ADC which has the full binary weighted capacitor DAC is illustrated in detail.

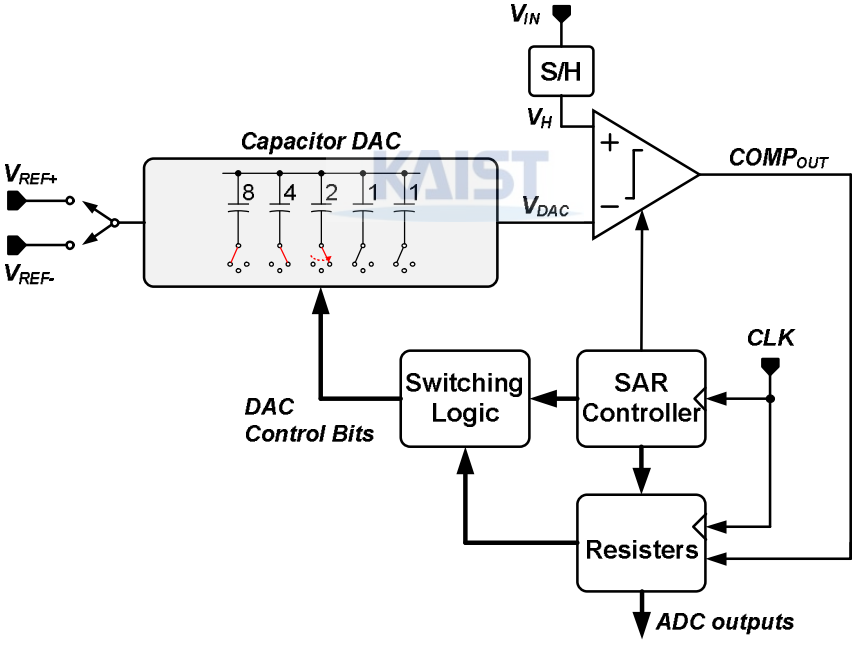


Fig. 1-6. Block diagram of a conventional SAR ADC

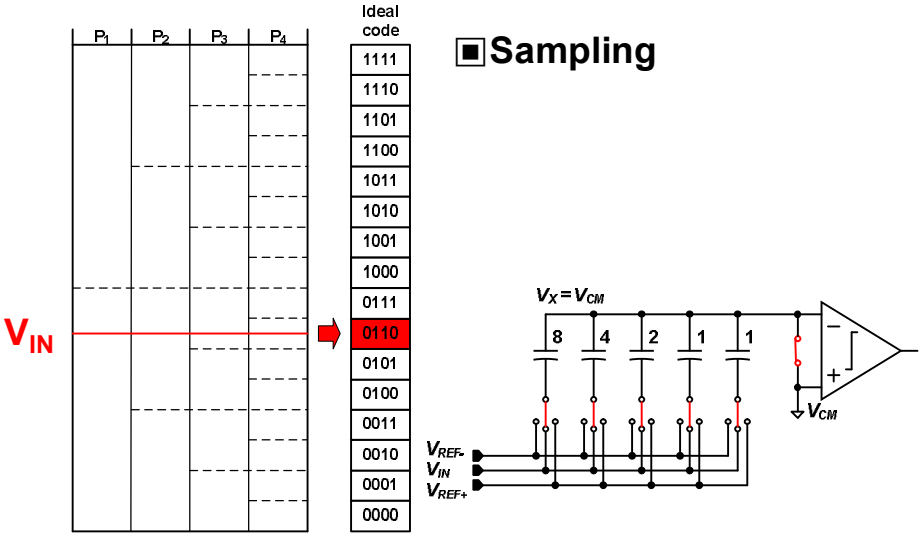


Fig. 1-7. Operation: sampling

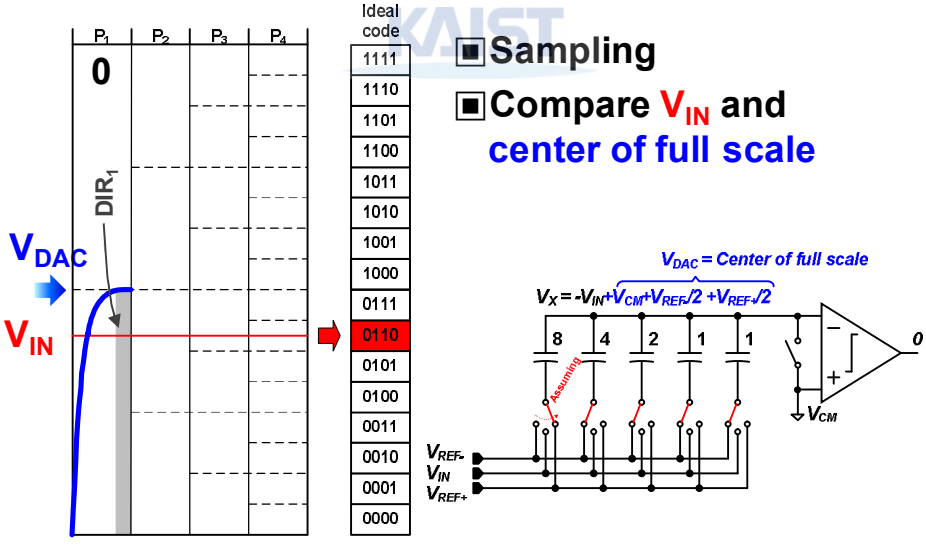


Fig. 1-8. Operation: MSB comparison

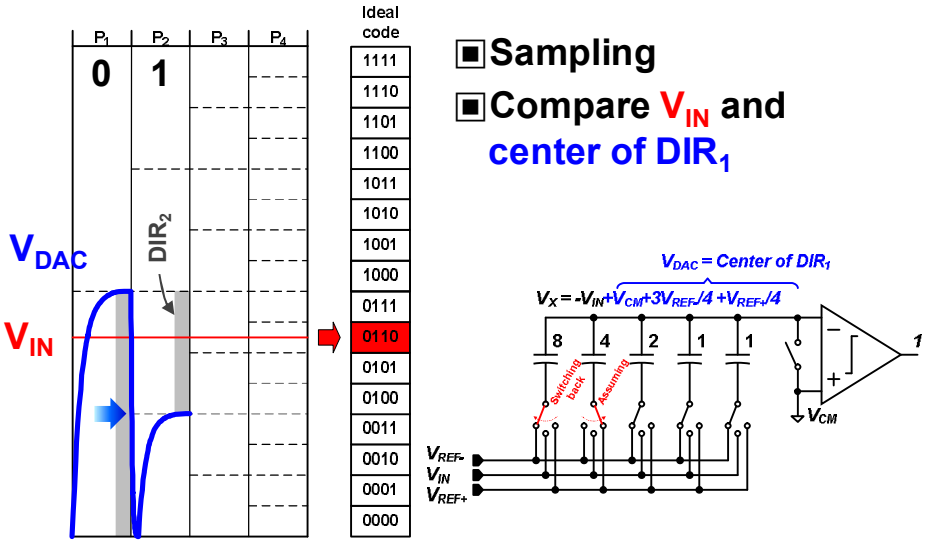


Fig. 1-9. Operation: MSB-1 comparison

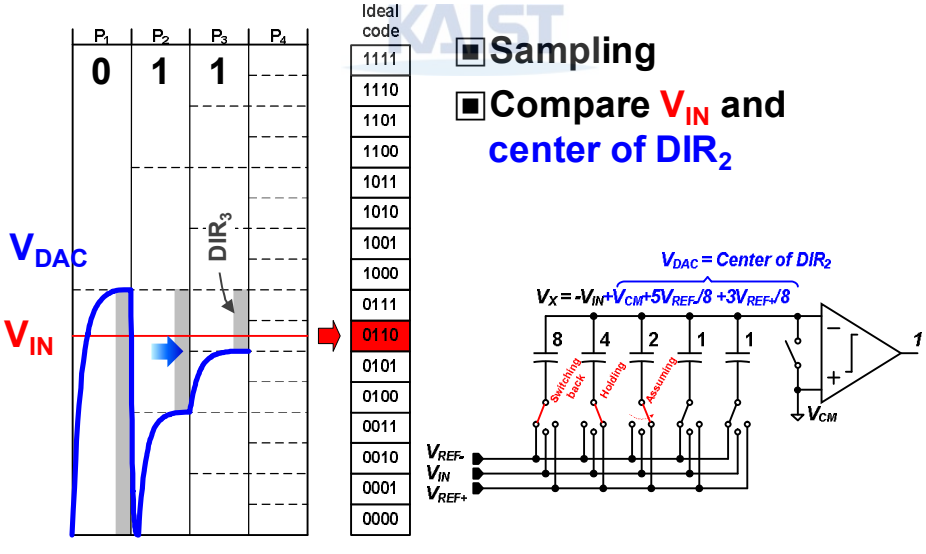


Fig. 1-10. Operation: LSB+1 comparison

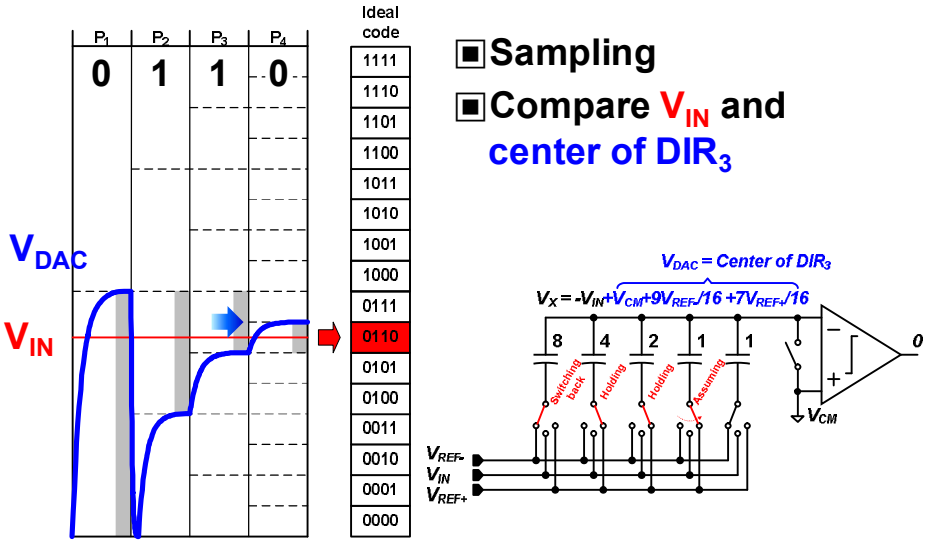


Fig. 1-11. Operation: LSB comparison

Basically, SAR conversion algorithm requires two phases. In sampling phase as shown in Fig. 1-7, the top plates of the capacitor array are connected to the V_{CM}, while all the bottom plates are done to the input analog signal. The top sampling switch is turned off and all the bottom plates are connected to the V_{REF-} when the operation of ADCs is changed from the sampling phase to the hold/conversion phase. The top plate voltage (V_X) will be equal to the V_{CM}-V_{IN}+V_{REF-}. In the conversion process, the bottom plates of the capacitors are switched to the V_{REF+} step by step starting from the largest capacitor. After the first switching as shown in Fig. 1-8, if the differential input of comparator [V_{CM}-Vx = V_{IN}-(V_{REF+}+V_{REF-})/2] is negative, then the bottom plate of the largest MSB capacitor (8C) that is switched to V_{REF+} is switched back to the V_{REF}-. It is because V_X is larger than V_{IN}, and, in other words, V_{IN} is larger than the center of input full scale. Therefore, it is natural of MSB capacitor to be switched back to drop the V_X level since a SAR ADC is a discrete

time negative feedback system. The corresponding bit in the SAR register is set to 0. Otherwise, the bottom plate of the 8C is left to V_{REF+} and the corresponding bit in the SAR register is set to 1. By the MSB decision, the first determined input range (DIR_1) is ranged from 0 to V_{CM}. The following 3 comparisons are described in Fig. 1-9~11. After all the capacitors are switched, the V_X approaches V_{CM}, as if two input nodes of the comparator are summing nodes of an opamp. As you can see, DIRs at each step are reduced by half and V_{DAC} always goes to the center of the DIR defined at previous phase. This is the binary searching algorithm. The result in the SAR register at the end of the successive approximation (SA) conversion process is the digital output which is always indicated by the last DIR.

There are two comments: The one is that a conventional SAR ADC always has assuming phases and DAC switching status follows what the corresponding output of comparator is, and the other is that the differential input of comparator (V_{CM}-Vx) can be always expressed as V_{IN}-V_{DAC} regardless of switching method and common mode voltage of a comparator. V_{DAC} is the output of the capacitor DAC.

1.2.2 Features

As previously stated, a SAR ADC is a very popular architecture due to its faster conversion speed and excellent power efficiency. Nevertheless, there are several drawbacks and all of them should be deeply understood for right ADC architecture selection.

Let's see the Fig. 1-12~3. This shows the timing difference of SAR and pipeline ADC. A pipeline ADC is possible to sample the input signal every rising edges, while a SAR ADC

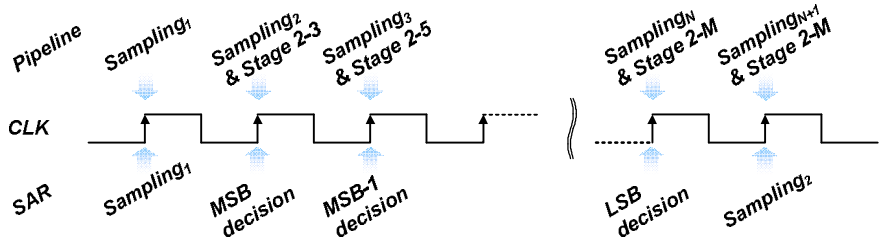


Fig. 1-12. Timing diagram of SAR and pipeline ADC

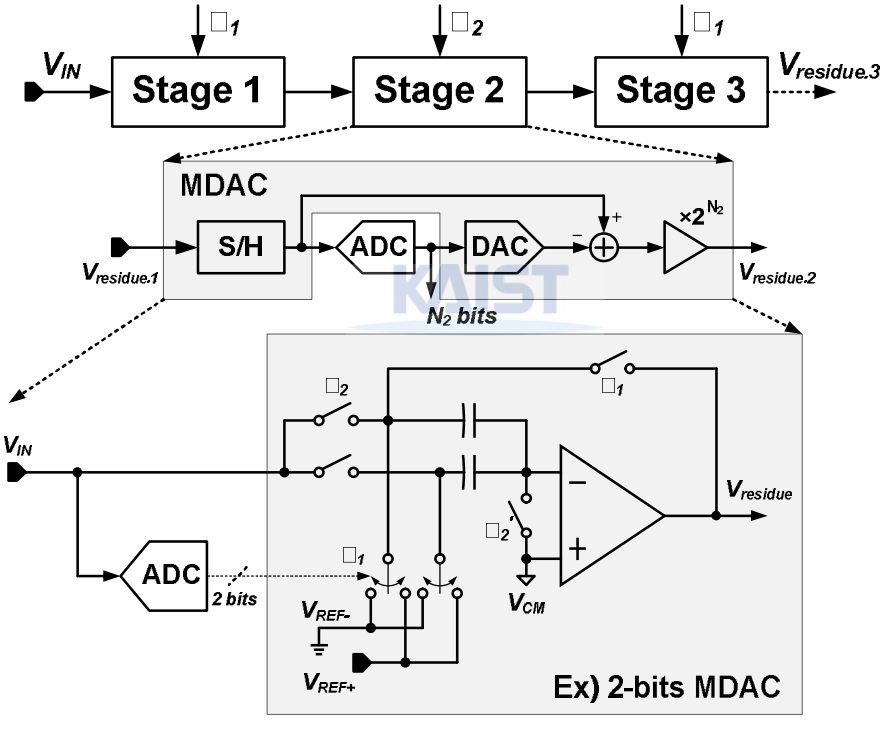


Fig. 1-13. Block diagram of pipeline ADC with 1.5b/stage.

with 1b ADC, a comparator, has to resolve the input of a comparator phase by phase after input sampling. This indicates that a pipeline ADC has the same sampling speed with

system CLK (f_{CLK}), but the sampling rate of a SAR ADC will be f_{CLK}/(resolution+1) usually. The term '+1' of the denominator means one CLK cycle for the input sampling. This remains as the fundamental speed bottleneck in a SAR ADC. Looking at the above timing difference from a different viewpoint, a SAR ADC requires the high frequency CLK driver to have the same sampling speed with pipeline ADC. In this case with the same sampling speed, the real input sampling and DAC settling time of a SAR ADC are very much shorter than those of a pipeline ADC.

The other drawback of a SAR ADC is the size of sampling capacitors driven by input driver or variable gain amplifier (VGA). If an N-bit binary weighted capacitor DAC is used for a SAR ADC, input sampling capacitor will be $2^N C_{min}$. For example, if an available minimum capacitor (C_{min}) is 30fF and the resolution of a SAR ADC is 10b, total sampling capacitance will be about 30pF. This value certainly will give overload the driver of a SAR ADC and more power will be consumed.

To sum up, designers must consider short sampling time, short DAC settling time, large sampling capacitor, and inherent slow SAR algorithm.

2.General Design Issues

This chapter will introduce general design issues of a SAR ADC. In section 2.1, the structures will be described along with kT/C and matching requirement. Section 2.2 will explain sampling method and bootstrapped switches. Section 2.3 will discuss a comparator. In the last section 2.4 and 2.5, synchronous and asynchronous controller, and SAR logics will be described.

2.1 Digital-to-Analog Converter

A DAC which generates analog voltage compared with the sampled input V_{IN}, is one of the most important sub-blocks. The static linearity performance of a SAR ADC is dominantly decided by this block. A capacitor-based-DAC (CDAC) is much more popular because a resistor-based-DAC (RDAC) consumes static current, though a RDAC is sometimes adopted to calibrate the mismatch of a CDAC.

2.1.1 Structure

DACs have many names according to the criteria for its classification: radix, grouping method of DAC elements, kinds of DAC elements and hybrid. If the criterion is the radix, DACs are classified as binary or non-binary, if it is the grouping method of DAC elements, DACs are done by binary controlled DAC or thermometer controlled DAC, if it is the kinds of DAC elements, DACs are categorized by CDAC or RDAC, and finally if it is

hybrid, DACs are grouped as ‘R and R’-based-DAC, ‘C and R’-based-DAC, or ‘C and C’-based-DAC. The most commonly used four DAC structures are shown from Fig. 2-1 to Fig. 2-4 about 4b resolution.

2.1.1.1 Binary weighted capacitor DAC (BWC DAC)

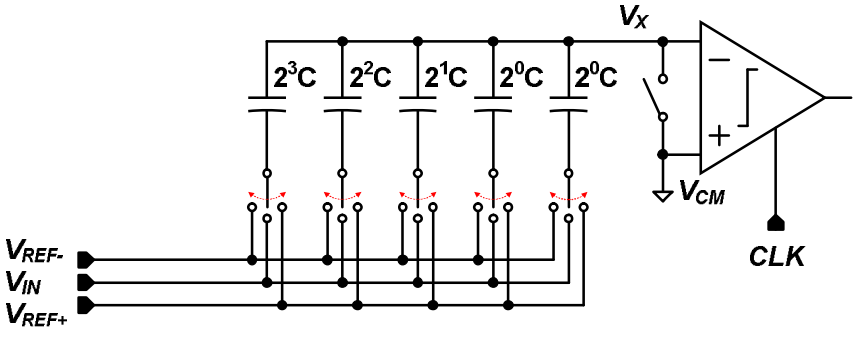


Fig. 2-1. Structure of a BWC DAC.

Fig. 2-1 shows the most basic BWC DAC structure. During A/D conversion, V_X is calculated by the charge conservation law, because charges at the output node of the DAC are frozen. The BWC DAC has next features: less number of switches and logics, but it has relatively large DNL peak. This point will be discussed in later section 2.1.2.2 in detail. The total capacitance is defined as 2^NC.

2.1.1.2 Non-binary weighted capacitor DAC (NWC DAC)

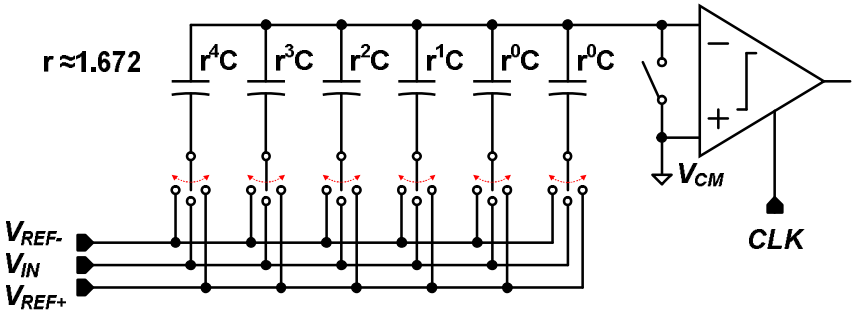


Fig. 2-2. Structure of a sub-radix NWC DAC

Fig. 2-2 shows the example of a NWC DAC structure. V_X is calculated by the same manner as mentioned above. This DAC must have more than 1 or 2 capacitor elements, too, as the sub-radix DAC requires more than 1 or 2 phases to get a proper digital output. This is the concept of the redundancy, and if an ADC obtains 4b ENOB through 5 times A/D conversions, the radix (r) is given by following Eq. 2-1.

$$\frac{r^5-1}{r-1}=2^4-1 \qquad \text{(Eq. 2-1)}$$

This equation comes from the fact that the total capacitance of a BWC DAC is the same with that of a NWC DAC. Frankly speaking, the NWC DAC was not practical due to the non-integer capacitor ratio; however, some designers have tried to overcome the capacitor mismatch problem by applying the LMS algorithm [06.ISSCC.Chen, 09.ISSCC.Wenbo, 10.ISSCC.Wenbo]. This NWC DAC results in a reduction in DAC settling time, even though sacrificing conversion time due to the additional extra comparison cycle(s).

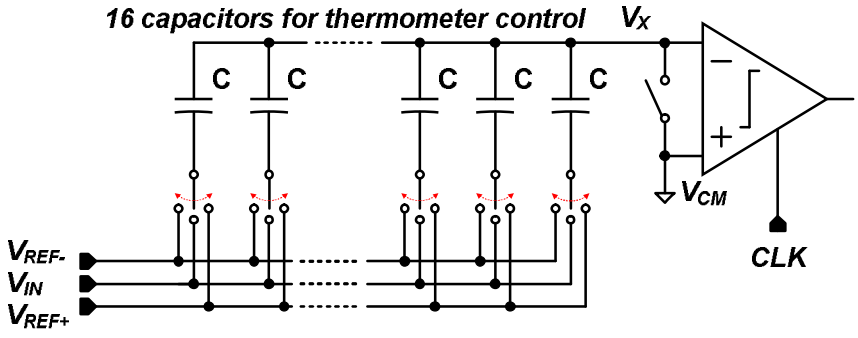


Fig. 2-3. Structure of a thermometer controlled NWC DAC

In fact, when the Kuttner proposed the non-binary SAR ADC with a capacitor DAC firstly at 2000's ISSCC [02.ISSCC.Kuttner], the DAC structure he implemented is the following Fig. 2-3. All elements of the DACs are controlled one by one, and its sub-radix is defined by digital ROM. This DAC structure has the same INL plot as the BWC DAC.

2.1.1.3 Bridge capacitor DAC (BC DAC)

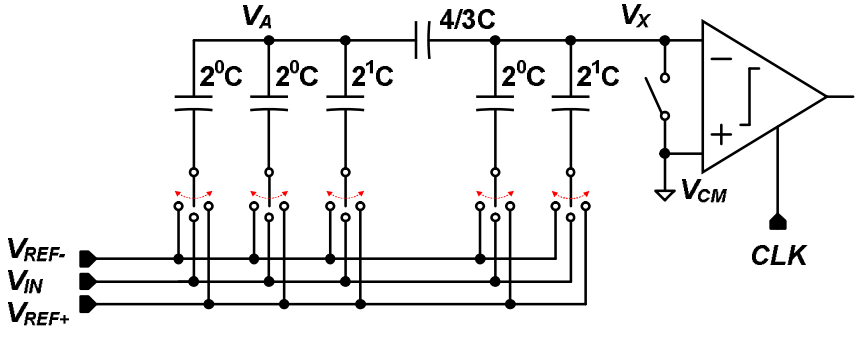


Fig. 2-4. Structure of a BC DAC

The BC DAC as shown in Fig. 2-4 is one type of the hybrid DAC mixing two capacitor

DACs. There are two elements at the MSB side and also two elements at the LSB side. Therefore it is called 2b+2b hybrid structure. This structure was also not feasible for more than 10b ADC since the mismatch of the weighting factors between the smallest capacitor of MSB side and all capacitors at the LSB side is large which comes from fractional bridge capacitor and which is induced by a parasitic capacitor at the V_A node. However, the growing interest in high resolution and high speed SAR ADCs makes the BC DAC be considered again because this DAC structure has small sample capacitance equivalently. With the calibration algorithms, the BC DAC has frequently been selecting to a 12b SAR ADC.

2.1.2 Design consideration

2.1.2.1 kT/C noise

The capacitor DAC in a SAR ADC is usually used as sampling capacitor of S/H circuits. Therefore, total sampling capacitor must be designed to satisfy the kT/C noise requirement. The relation of signal power to kT/C noise is expressed by following Eq. 2-2 about the single ended sampling network when V_{PP} indicates peak-to-peak signal voltage.

$$\text{Signal-to-kT/C noise}_{\text{single-ended}} = 10\log\frac{P_{\text{Signal}}}{P_{\text{kT/C}}} = 10\log\frac{V_{PP}^{\,2}/2}{\text{kT/C}} \qquad \text{(Eq. 2-2)}$$

If the input sampling network is designed differentially, because signal amplitude is two times larger and noise power increases as two times, the relation is modified as follows.

$$\text{Signal-to-kT/C noise}_{\text{diff}} = 10\log\frac{(2V_{PP})^2/2}{2\cdot\text{kT/C}} = 3\text{dB}+10\log\frac{V_{PP}^{\,2}/2}{\text{kT/C}} \qquad \text{(Eq. 2-3)}$$

Using this equation, we can obtain minimum capacitance to satisfy the kT/C noise

requirement when the resolution and signal power are given.

2.1.2.2 Capacitor matching

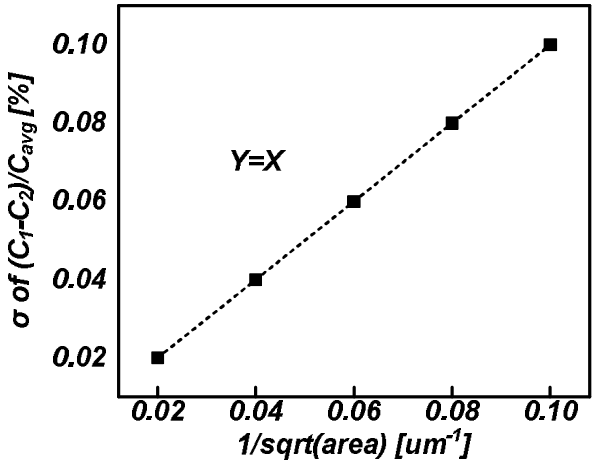


Fig. 2-5. Capacitor mismatch

To know the size of a unit capacitor, the designer must find the standard deviation value (one sigma = σ) which meets certain yield (ex. 99.9%) at first. The specific sigma value has the designers choose the unit capacitor size with the mismatch information provided by the foundries as shown in Fig. 2-5. The sigma value can be obtained by a behavioral MATLAB simulation [98.JSSC.Lin]. Next three Fig. 2-6~8 show the RMS DNL and INL plots about three DACs with 10b resolution and 2% standard deviation of the four DACs described in the section 2.1.1. RMS DNL and INL peak values of BWC DAC are 0.64LSB and 0.32LSB, respectively. Those of thermometer DAC are 0.02LSB and 0.32LSB, respectively. Note that the RMS INL peak value is still the same. Those values of BC DAC are about 4LSB and 2LSB, respectively. We can know that the yield is totally different according to a DAC structure, even though the resolution and one sigma value are the same.

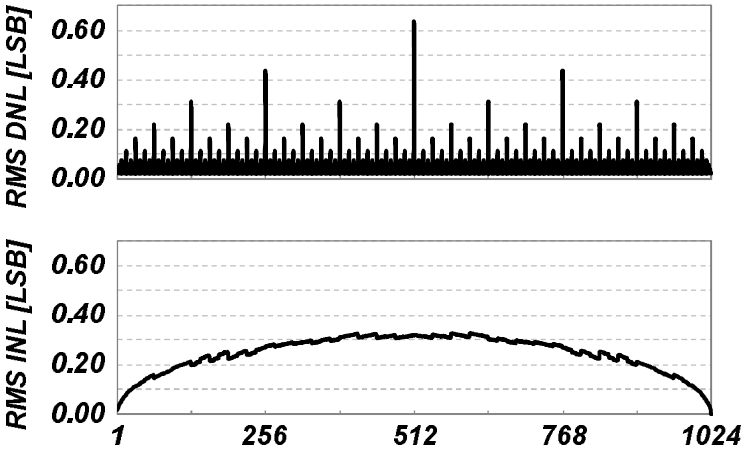


Fig. 2-6. RMS DNL and INL of BWC DAC

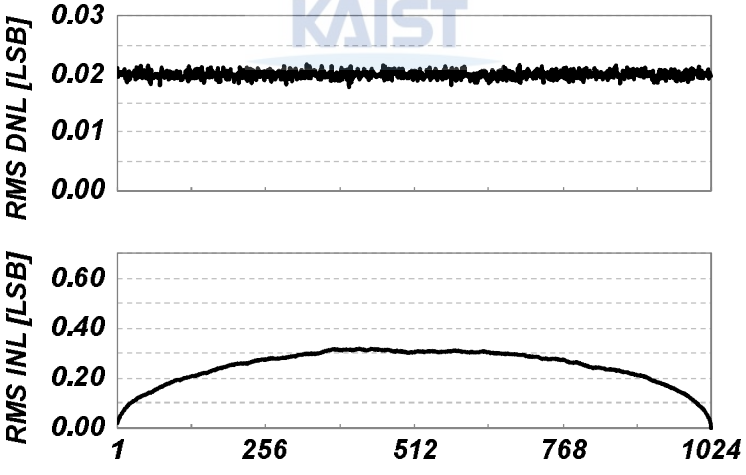


Fig. 2-7. RMS DNL and INL of thermometer DAC

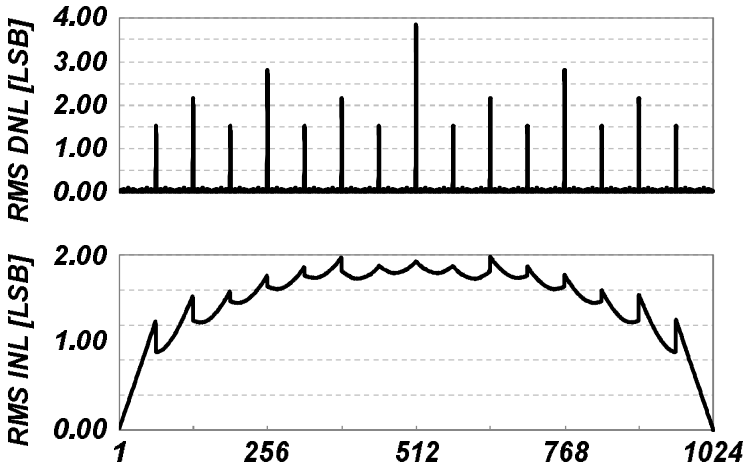


Fig. 2-8. RMS DNL and INL of BC DAC (5b+5b)

2.2 Sampling switch

A sampling switch has to be carefully designed with consideration of linearity performance, since non-linearity in the sampling network contributes to overall ADC linearity errors. There are two kinds of switches: top plate sampling switch and bottom plate sampling switch.

2.2.1 Top plate sampling (TPS) switch

Fig. 2-9 shows a NMOS top plate sampling. This is called a "top plate sampling" switch, because this circuit samples the input at the moment when the switch on top plate of sampling capacitor is turned off. When Φ_{sam} is high, the NMOS switch operates at $V_{GS} = V_{DD}-V_{IN}$, and the signal transfer function (STF) is expressed by the following Eq. 2-3.

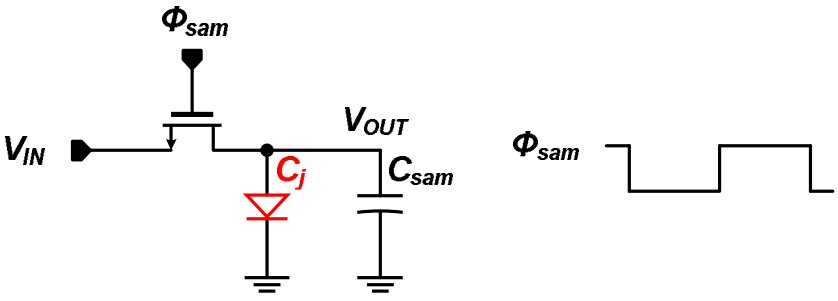


Fig. 2-9. NMOS top plate sampling switch

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1+s \cdot R_{on}(C_{sam}+C_j)} \quad \text{(Eq. 2-3)}$$

If R_{on} is an ideal resistor, the above STF certainly is linear on input amplitude; however, since R_{on} is the function of input amplitude as expressed in Eq. 2-4., the signal gain is different according to its input level. This is the main reason to injure its linearity on the TPS switch.

$$\frac{1}{R_{on}} = \mu_n C_{ox} \frac{W}{L}(V_{DD}-V_{IN}-V_{th}) \quad \text{(Eq. 2-4)}$$

There are the other four reasons; input dependant CLK feed through, input dependant channel charge injection, input dependant change of threshold voltage (V_{th}) by body effect, and input dependant capacitance of C_j.

PMOS and CMOS top plate sampling switches can be identically understood with a NMOS TPS switch except for sampling the input of a higher common level.

2.2.2 Bottom plate sampling (BPS) switch

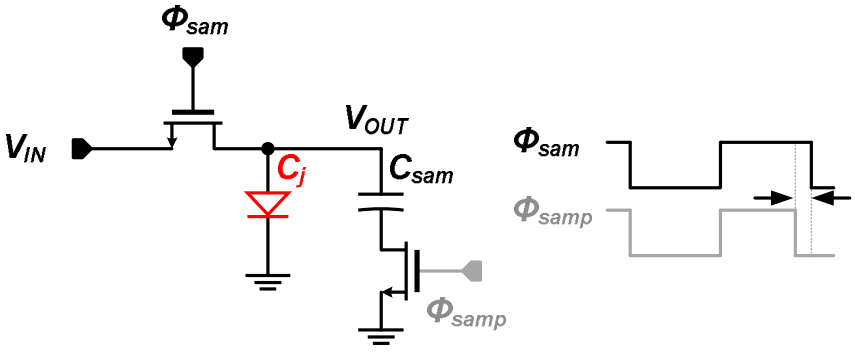


Fig. 2-10. NMOS bottom plate sampling switch

Fig. 2-10 shows a NMOS bottom plate sampling. This is called "bottom plate sampling" switch, because this circuit samples the input at the moment when the switch connected with bottom plate of sampling capacitor is turned off, not at the falling edge of Φ_{sam}.

Many designers use the bottom plate sampling switch technique, because input dependant CLK feed through and channel charge injection problems are easily solved even through the prime CLK (Φ_{samp}) generator and one TR switch are additionally used. Note that the effects of nonlinear R_{on}, varying V_{th}, and nonlinear C_j on SFDR still remain as problems that must be solved.

2.2.3 Bootstrapped switch

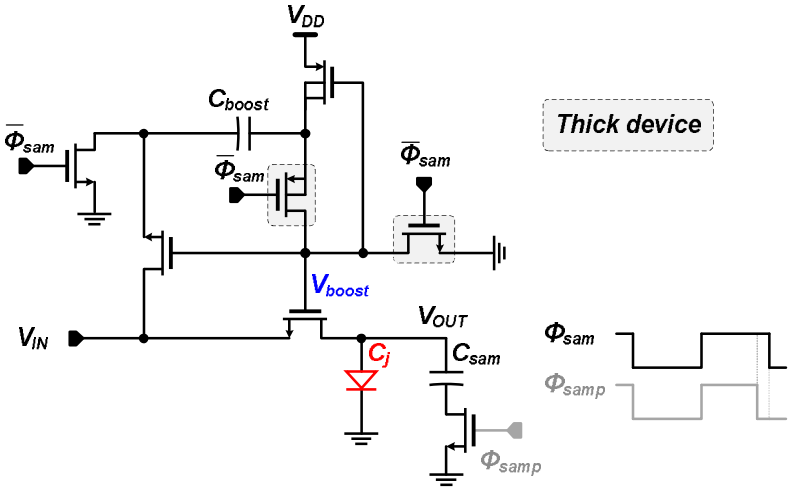


Fig. 2-11. Schematic of Eric's bootstrapped switch

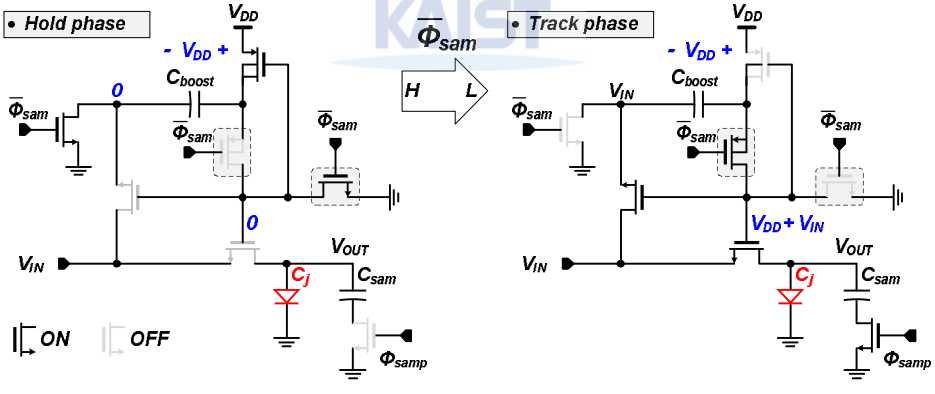


Fig. 2-12. Operation of Eric's bootstrapped switch

In the low supply voltage application, it's even hard to guarantee the signal swing range. This problem along with nonlinear R_{on}, varying V_{th}, and nonlinear C_j mentioned above can be mitigated greatly by the clock bootstrapped switch technique, which

increases the gate voltage of sampling switch. [95.JSSC.Cho, 99.JSSC.Abo, 00.ISSCC.Pan, 04.JSSC.Eric] The Fig. 2-11~12 shows Eric's bootstrapped switch and its operation which is popular and composed of the least number of gates.

During a hold phase, C_{boost} is pre-charging V_{DD} and the input tracking switch is turned off by V_{boost}. (=0). After $\overline{\Phi_{sam}}$ goes to low, the branches from power supplies connected to C_{boost} are broken, and the bottom plate of C_{boost} begins to track the input (V_{IN}). Therefore, the V_{boost} becomes $V_{DD}+V_{IN}$ as shown in Fig. 2-12. In practical, V_{boost} will be a little less since the considerable parasitic capacitance is being at the V_{boost} node. If the total parasitic capacitance seen at the V_{boost} node is christened C_P, the new V_{boost} is re-defined as following Eq. 2-5. To reduce charge sharing effects by C_P, C_{boost} must be chosen to be properly large.

$$V_{boost} = \frac{C_{boost}}{C_{boost}+C_P} \cdot \left(V_{DD}+V_{IN}\right) \quad \text{(Eq. 2-5)}$$

2.3 Comparator

A comparator is the key building block as a 1b-quantizer to resolve the sampled input V_{IN} and the output of a DAC. The two main design factors in a comparator are thermal noise and offset. To meet the tight thermal noise and offset requirement in the high resolution SAR ADC, a preamplifier has been a good solution, but if the latch-only comparator without a preamplifier has sufficient margins for noise and offset, it is just a burden. The Fig. 2-13 shows an example schematic of a latch-only comparator. In

addition, together a kick-back noise and the total capacitance of a DAC should be considered.

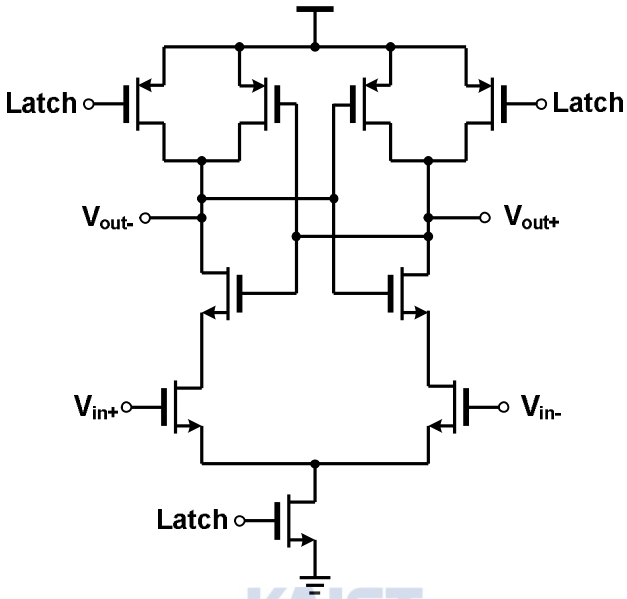


Fig. 2-13. Schematic of a dynamic latch

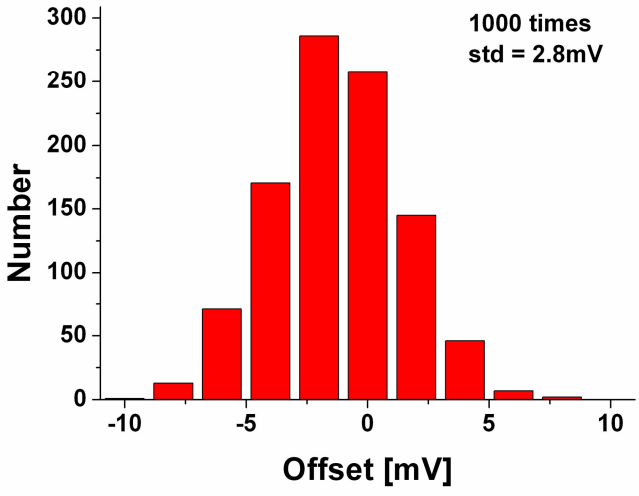


Fig. 2-14. Offset simulation example

2.3.1 Offset

The offset of a comparator is the total offset of a SAR ADC which just limits little signal power but not linearity, and, therefore, it is out of considerations in most cases. However, note that when SAR ADCs are applied to time-interleaving technique or a comparator is used for a capacitor mismatch calibration, the offset should be calibrated. Fig. 2-14 shows an example of Monte-Carlo offset simulation to estimate the offset of a comparator. The 'std' means one sigma offset voltage.

2.3.1 Thermal noise

The thermal noise of a comparator is one of the main noise sources in a SAR ADC. Let's see the influence of the thermal noise by the followings extracted from [08.ISSCC.Giannini] of the IMEC.

"In SAR ADCs, comparator thermal noise can limit the maximum achievable resolution. More than 1 and 2 ENOB reductions are observed in [07.ISSCC.Craninckx] and [02.ISSCC.Kuttner], respectively, because of thermal noise, and degradations could be even worse with scaled supply voltages and the extensive use of dynamic regenerative latches without pre-amplification. Unlike mismatch, random noise cannot be compensated by calibration and would finally demand a quadratic increase in power consumption unless alternative circuit techniques are devised."

This tells us that the thermal noise level need to be exactly estimated using AC noise, or transient noise simulations. To understand additionally how the thermal noise

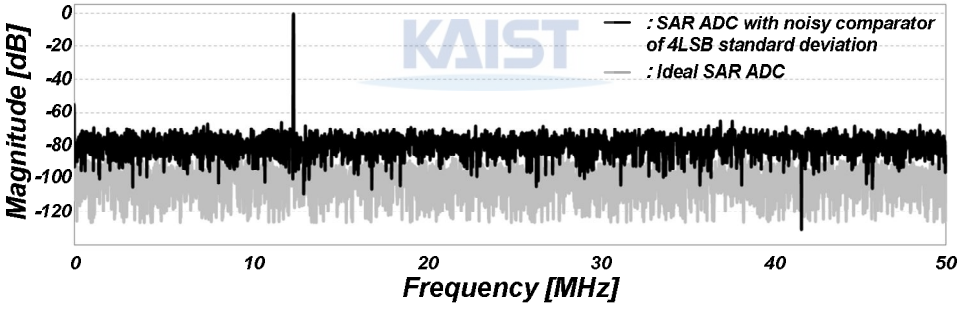


Fig. 2-15. FFT waveforms of the SAR ADCs with noiseless and noisy comparator

influences a FFT profile, the SAR ADC is modeled with the comparator having white noisy decision-thresholds by MATLAB.

The noise power is controlled by the standard deviation of a white Gaussian random sequence. When one-sigma values were changed to '0 → 1 → 2 → 4'LSB for an ideal

SAR ADC with 10b ENOB, each ENOB became '10 → 9→ 8.24 → 7.37'b. As you can see in Fig. 2-15, the noise floor just goes upward. Please, keep in mind that there are any no tones at all.

2.4 SAR controller

2.4.1 Synchronous SAR controller

Before 2006, the controller for most SAR ADCs is designed synchronously. This means as illustrated in Fig. 2-16 that overall control signals are generated by an external system CLK which is usually '1+resolution' times faster than an assigned sampling frequency (f_s). Fig. 2-17 shows SAR controller waveforms. All 5bits from MSB to LSB will be resolved one by one, beginning of rising edge of C1. After 5 times conversions,

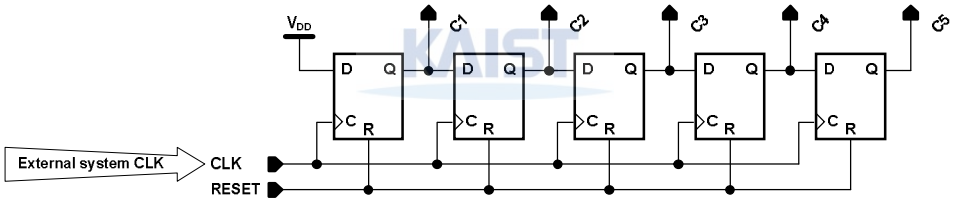


Fig. 2-16. Synchronous 5b SAR controller

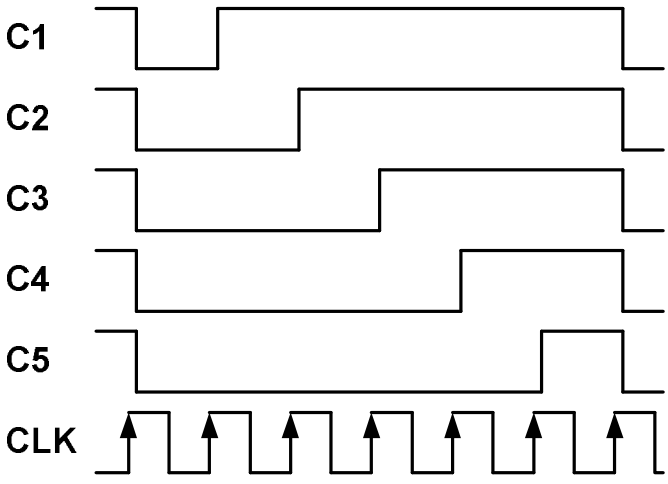


Fig. 2-17. SAR controller waveforms

all DFFs are reset by the rising edge of a system CLK only for the logic high period of C5. The synchronous SAR controller is driven by a high frequency CLK driver.

2.4.2 Asynchronous SAR controller

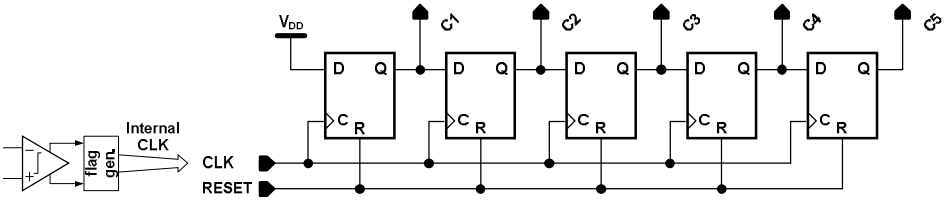


Fig. 2-18. Asynchronous 5b SAR controller

The Fig. 2-18 shows the schematic of an asynchronous 5b SAR controller. A DFF array is identical to a synchronous one. Only one difference is the sources of CLK, which are the two outputs of a comparator. Exclusive-OR (XOR) gate driven by comparator performs the roll of flag generator, whose output will be high when the comparator has two different outputs in the latching phase, and whose output will be low when the two outputs of a comparator are the same in the reset phase as if the "flag" is an external high frequency CLK. In an asynchronous decision, the signal "flag" detected with XOR indicates the completing a comparison. The rising edge and falling edge of this CLK shows up asynchronously by irregular repetitions of latching and reset of a comparator, because the comparator's latching time is logarithmically proportional to its input magnitude [06.JSSC.Chen]. The SAR ADC with asynchronous controller can increase the conversion speed effectively, because the DAC settling operation is started as soon as the flag goes up. This is different with a synchronous SAR ADC which must unconditionally wait the next falling edge of a system CLK to start DAC settling after comparison at the rising edge. The ratio of total latching time of asynchronous and synchronous SAR ADC (T_{asynch}/T_{synch}) approaches 1/2 as the resolution increases. [06.JSSC.Chen] Besides, this controller does not require external high frequency system CLK.

2.5 Switching logics

Switching logics play a role to control switches driving references and input signal and are usually designed by using static logics: inverter, NAND, NOR, and so forth. Design issues of these logics are two: one is the logic delay, and the other is power

consumption. If, in 10b SAR ADC, one cycle excess logic delay is measured as 100ps, this ADC wastes time about 1ns (10*100ps). The most recent SAR ADC in the IMEC implements logics to minimize the power consumption [10.ISSCC.Harpe].

3.Power Efficient Algorithms: MTS SAR ADC

Abstract: A dual-channel asynchronous successive approximation register (SAR) analog-to-digital converter (ADC) for low-power communication systems is presented with two power-efficient conversion techniques. Straightforward digital-to-analog converter (DAC) control removes the switch-back operation in traditional SAR ADC and saves DAC switching power consumption. The metastable-then-set (MTS) algorithm further reduces power consumption by finishing the conversion when the metastability is detected. The interference between two asynchronous ADCs sharing a common reference is minimized by the flag-synchronization method. The prototype ADC has been implemented in a CMOS 0.13μm technology and operates under 1.2V supply. At a sampling rate of 17.5MS/s, the chip achieves a peak SNDR of 51.3dB at the input frequency of 1.73MHz. The measured total power dissipation is 580μW, and the figure of merit is 100fJ/step.

In this chapter 3, we have exploited the possibility of SAR ADC in low power communication systems by designing an I/Q dual-channel ADC. The prototype ADC adopts an asynchronous conversion technique which makes SAR ADC more feasible for high speed applications by removing the high frequency internal clock and also by reducing the time for the comparator latching operation in the whole conversion process.

Two power-efficient conversion techniques have been proposed. The straightforward DAC control method saves power dissipation from the DAC by removing the switch-back operation of the DAC element which occurs in conventional SAR ADCs. The proposed metastable-then-set (MTS) algorithm utilizes the characteristic of the comparator's metastability to reduce the digital power consumption of the SAR logic and switch drivers. With the designed single channel ADC, dual-channel ADC has been built up for the use of an I/Q receiver path in communication systems.

This chapter is organized as follows. The proposed straightforward DAC control method in section 3.1 and the MTS algorithm in section 3.2 will be explained with corresponding circuit designs. Section 3.3 and section 3.4 will show the designed DAC structure and overall architecture. In section 3.5, the inter-channel synchronization method for the two asynchronous ADCs will be discussed to reduce the inter-channel interference under the shared reference condition. Section 3.6 will show the measurement results, and the conclusion will be described in section 3.7.

3.1 Straightforward DAC switching algorithm

3.1.1 Understanding straightforward DAC switching algorithm

One major source of power consumption in a SAR ADC comes from the charge and discharge operations of the DAC during the bit decision cycles [05.ISCAS.Ginsburg]. We find the possibility to consume more DAC switching power in a conventional SAR ADC. The reason is that there are two types of DAC switching; assumption-switching and feedback-switching as shown in Fig. 3-1. The assumption-switching needs to make V_{DAC} level be located at the center of every DIRs and a SAR ADC selects the corresponding DIR

for the next A/D conversion by feedback- switching. These assumption-switching and

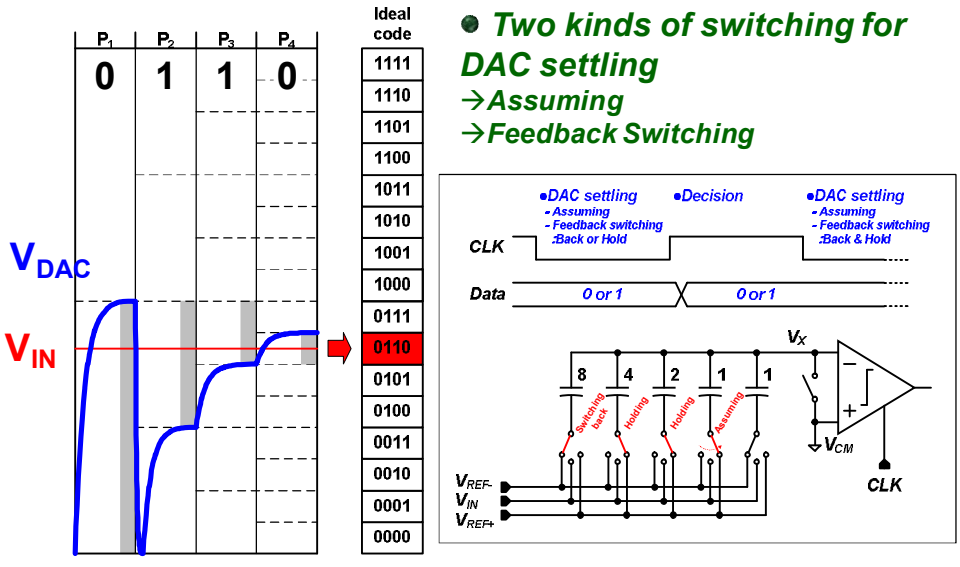


Fig. 3-1. Two types of switching in a conventional SAR ADC

switch-back operations of DAC element consume unnecessary switching power in a conventional SAR ADC.

The proposed straightforward DAC control method for a 4b SAR ADC is animated from Fig. 3-2 to Fig. 3-6 against a conventional SAR DAC switching algorithm. Fig. 3-2 shows sampling phase where DACs sample the input signal (= 6.5/16) through bottom plates. The most notable difference is that there is no the largest MSB capacitor ($2^{N-1}C = 8C$). Fig. 3-3 shows the MSB decision phase (P_1) of straightforward switching. Reminding that the MSB represents the signal polarity compared with V_{CM}, we can simply achieve the MSB by detecting the input signal polarity. If the bottom plates of all the capacitors are connected to the V_{CM} after sampling the input signal, then the signal polarity is determined by the

input signal itself without the need of 8C. In other to generate the next quantization level

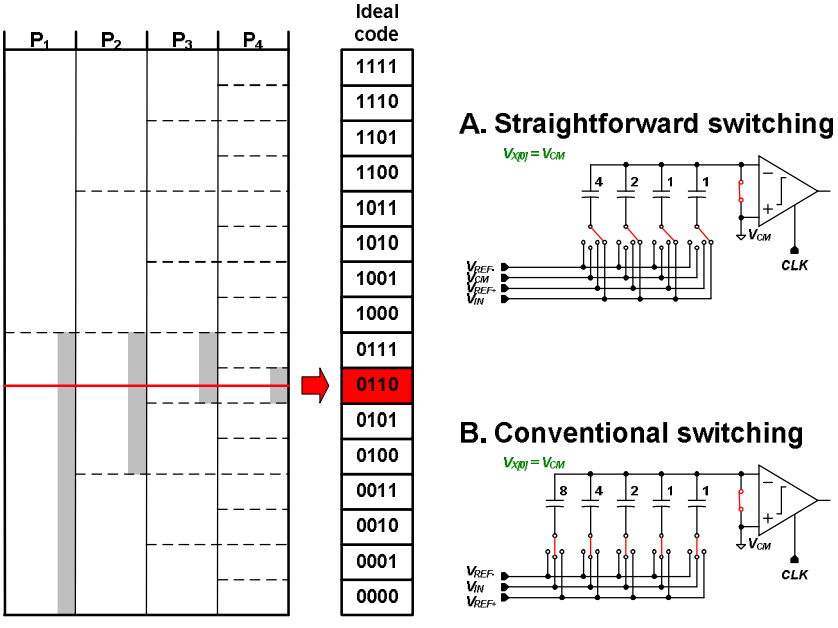


Fig. 3-2. Sampling phase of straightforward switching

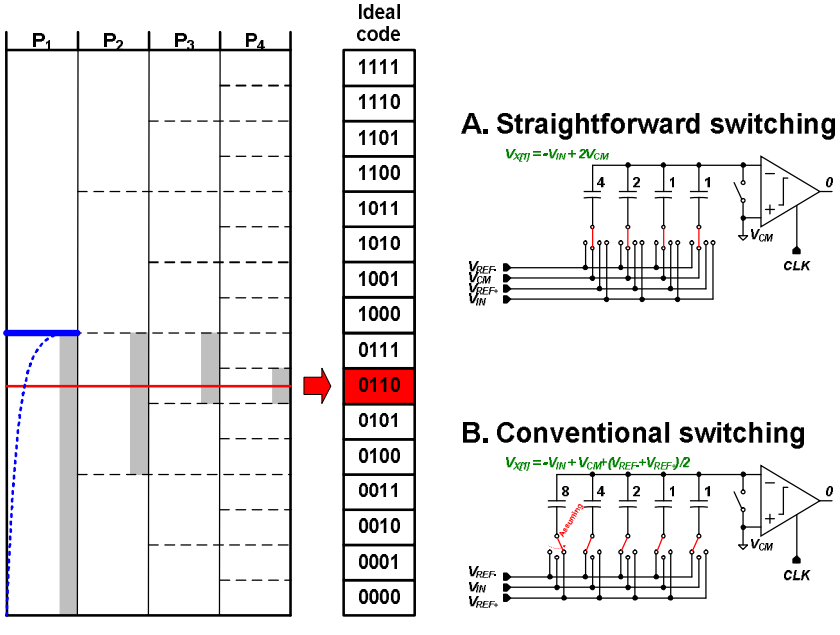


Fig. 3-3. MSB decision phase (P_1) of straightforward switching

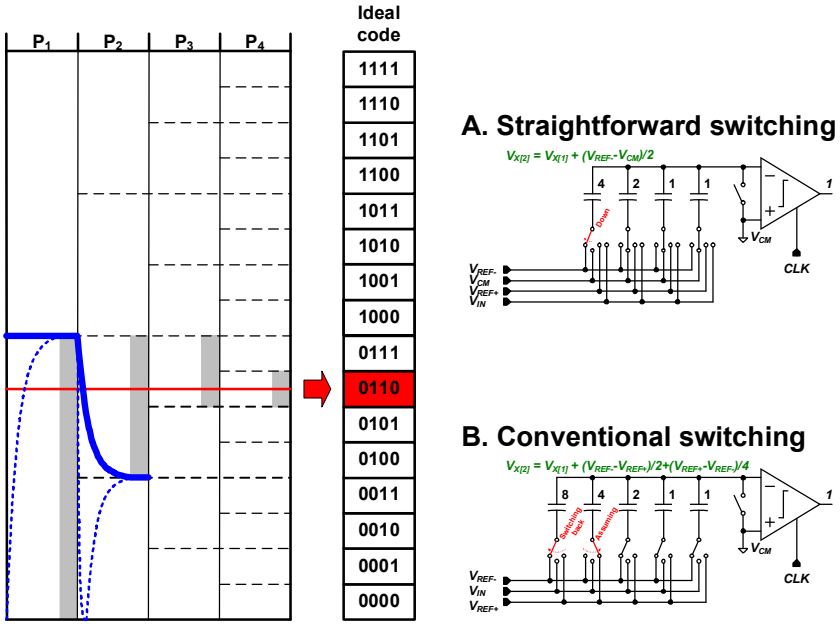


Fig. 3-4. MSB-1 decision phase (P_2) of straightforward switching

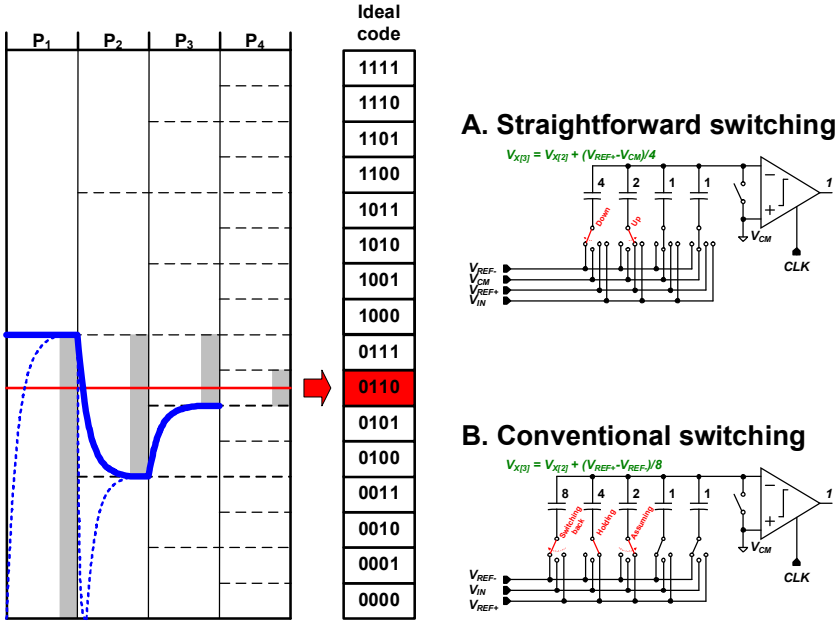


Fig. 3-5. LSB+1 decision phase (P_3) of straightforward switching

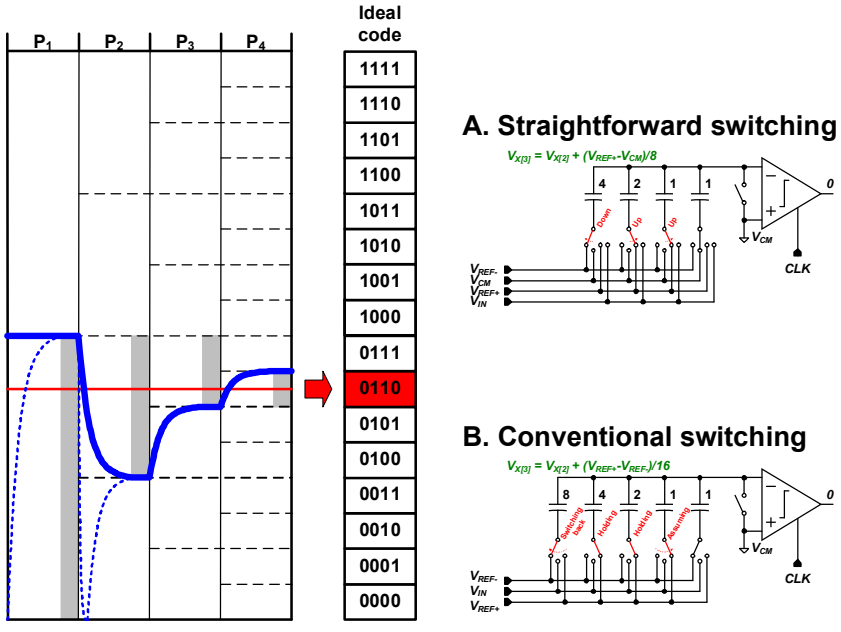


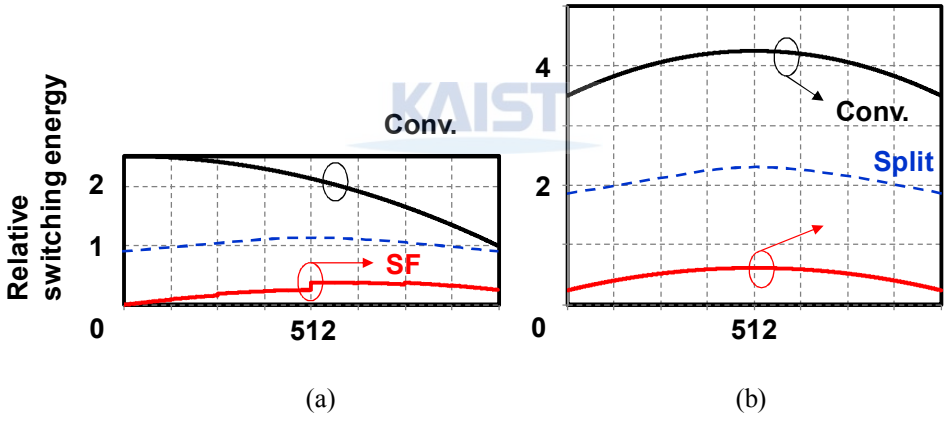
Fig. 3-6. LSB decision phase (P_4) of straightforward switching

which is the center of the DIR_1, we have to connect the 4C to either V_{REF+} or V_{REF-}, while the other capacitors are still connected to the V_{CM}. If the MSB is 0, in the example, the capacitor 4C is directly connected to V_{REF-} as shown in Fig. 3-4. Seeing the DAC waveforms in Fig. 3-4, you know that the trace of a dashed V_{DAC} twists relatively more, that is, it means that a conventional SAR ADC has unnecessary DAC switching. In cases of rest two figures (Fig. 3-5~6), the two V_{DAC} waveforms trace the same way since there is no the switching back operations in a conventional SAR ADC. V_{DAC} eventually reaches V_{IN} at the end of the conversion in this straightforward DAC control, because the successive approximation (SA) operation is the discrete-time negative feedback operation,

as defined in the above section 1.2.1.

3.1.2 Effect of straightforward DAC switching algorithm

Several algorithms have been reported to reduce the power wasting in DAC switching in SAR ADC [05.ISCAS.Ginsburg], but the straightforward switching method completely eliminates unnecessary DAC operations and its power wasting. The straightforward DAC control method consumes only about 12.5% of conventional switching energy as shown in Fig. 3-7. By removing the MSB capacitor, this algorithm reduces the DAC size by half and reduces DAC charging energy as well.



(a) (b)

Fig. 3-7. Comparison of DAC switching energies according to algorithm (a) single-ended SAR ADC (b) differential SAR ADC

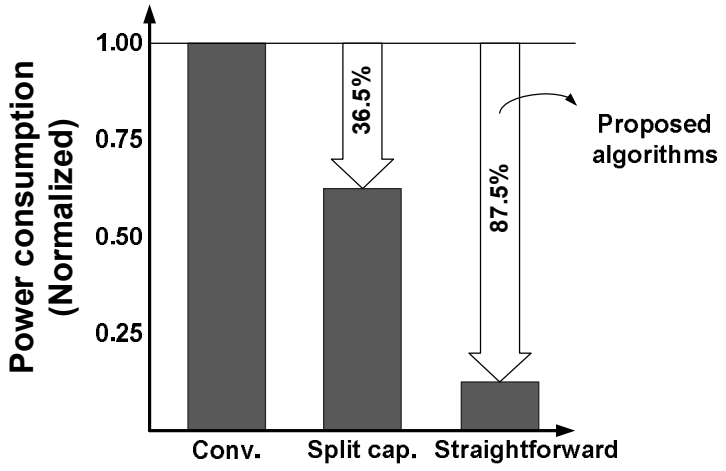


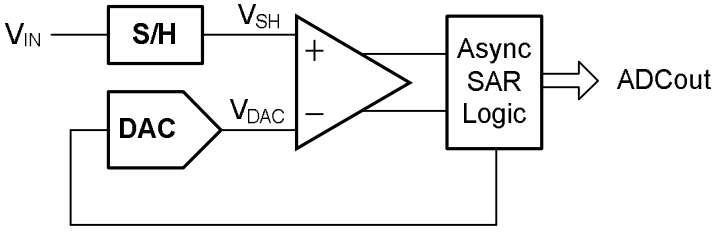
Fig. 3-8. Comparison of power efficient algorithms

3.2 Metastable-then-set (MTS) algorithm

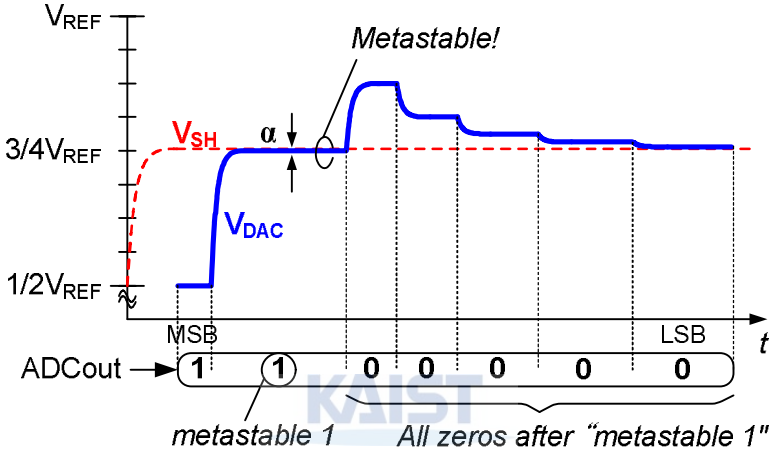
3.2.1 Understanding metastable-then-set (MTS) algorithm

Metastability of the latch-based comparator is troublesome in many data converters, because it takes unusually long time for logic level decision, and it often generates huge amount of decision error. To avoid a metastability problem, traditional ADC designs have tried to design high-gain, high-speed comparators, to use an external high frequency system CLK unnecessary in an asynchronous SAR ADC [05.CICC.Ginsburg], or to generate early flag before the metastability occurs [06.ISSCC.Chen]. Unlike previous works, however, the design utilizes the characteristic of metastability to save the digital power consumption and it is called the metastable-then-set (MTS) algorithm.

The operational principle of the MTS algorithm is explained with Fig. 3-9. Fig. 3-9(a) shows a conceptual block diagram of an asynchronous SAR ADC. Note that S/H and



(a)



(b)

Fig. 3-9. (a) Simple block diagram of asynchronous SAR ADC and (b) transient waveform of DAC and the code decision

DAC are separated just for convenient explanation. Fig. 3-9(b) shows the waveform of the DAC (V_{DAC}) for the sampled input, V_{SH}. Sequentially achieved digital code in each phase is shown at the bottom of the waveform (ADCout).

Let's assume that V_{SH} is very slightly higher than 3/4 V_{REF} by a fraction of α LSB. In contrast to the MSB decision, the MSB-1 bit decision takes quite long time because of the metastability ($V_{DAC} \approx V_{SH}$). Since MSB-1 = 1, in the example, we call it "metastable

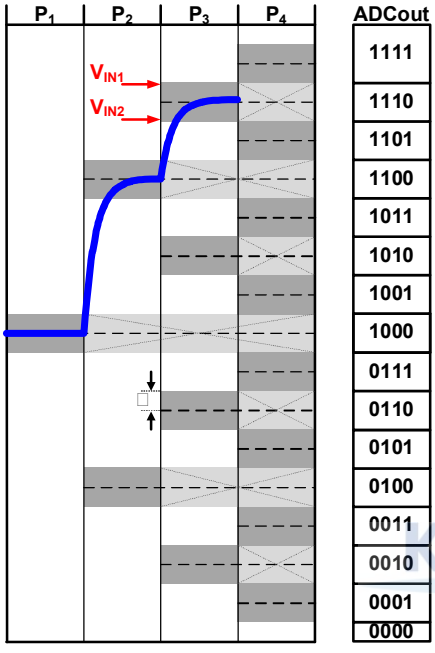
1". After the metastable 1, we can say that the following LSBs will be 0 consecutively by the SA algorithm. This observation can suggest a modified SA algorithm. That is, once the metastability has been detected, the rest ADC code can be forced to be 100…0. If we consider the case where V_{SH} is slightly lower than V_{DAC} in a certain decision phase, the corresponding bit will be 0, and the following bits should be all 1's. However, we do not need to be bothered to separate these two cases because the error amount is usually acceptable as α LSB. Thus, the proposed MTS algorithm sets the rest code 100…0 once the metastability is detected.

3.2.2 Effect of metastable-then-set (MTS) algorithm

The proposed MTS algorithm reduces the number of decision cycles, and, therefore, the digital power saving from the SAR logic is proportional to the number of the omitted decisions. In Fig. 3-10 (a), when the sampled input V_{IN} is located on a certain thick gray block, and, in other words, when the comparator has the input magnitude of less than α-LSB ($\alpha < 0.5$), the metastability occurs at the phase including a thick gray block and A/D conversions in rest phases do not happen as signed by soft gray with an X mark. Fig. 3-10 (b) calculates the power saving of the MTS SAR ADC.

If the metastability occurs in LSB+1 bit decision, then the LSB decision cycle can be omitted with the probability of α. This reduces the digital power consumption by $\alpha \times 1/N$ in an N-bit ADC. Similarly, metastability occurred in LSB+2 bit decision eliminates two LSB decisions with the probability of $\alpha/2$, and, therefore, the power saving is $\alpha/2 \times 2/N$. Accordingly, power saving from the reduced logic operations in an N-bit ADC can be expressed as Eq. 3-1.

$$\frac{P_{\text{Saved digtal}}}{P_{\text{Digital of conventional one}}} = \sum_{k=1}^{N-1} \frac{\alpha}{2^k} \frac{k}{N} \qquad \text{(Eq. 3-1)}$$



ADCout
1111
1110
1101
1100
1011
1010
1001
1000
0111
0110
0101
0100
0011
0010
0001
0000

■ **Start at the rising edge**

1. Input sampling

```
while (i ≤ N && meta=0 )
   {
      2. Compare VIN & VDAC
      If ('meta<i>=0')
            Save the data (D<i>) from
            comparator
      else,
            Save the 'D<i>=1 & D<i+1:N>=0'
      end
   }
```

■ **Wait the next rising edge**

(a)

	$P_{4(LSB)}$	P_3	P_2	P_1
Probability	α	$\frac{\alpha}{2}$	$\frac{\alpha}{4}$	$\frac{\alpha}{8}$
Saved power ratio	0	$\frac{1}{N}$	$\frac{2}{N}$	$\frac{3}{N}$
Total saved power ratio	$\frac{\alpha}{2}\frac{1}{N} + \frac{\alpha}{4}\frac{2}{N} + \frac{\alpha}{8}\frac{3}{N} = \sum_{k=1}^{N-1}\frac{\alpha}{2^k}\frac{k}{N}$			

(b)

Fig. 3-10. (a) MTS algorithm and (b) power saving calculation of MTS algorithm

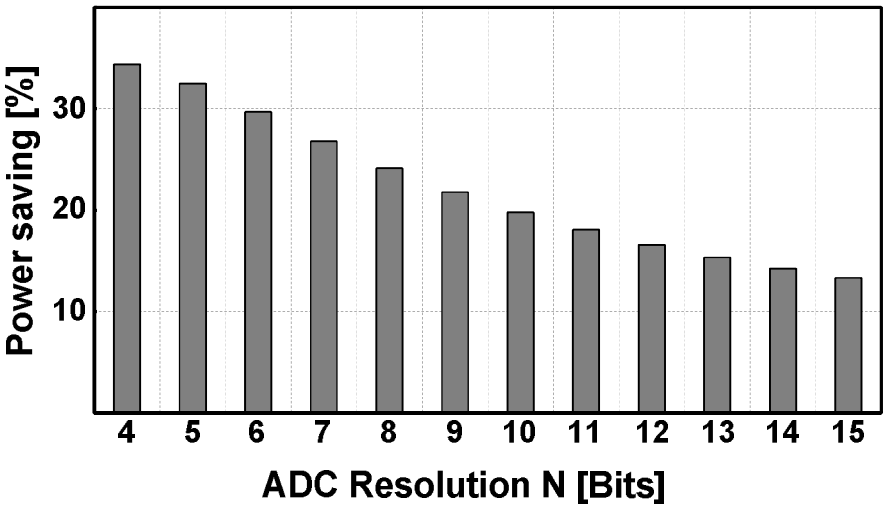


Fig. 3-11. Power saving effects of MTS algorithm when α= 0.5 in 4~15 bit ADC

The calculated total digital power saving from the logic operation in an N-bit ADC with α = 0.5 is shown in Fig. 3-11. This shows that the MTS algorithm is more effective in a low resolution ADC, and the maximum power saving by MTS algorithm is about 10% in a 10b MTS SAR ADC. Considering the range of the metastability strongly depends on PVT variations, we made α be designed less than 0.5 to avoid a missing code and be controlled externally to measure the relation between α and saved power.

3.2.3 Implementation of metastable-then-set (MTS) algorithm

Fig. 3-12 shows a part of the block diagram of the prototype ADC. At the rising edge of the *flag* (internal high frequency CLK), the SAR logic sets the DAC configuration according to the comparison result, and the DAC is settled to new value while the *extended flag* ($flag_{EXT.}$) is high whose pulse width is determined by the internal delay

cells. The relevant waveforms are depicted in Fig. 3-13. The metastability detector is implemented by using a ramp generator and a comparator with the decision threshold V_{TH_meta}. When the comparator is turned on by the rising edge of ϕ_{latch}, the *ramp* starts increasing. If the *flag* is 0 until the ramp reaches V_{TH_meta}, the metastability detector generates "*meta* = 1" signal to indicate the metastability occurrence. Once *meta* = 1, the rest SA operations stop and the rest codes are set to be 100…0, and the ADC starts tracking a new input until the next sampling edge comes. The first half of the waveforms in Fig. 3-13 shows a case with large input at the comparator, and the last half shows a case with very small input which results in metastability.

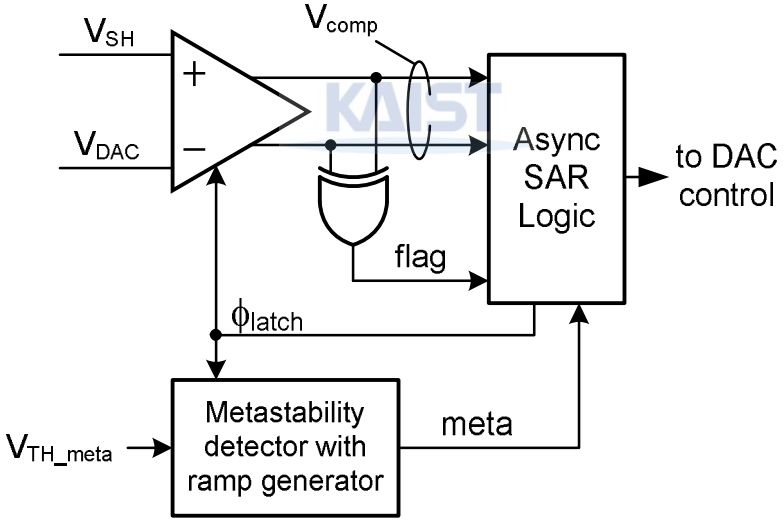


Fig. 3-12. Detailed diagram of asynchronous decision block

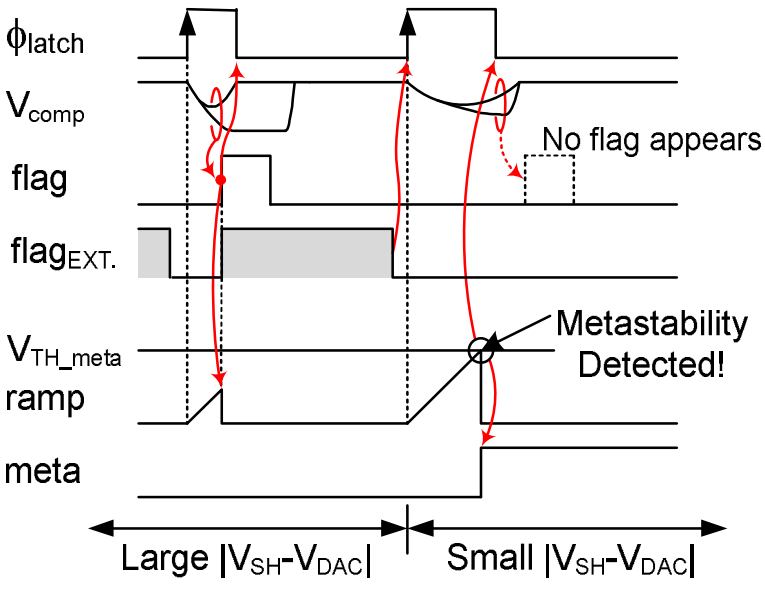


Fig. 3-13. Conceptual waveforms of metastability detector

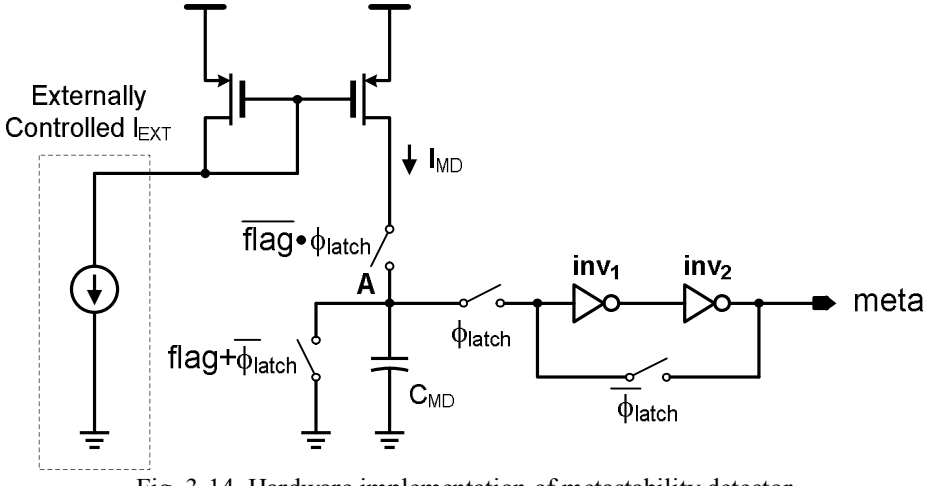


Fig. 3-14. Hardware implementation of metastability detector

Fig. 3-14 shows the hardware implementation of the metastability detector. The ramp generator has been designed with a simple integrator composed of a current source and a capacitor. By the rising edge of the latch clock, ϕ_{latch}, the integrator starts charging the capacitor. The integration finishes when *flag* = 1 or when the metastability is detected (when the node A reaches the logic threshold of the following inverter, inv_1). The inv_1 and inv_2 hold the *meta* value until the next ϕ_{latch} appears. The bias current is controlled externally to change the metastable detection time for the test purpose. In the design, the nominal external current was set to be 5μA. Since the capacitor value is 60fF, the designed nominal time for the metastability detection (t_{MTS}) is 1.1ns.

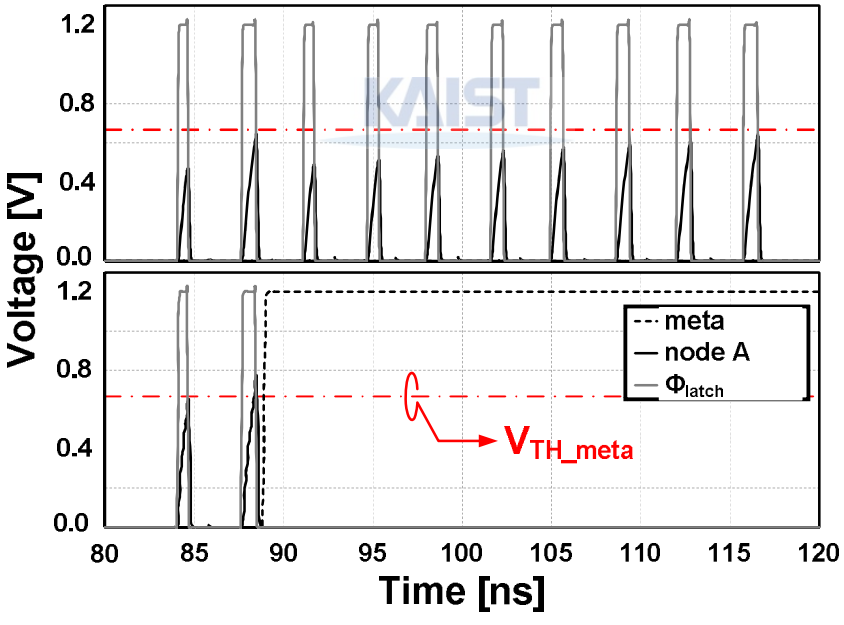


Fig. 3-15. Transient simulation waveforms of metastability detector in the case without metastability occurrence (upper) and with metastability occurrence (lower)

Fig. 3-15 shows the simulation waveforms of the metastability detector of the prototype ADC in cases without metastability occurrence (upper) and with metastability (lower). The logic threshold of inv_1 plays the role of V_{TH_meta} in this design and the value is about half of the supply voltage. Note that, *meta* = 1 stops the following SAR operations in the metastability occurred case by deactivating the ϕ_{latch}.

3.3 DAC structure

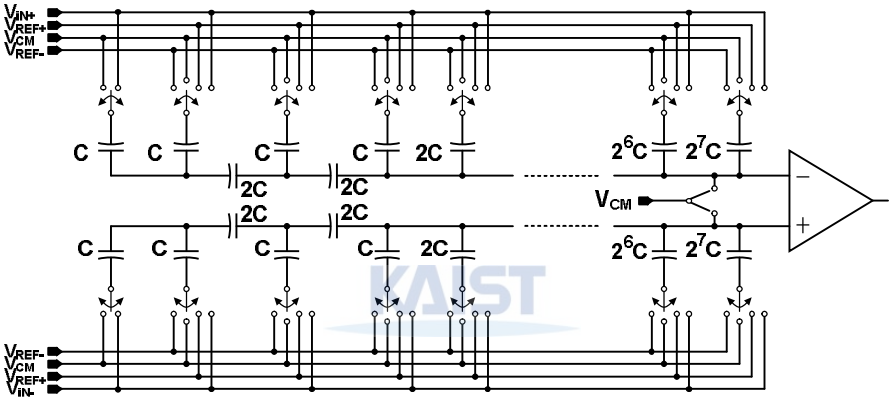


Fig. 3-16. 10b DAC architecture for MTS SAR ADC

A binary-weighted capacitor DAC has been designed in a fully differential structure for the prototype ADC. In order to further reduce the total capacitor size, the prototype 10b ADC employs a segmented DAC architecture with C-2C ladders as shown in Fig. 3-16. The DAC has only 9b resolution owing to the straightforward decision method. Since the bottom plate parasitic capacitance of the attenuation capacitor in C-2C structure can degrade the DAC linearity, a design trade-off between the capacitor size and linearity has been performed, and two C-2C ladders for the LSB segments with 40.7fF of unit capacitor

has been chosen. The total input capacitance is 5.2pF.

3.4 Overall architecture

Fig. 3-17 shows an overall architecture of metastable-then-set SAR ADC and the block diagram of a single channel ADC. I and Q channel MTS SAR ADCs are implemented for I/Q dual-channel input V_{IN_I} and V_{IN_Q}.

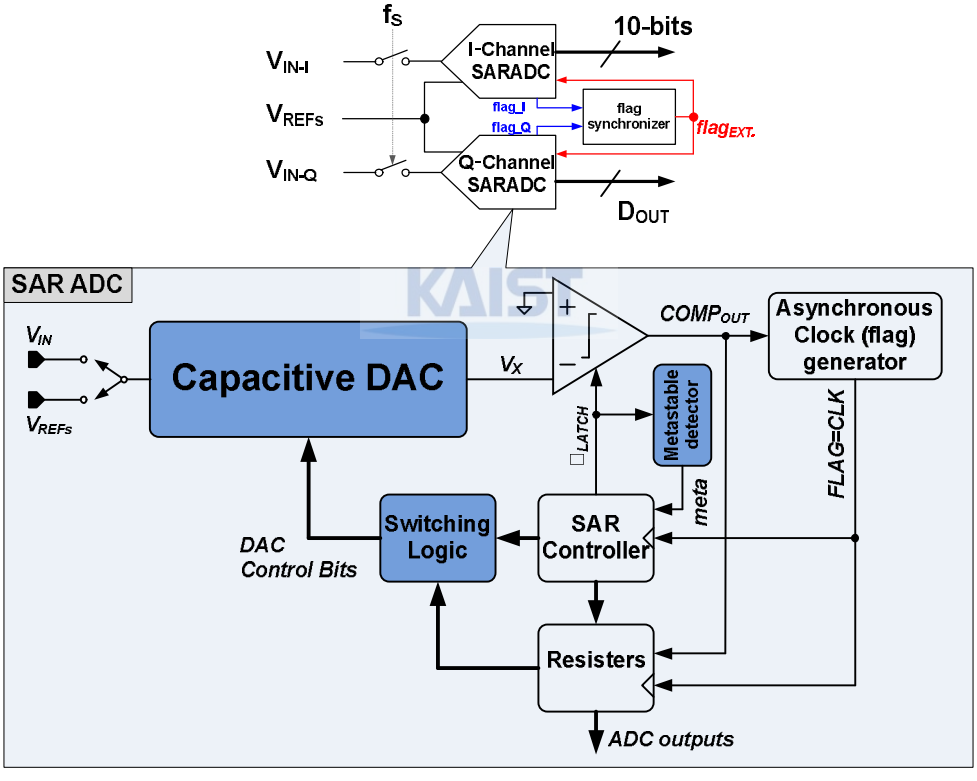


Fig. 3-17. Overall architecture of metastable-then-set SAR ADC and the block diagram of a single channel ADC

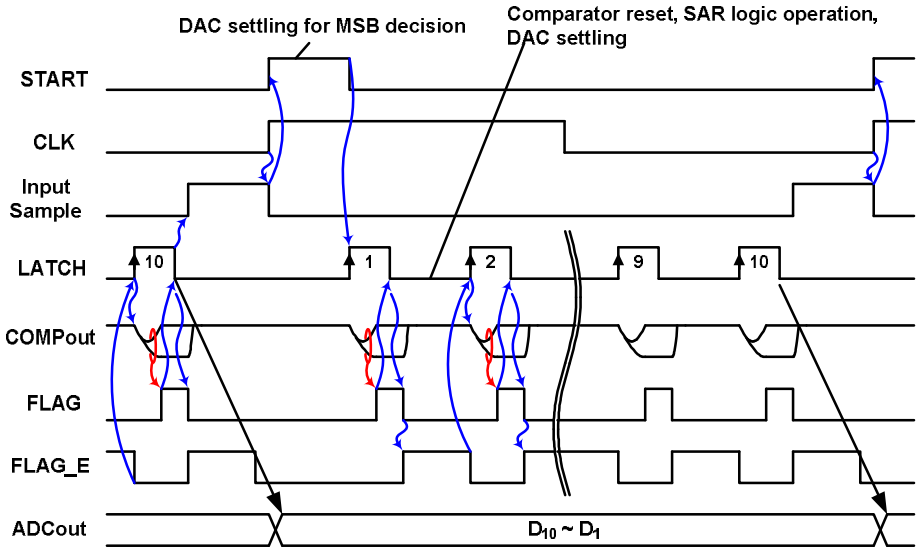


Fig. 3-18. Timing diagram for MTS SAR ADC

Fig. 3-18 shows a timing diagram which is the most vital in all data converter designs. Global system CLK (*CLK*) triggers start-up pulse generator which is not seen in the block diagram though. During the high level of the *START* signal generated by start-up pulse generator, the capacitor DAC completes the DAC settling for MSB decision. At the falling edge of the *START*, a comparator begins to resolve the MSB, and its pulse name is the *LATCH*. The outputs of a latch-only comparator are indicated by $COMP_{out}$. The *FLAG* goes up by flag generator when the outputs of a comparator are nearly split to logic levels. This rising edge makes the falling edge of the *LATCH* reset a comparator. The *FLAG* goes down because the both comparator outputs are reset together to V_{DD} by a low *LATCH* signal. The DAC settling for a second bit can start from the rising edge of *FLAG* which tells us the completion of comparison, and it is finished by the falling edge of *FLAG_E* after guaranteeing a sufficient time for DAC settling; in addition to, the

falling edge of *FLAG_E* makes *LATCH* go up to compare a second bit (MSB-1). After repetition by the time when the LSB is obtained, the input sampling CLK (*Input Sample*) is generated by the falling edge of 10th LATCH. The input signal has been tracked and held by the rising edge of *CLK*. The MTS SAR ADC was operated as following this timing diagram.

3.5 Inter-channel synchronization method

In this work, we have exploited the possibility of the application of SAR ADC for communication systems by designing an I/Q dual-channel ADC based on above-explained design techniques. In order to achieve good performance matching between the two ADCs, common reference supplies (V_{REF+}, V_{CM}, V_{REF-} in Fig. 3-16) have been shared by the two capacitor DACs. In the shared reference environment, we need to

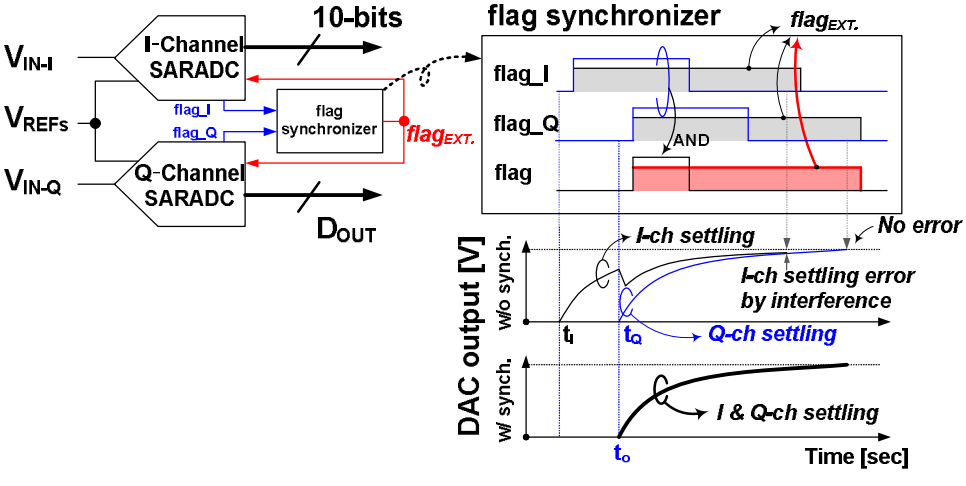


Fig. 3-19. Two channel synchronization

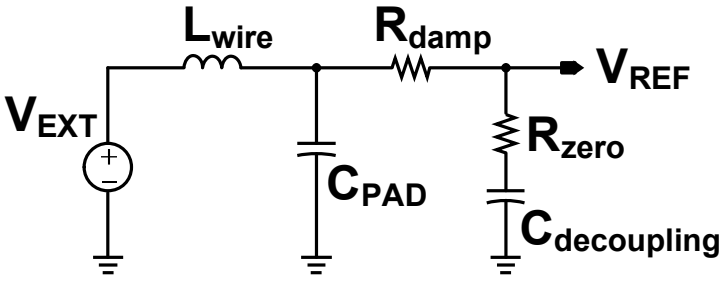


Fig. 3-20. Reference damping networks

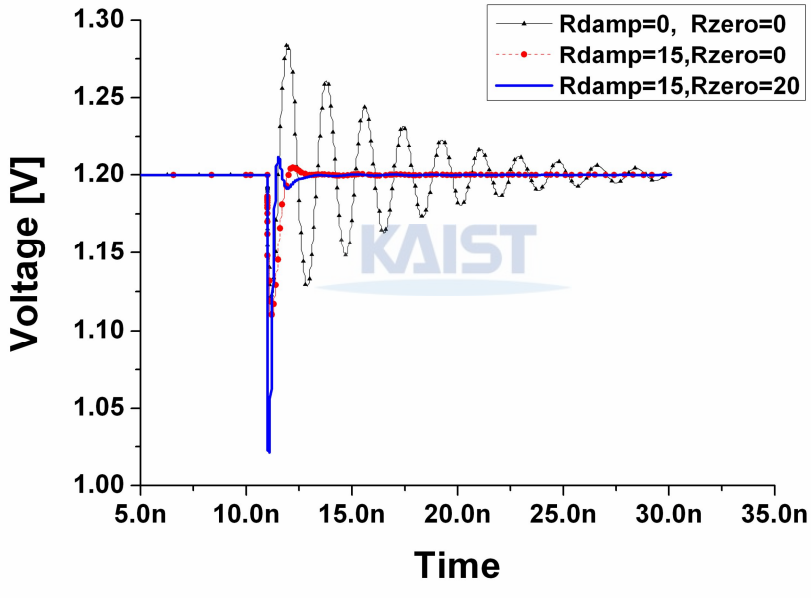


Fig. 3-21. Simulation waveform of reference damping networks

consider the possibility that one of the asynchronously controlled DACs can seriously spoil the settling behavior of the other by starting to be charged in the middle of the settling period of the other DAC as shown in Fig. 3-19.

In order to avoid such a destructive operation, two DACs' behaviors are synchronized by the proposed flag synchronizer which is designed using an AND gate. It takes two flag signals from both channels (flag_I and flag_Q) as its inputs and generates a common flag signal for both of them. By this, two DACs start to settle simultaneously, and no interference occurs any more. In case of no flag by the metastability occurrence in one channel, the *meta* signal is used for the synchronization.

For better reference settling performance, reference damping networks composed of shunt capacitor and series resistor have been inserted between the reference pads and the DACs as shown in Fig. 3-20. Fig. 3-21 shows how much the R_{damp} is effective to make quiet references.

3.6 Measurement results

3.6.1 General measurement

The proposed dual-channel SAR ADC has been fabricated in a 1.2V 0.13μm CMOS technology. The chip photo is shown in Fig. 3-22. The active area of the single-channel ADC is 500 × 700μm^2 and the dual-channel ADC occupies 500 × 1550μm^2. The measured FFT from a single channel ADC, while the other channel ADC was simultaneously working, is shown in Fig. 3-23. The input frequency is 1.73MHz, and the sampling rate is 17.5MS/s. The third harmonic is relatively high as 61dB, and the noise floor shows quite many small tones. Fig. 3-24 shows dynamic performances measured at 17.5MS/s with three input frequencies, 1.75MHz, 5MHz, and 8MHz. The measured peak SNDR is 51.3dB. Results in Fig. 3-23 and 24 show relatively poor performance than expected. One obvious reason has been found as the poor static

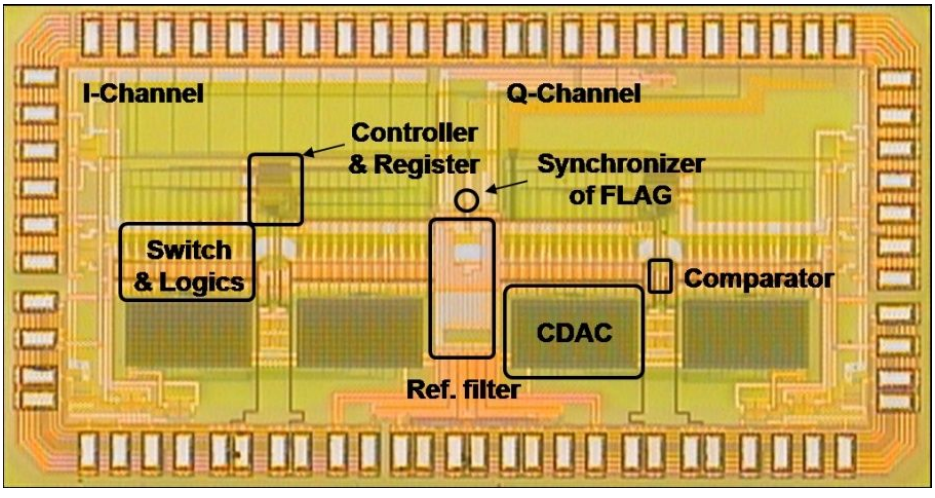


Fig. 3-22. Chip photo

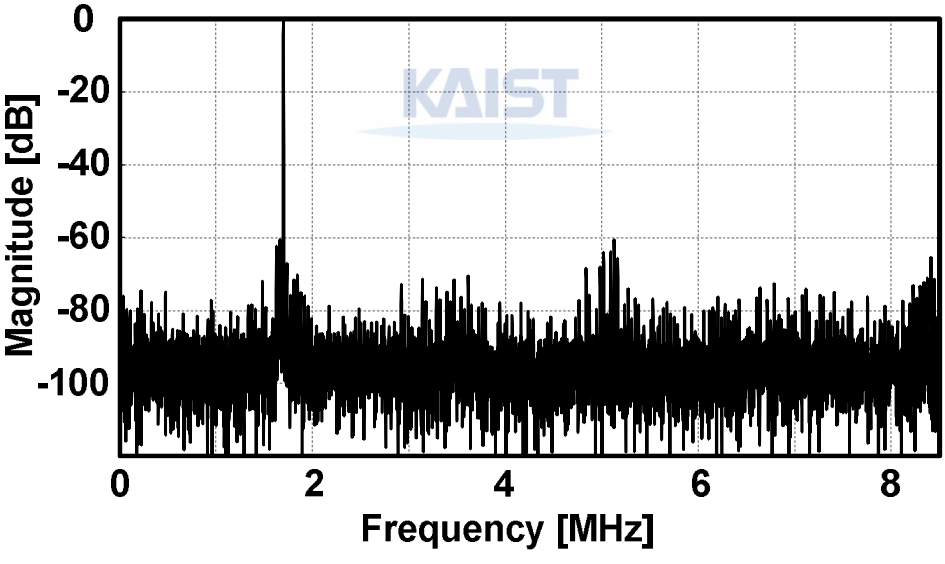


Fig. 3-23. Measured FFT result for 1.73MHz signal at 17.5MS/s

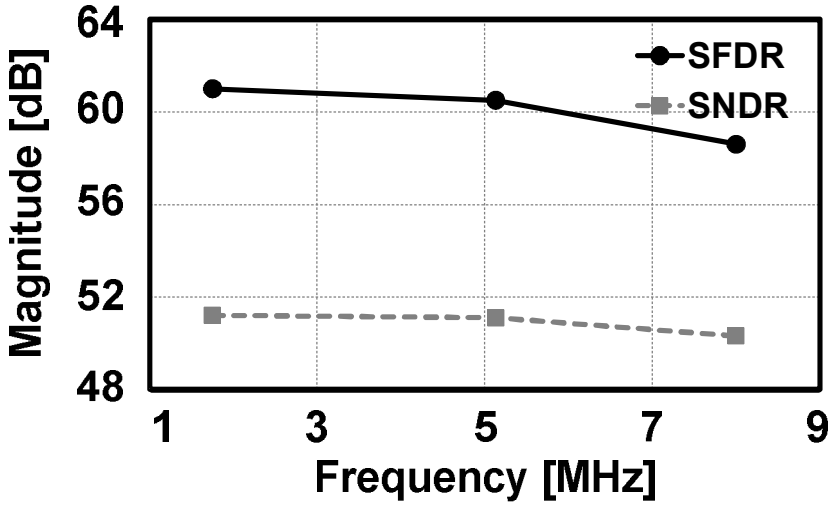


Fig. 3-24. Input frequency sweep at 17.5MS/s

Process	CMOS 0.13 μm	
Active Area (single)	500x1550 (500x700) μm^2	
Sampling Rate	17.5 MS/s	
Power (single channel)	Analog	66 μW@1.2V
	Digital	388 μW@1.2V
	Total	438 μW@1.2V
ENOB	8.3 bits	
FOM	79 fJ/Step	

Table 3-1. Performance summary of MTS SAR ADC

linearity of the capacitor DAC from the post simulation. Due to the capacitor mismatch by the parasitic capacitance formed by the long bottom plate routing of the capacitor for (MSB–4) bit and the common top plate, the measured linearity was limited to 8b for ±1LSB DNL.

The total power consumption of the single ADC is 438μW under 1.2V supply at 17.5MS/s. The power consumption from the digital block is 388μW, and the analog is 66μW. The power consumption for the external reference driver is not counted. The measured ENOB is 8.3b, and the figure of merit is 100fJ/step at 17.5MS/s. The performance of the chip is summarized in Table 3-1.

3.6.2 Measurement for efficiency of metastable-then-set algorithm

The key motivations of MTS SAR ADC are to solve the metastability of asynchronous SAR ADC and reduce the digital power about 10% for 10b resolution. It is performed to sweep the externally controlled current (I_{EXT}) in the metastability detector (MD) as shown in Fig. 3-14 to know the power efficiency of MTS SAR ADC. Measured power and performance are listed up in table 3-2.

$I_{EXT\ :\ MD}$ (1:6)		t_{MTS} [ns]	SNDR [dB]	$I_{comparator}$ [uA]	I_{analog} [uA]	$I_{digital}$ [uA]	I_{TOT} [uA]
I_{EXT} [uA]	I_{MD} [uA]						
5	30.0	1.10	51.1	20	55.0	310	365
6	36.0	0.92	51.1	20	62.0	310	372
7.2	43.2	0.76	51.7	20	70.7	301	372
9.1	54.6	0.60	50.0	20	83.7	292	376
10.5	63.0	0.52	47.5	20	93.5	275	368
11.5	69.0	0.48	40.0	20	100.0	265	365

Table 3-2. Power measurement of a MTS SAR ADC

When the I_{EXT} is swept from 5μA to 11.5μA, t_{MTS} ranges from 1.1ns to 0.48ns which is expressed as Eq. 3-2. It is the lapse of time of a comparator to ought to complete a comparison without metastability. Fig. 3-25 shows the dynamic performance according to a change of I_{MD}. The analog current (I_{analog}) is the sum of I_{EXT}, I_{MD} and $I_{comparator}$. As the I_{EXT} increases, the metastability occurs more frequently because the given time (t_{MTS}) for an exact decision is reduced. This has a bad effect on accuracy of the MTS SAR ADC, and therefore a SNDR is dropped gradually.

$$t_{MTS} = \frac{C_{MD} \cdot V_{TH\_meta}}{I_{MD}} \quad \text{(Eq. 3-2)}$$

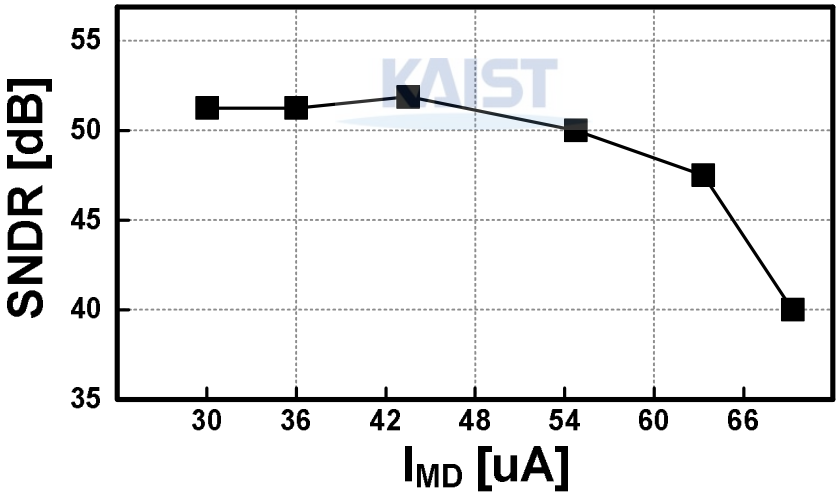


Fig. 3-25. Dynamic performance according to a change of I_{MD}

As you can see in the table 3-2, the more the I_{EXT} increases, the less the digital current ($I_{digital}$) is consumed. However, the total current (I_{TOT}) does not decrease but nearly is

unchanged since the I_{analog} increases simultaneously. It is a burden of metastable detector.

$I_{EXT:MD}$ (1:3)		t_{MTS} [ns]	SNDR [dB]	$I_{comparator}$ [uA]	I_{analog} [uA]	$I_{digital}$ [uA]	I_{TOT} [uA]
I_{EXT} [uA]	I_{MD} [uA]						
2.5	30.0 → 7.5	1.10	51.1	20	55.0 → 30.0	310	340
3	36.0 → 9.0	0.92	51.1	20	62.0 → 32.0	310	342
3.6	43.2 → 10.8	0.76	51.7	20	70.7 → 34.4	301	336
4.55	54.6 → 13.7	0.60	50.0	20	83.7 → 38.2	292	331
5.25	63.0 → 15.8	0.52	47.5	20	93.5 → 41.0	275	316
5.75	69.0 → 17.3	0.48	40.0	20	100.5 → 43.0	265	308

Table 3-3. Calculated power for a MTS SAR ADC with reduced I_{analog}

To reduce this overload, if reference current and the size ratio of current source are down by half, each current is summarized as following table 3-3. Next Fig. 3-26~27 compare the prototype ADC and reduced current design example. Fig. 3-26 plots the analog current, the digital current and the reduced analog current of design example

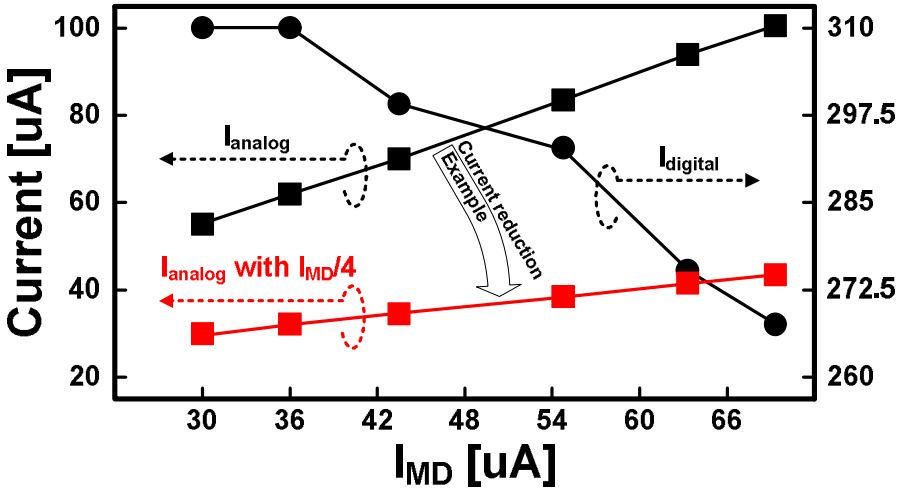


Fig. 3-26. Analog and digital current consumption according to a change of I_{MD}

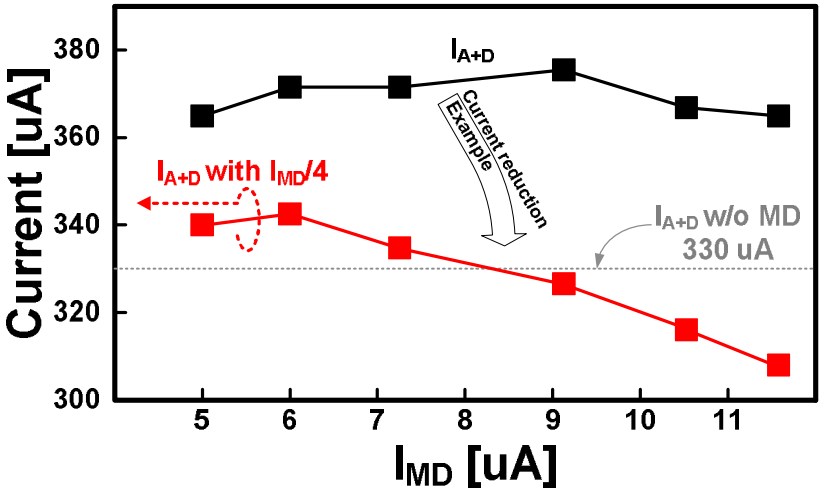


Fig. 3-27.Total current consumption according to a change of I_{EXT}

separately. In the design example, an upturn in the I_{analog} becomes sluggish, and an absolute I_{analog} also is reduced by more than half.

3.7 Summary

A dual channel asynchronous SAR ADC for low power communication systems has been implemented with two power-efficient conversion algorithms. The straightforward DAC control method saves DAC power consumption by removing unnecessary switch-back operations and by reducing the capacitor size by half. The MTS algorithm reduces its power consumption from the digital logic and is verified by measurement its efficiency. The DAC synchronization of dual-channel ADC minimizes channel isolation under the shared reference condition.

4.Power Efficient Algorithms: ADEC SAR ADC

Abstract: A speed-enhanced 10b asynchronous SAR ADC with multistep addition-only digital error correction (ADEC) is presented in this chapter 4. Three virtually divided sub-DACs have a 0.5 LSB over-range between stages owing to additional decision phases incorporating DAC rearrange only. These redundancies make it possible to guarantee 10b linearity with a 37% speed enhancement under a 4b-accurate DAC settling condition at MSB decision. A prototype ADC was implemented in CMOS 0.13μm technology. The chip consumes 550μW and achieves a 50.6dB SNDR at 40MS/s under a 1.2V supply. The figure-of-merit (FOM) is 42fJ/conv.step.

This chapter is organized as follows. The concept and operation of the proposed addition-only digital error correction (ADEC) will be described with previous similar works in section 3.1. Section 3.2 will show the implementation of a 10b ADEC SAR ADC. Section 3.3 will show the measurement results, and the summary will be described in section 3.4.

4.1 Addition-only digital error correction (ADEC) technique

As the most time-consuming process in medium-to-high resolution SAR ADCs is the DAC settling, the time for a complete A/D conversion can be significantly reduced if the

accuracy requirement for DAC settling can be relaxed. As reported in several papers [02.ISSCC.Kuttner, 06.IEEJ VLSI workshop.Hotta, 10.ISSCC.Liu, 09.ASSCC.Chen], redundancy in code decisions makes this possible. Contrary to hardware-burdened earlier methods [Kuttner, Hotta], the recent publications [Liu, Chen] show that error correction methods based on binary DAC operations can greatly lessen the hardware overhead. However, the additional capacitors in DAC for redundancy in Liu's ADC and less systematic digital operations in Liu's ADC, and Chen's ADC leave room for further improvement.

Prior to the binary DAC based techniques mentioned above, the authors reported a SAR ADC oriented digital error correction algorithm which required only the addition of a simple digital code with no DAC burden [09.EL.Cho.]. This section presents a speed-enhanced prototype SAR ADC that is built on this idea with advanced hardware implementation.

4.1.1 Motivation

The operation of an ideal SAR ADC with sampled input ($6.5/16V_{REF}$) can be explained with Fig. 4-1 which shows its V_{DAC} waveform and every determined input ranges (DIRs) indicated by gray bars. The obtained exact output code is '0110'. However, if the DAC settling is not enough as having the error of 1.8LSB at the first settling, the wrong MSB ('1') is decided as shown in Fig. 4-2. Because this wrong decision makes the first DIR be found incorrectly as upper half gray bar, the final digital code is also wrong as '1000' by 2LSB difference, even though the rest bit decisions are correct. As you can see, the incomplete DAC settling can cause the code error as much as the DAC settling error

amount.

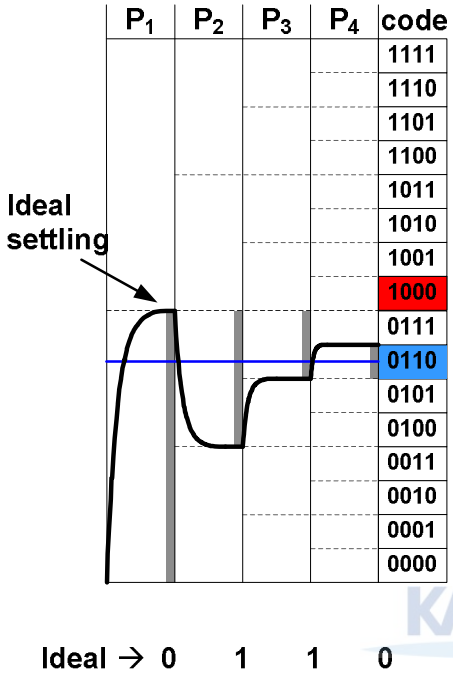


Fig. 4-1. V_{DAC} trace about an ideal SAR ADC operation

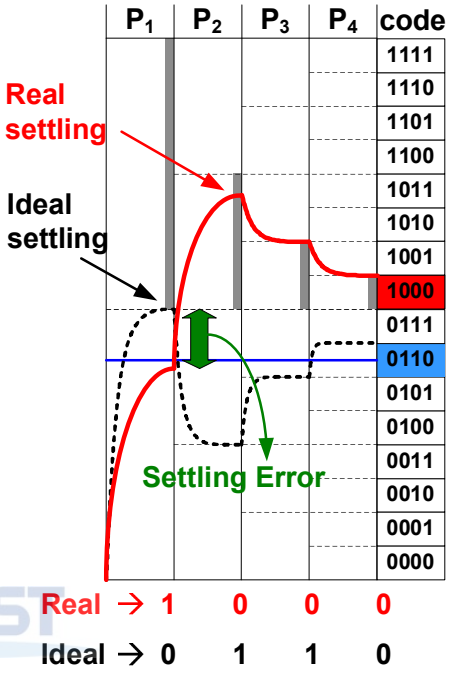


Fig. 4-2. V_{DAC} trace about real SAR ADC operation with DAC settling error

4.1.2 Previous solutions for DAC settling requirement

Solving the incomplete DAC settling, previous works will be reviewed using this section as mentioned in the introduction of this chapter 4 [02.ISSCC.Kuttner, 06.IEEJ VLSI workshop.Hotta, 09.ASSCC.Chen, 10.ISSCC.Liu].

4.1.2.1 Non-binary SAR ADC [02.ISSCC.Kuttner]

For this converter, the result of the first decision does not mean that the input voltage is greater or smaller than half of the reference voltage. A logical one ('1') means only that the input voltage is greater than half the reference voltage minus some error tolerance defined by sub-radix number (e.g. 12.7%). So the next comparison is not done with 256 or 768. A '1' means that the code is greater than 512 minus 12.7%, so the next comparison is with the middle of the next range 447…1024 = 735. A '0' means, that the code is smaller than 512 plus 12.7%, so the next comparison is with 288. Therefore error of the first conversion can be up to 65LSB of the 10b code. The bit weights (447 251 142 80 45….) are stored in a ROM.

The above paragraph is describing the operation of non-binary SAR ADC. The some error mentioned is dominantly induced by incomplete DAC settling. In Fig. 4-3, non-binary SAR ADC has the redundancy (12.7%) calculated in the digital part (ROM and AU) of the converter. Therefore, unlike binary searching algorithm (SAR), the DIRs are extended as a certain percent (12.7%) in the non-binary SAR ADC. This gives a change to fix a previous wrong decision. This is the reason why the non-binary SAR algorithm makes SAR ADCs faster. As seen in Fig. 4-4, a non-binary SAR ADC has many

additional blocks such as ROM, AU, flip-flops, decoder and MUX.

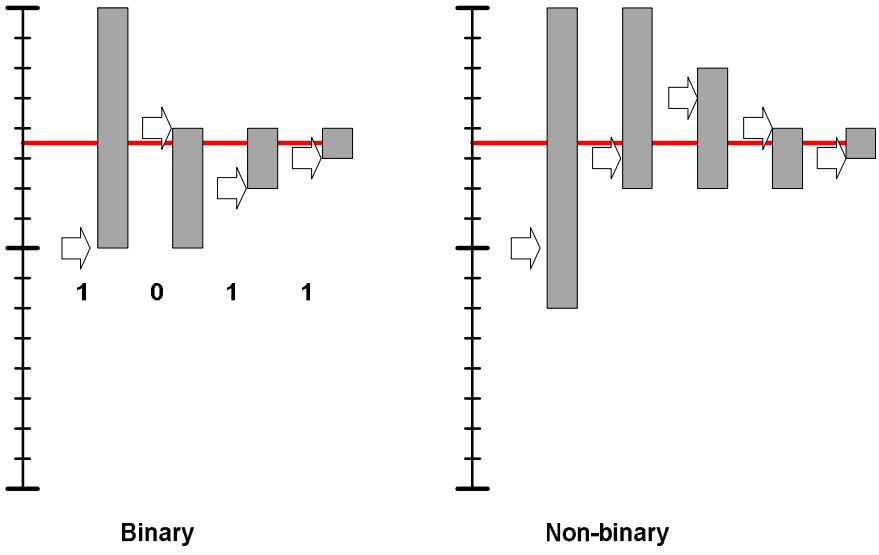


Fig. 4-3. Excerpted figure from Kuttner's paper: comparison binary and non-binary

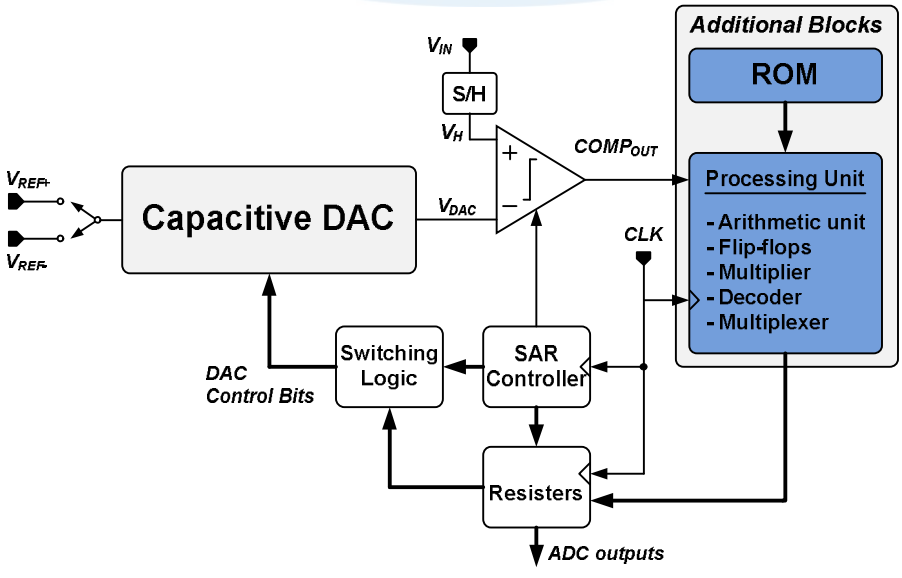


Fig. 4-4. Block diagram of non-binary SAR ADC

4.1.2.2 Binary error correction SAR using 2b per conversion concept [06.IEEJ VLSI workshop.Hotta]

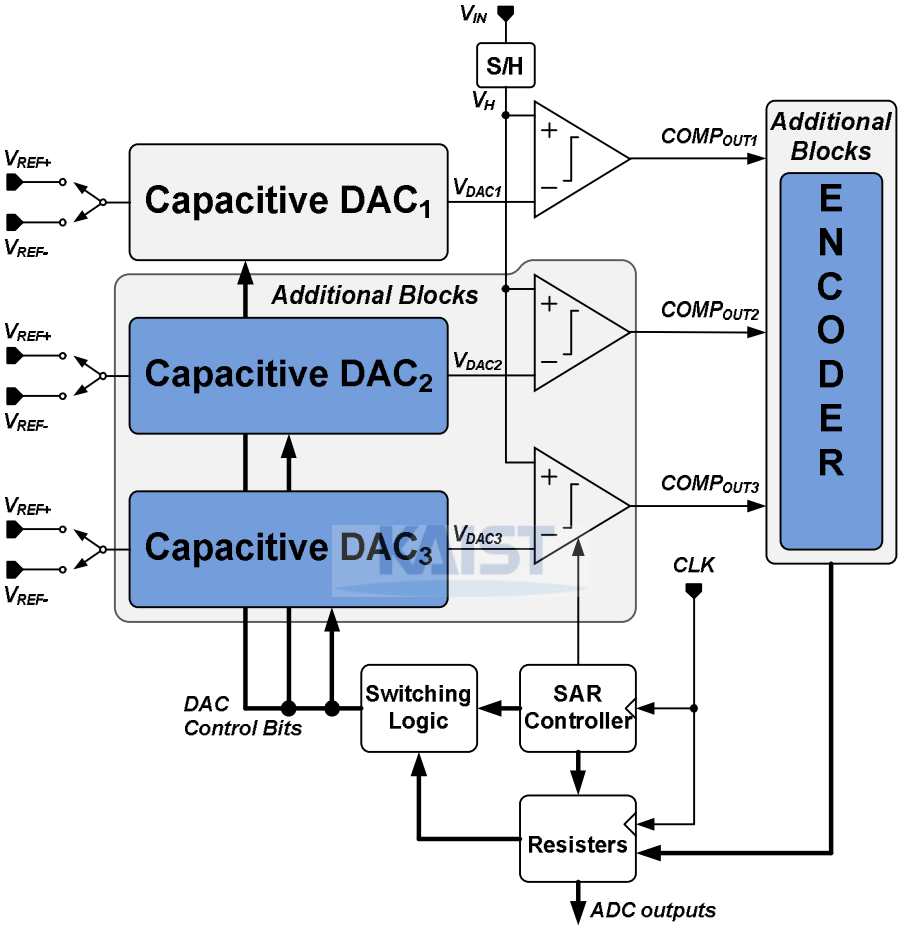


Fig. 4-5. Binary error correction SAR ADC based on 2b/Conv.

The proposed SAR ADC has three comparators, and it obtains 2-bit data in the first comparison step and 1-bit data in each subsequent steps. Thus, N comparisons result in

(N + 1) bit digital data, and the redundancy of the three comparators is used to improve the immunity against DAC settling error. However, additional blocks are too large.

4.1.2.3 Sub-range SAR ADC [09.ASSCC.Chen]

One example of sub-range binary search algorithm is shown in Fig.4-6. In this example, the analog input level is equivalent to digital word 2020. After tracking, like conventional SAR ADC, the first decision point, 2048, is 1/2 of full input range. Under the condition of incomplete DAC settling, an error decision is assumed to occur and the comparator result is 1 instead of 0. It makes the 2nd decision point form at 3072 point. Since the residue voltage for the 2nd decision is big enough, the latch comparator can make correct decision even if the capacitor array output is not settled. The search sequence repeats in the same manner for the rest of the coarse conversion. Starting from the 7th bit resolving, the capacitor array output has longer time settling and larger gain amplifying; therefore, the analog circuit has higher accuracy for fine conversion. No error is allowed afterwards. Before the 7^{th} decision is made, the input is between 2143 and 2016. The 7^{th} decision point is 2080, and the comparator result should be 0. The 7th result indicates the input should be between 2080 and 2016. The error decision is only possibly made in 2048 during coarse conversion. Then, it is needed to re-examine the 2048 decision point for the 8th bit resolving. The 8th bit resolving result should be 0.

The re-examination process is the redundancy. One difference between this re-examination and redundancy of a non-binary SAR ADC is that the above re-examination is just added in a designed specific decision phase, while the redundancy of a non-binary SAR ADC is usually added every phases. One burden is that this algorithm should

implement a digital subtraction function to perform its digital error correction.

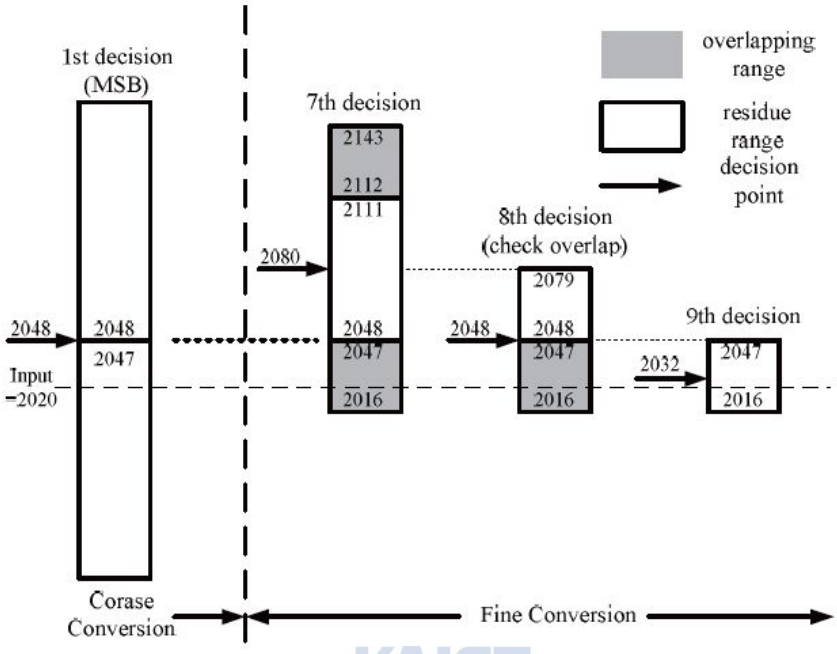


Fig. 4-6. Excerpted figure from Chen's paper: 12b sub-range binary search algorithm

4.1.2.4 Binary scaled error compensation SAR ADC [10.ISSCC.Liu]

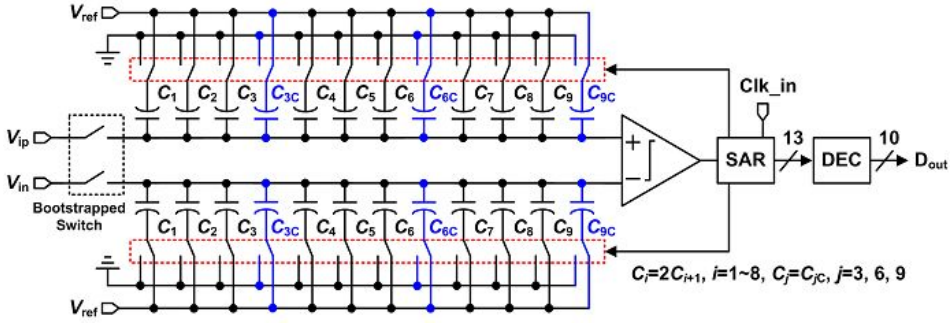


Fig. 4-7. Excerpted figure from Liu's paper: block diagram of binary scaled error compensation SAR ADC

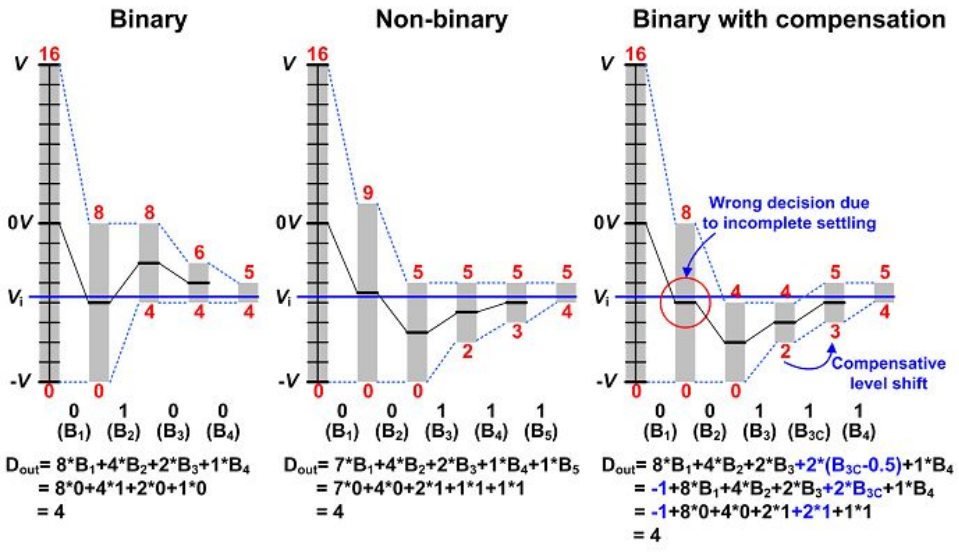


Fig. 4-8. Excerpted figure from Liu's paper: binary with compensation algorithm

Fig. 4-7 shows the excerpted block diagram of binary scaled error compensation SAR ADC, and Fig. 4-8 shows the concept of binary scaled error compensation. Fig. 4-8 is the same with Fig. 4-6 of sub-range binary search algorithm conceptually, because it is said that the redundancy is just added in a designed specific decision phase which is 'B_{3C}' in Fig. 4-8. The drawback of the above ADC is that it has the additional two capacitors to give the redundancy: 64C and 8C as shown in Fig. 4-7.

4.1.3 Understanding ADEC SAR algorithm

The addition-only digital error correction (ADEC) SAR algorithm is made to relax the DAC settling requirement in common with previous four error correction algorithms. As mentioned in section 4.1, the ADEC SAR algorithm can be implemented with very less

hardware burden than prior works and has power efficient effects at the same time.

To deeply understand the ADEC SAR algorithm, the operation will be explained from two different angles; the explanation in terms of a SAR ADC itself and explanation by the analogy of digital error correction in two-step and SAR ADCs.

4.1.3.1 Explanation in terms of a SAR ADC itself

The figures from 4-9 to 4-15 illustrate the operation of a 4b ADEC SAR ADC. First, Fig. 4-9 shows the sampled input level (6.5/13), DAC switches status and the schematic of an example SAR ADC. V_{REF+}, V_{CM}, and V_{REF-} are assigned by 1V, 0.5V and 0V, respectively. In the Fig. 4-10, the V_{SHIFT} is generated by the largest capacitor of the sub-DAC_2, and its amount is 0.5 coarse LSB size ($0.5LSB_1 = 1/8V_{REF}$). The correct MSB is fortunately

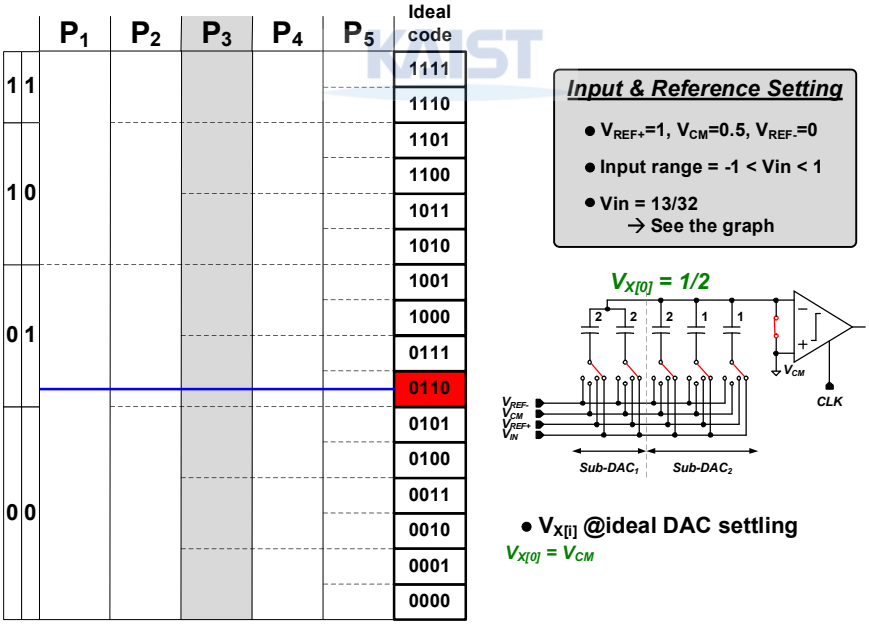


Fig. 4-9. ADEC SAR algorithm: sampling

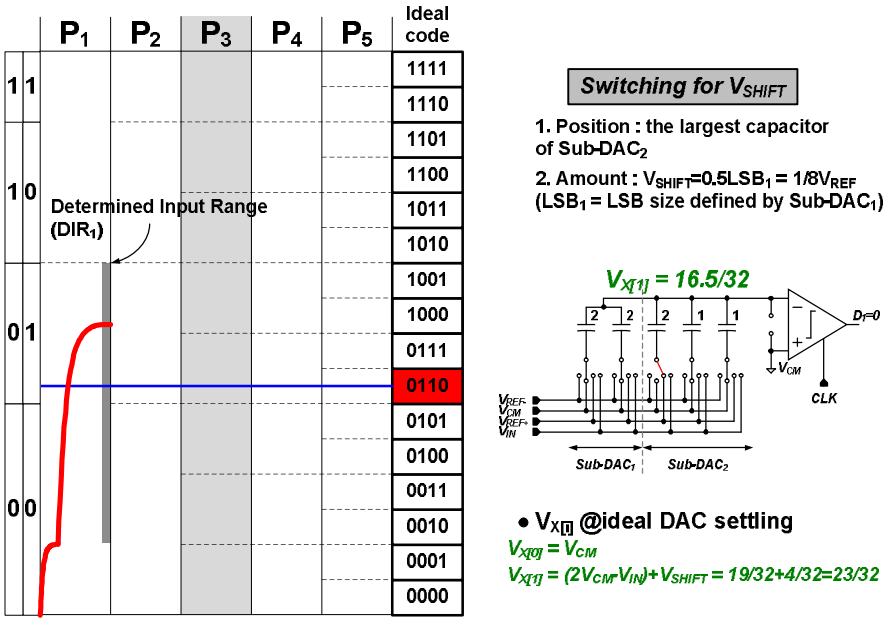


Fig. 4-10. ADEC SAR algorithm: MSB decision

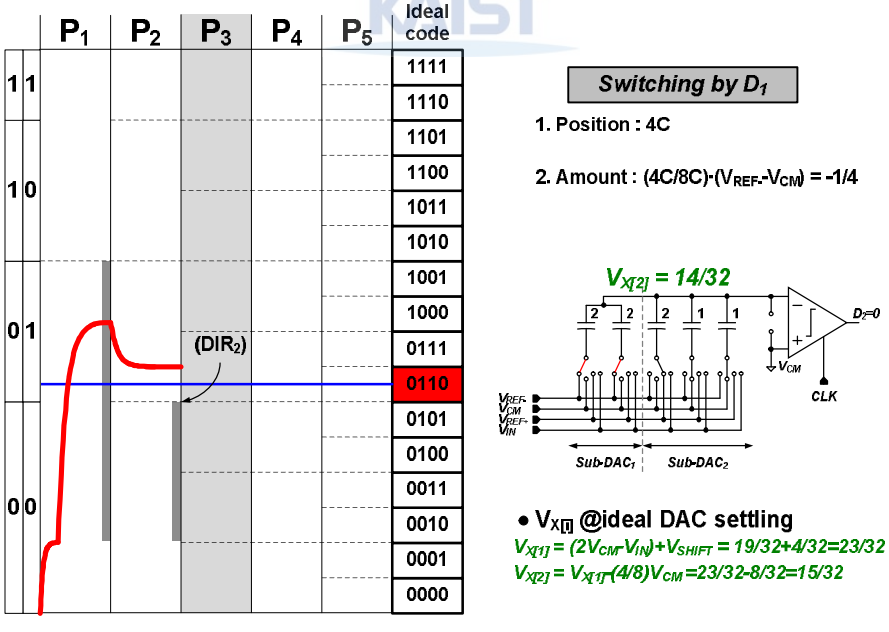


Fig. 4-11. ADEC SAR algorithm: MSB-1 decision

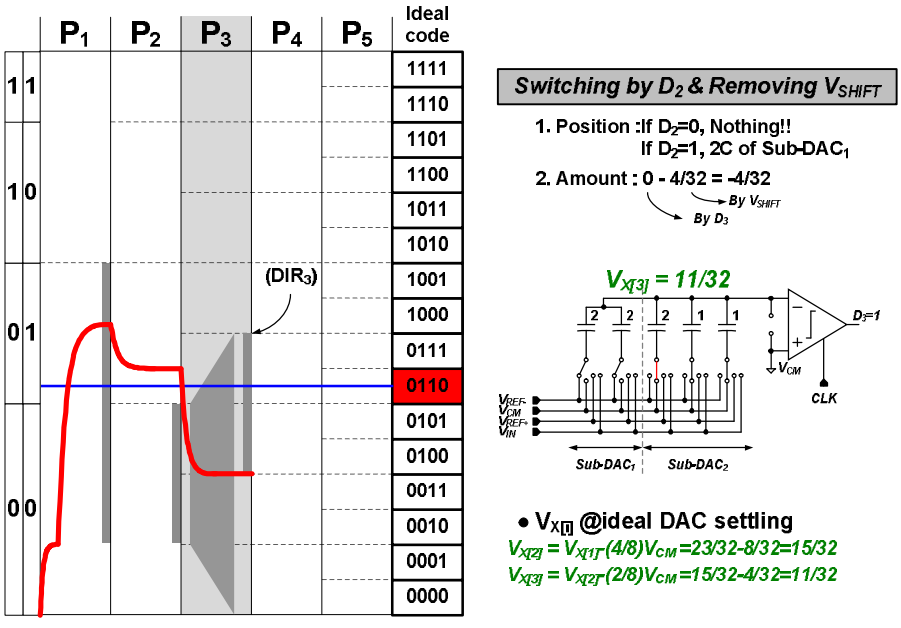


Fig. 4-12. ADEC SAR algorithm: redundancy decision

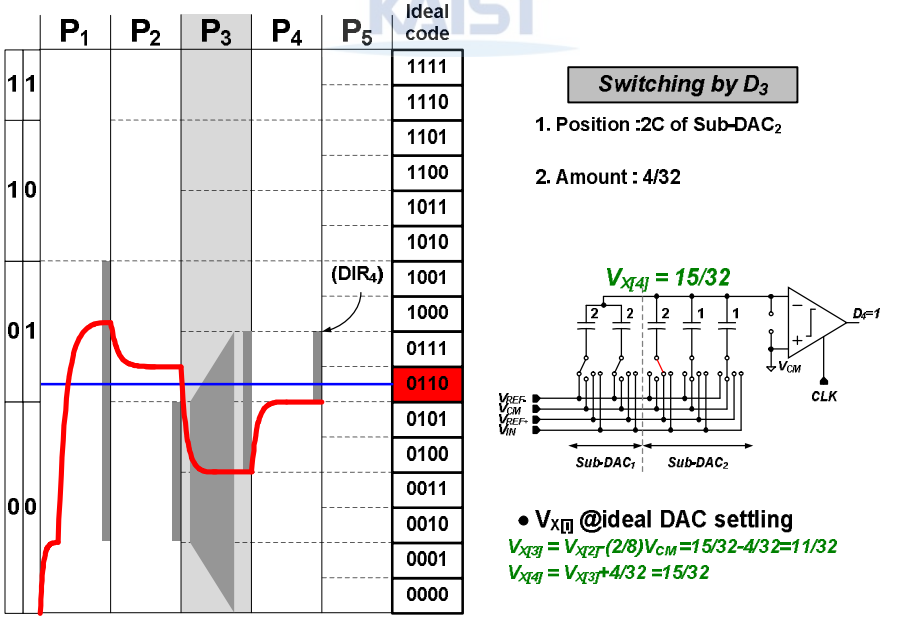


Fig. 4-13. ADEC SAR algorithm: LSB+1 decision

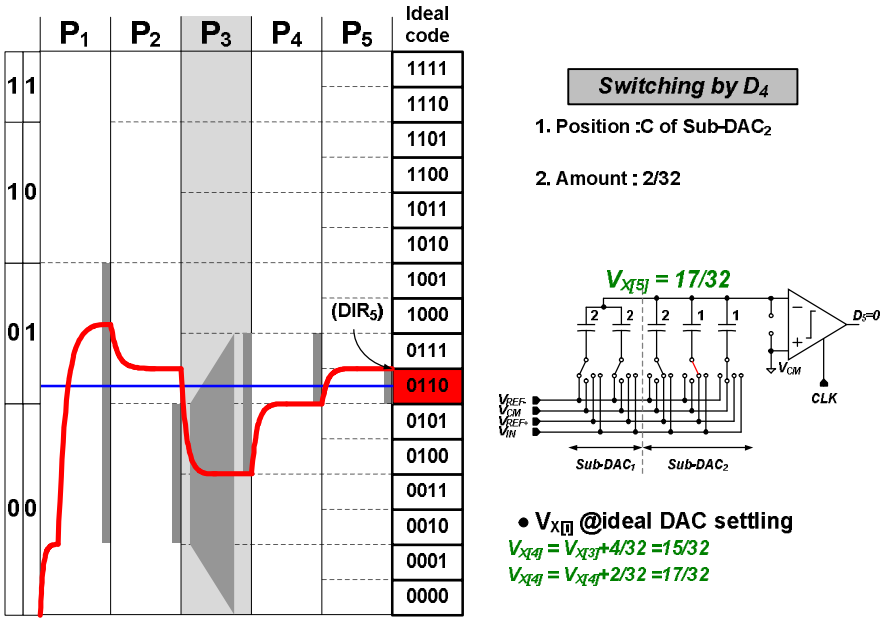


Fig. 4-14. ADEC SAR algorithm: LSB decision

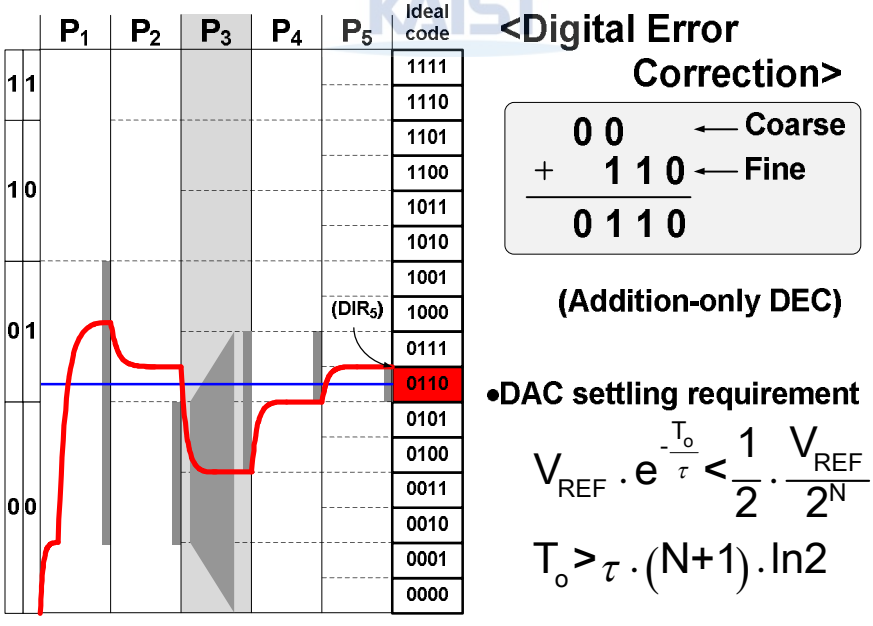


Fig. 4-15. ADEC SAR algorithm: digital addition for ADEC

obtained even though the first DAC settling error is nearly 2 LSB. The DAC level has to settle to the center of DIR_1 by using the MSB code, but it cannot go to that center due to incomplete DAC settling as shown in Fig.4-11. In this phase, the second digital output indicates wrong DIR_2. In other words, the V_{IN} is out of the DIR_2. The DIR_2 must be extended to cover the V_{IN}. The next P_3 is the redundancy phase to extend the DIR_2, and, in its phase, only elements of sub-DAC_1 after eliminating the V_{SHIFT} are rearranged according to the LSB of coarse code as shown in Fig. 4-12. Details of the rearrangement will be described at the next section 4.2 (Implementation of 10b ADEC SAR ADC). After performing the rest bit decisions as shown in Fig. 4.13~14, we can get two type digital codes; coarse code and fine code. They are added with 1b overlap. The same final code with ideal one will be achieved as '0110' even though the DAC settling is incomplete, so we can say that the ADEC algorithm enhances the sampling frequency. For example, based on an exponential DAC settling behavior, a conventional 10b SAR ADC requires '76τ' for DAC settling while a proposed 6b-5b ADEC SAR ADC requires only '53τ' including one redundant decision phase. It makes SAR ADCs about 30% faster as shown in Fig. 4-15.

The whole ADEC progress will be discuss about 10b real design one more time in detail.

4.1.3.2 Explanation by analogy of digital error correction in two-step and SAR ADCs

Fig. 4-16 shows an analogy of addition-only digital error correction (ADEC) algorithms in a two-step ADC and a SAR ADC using a 4b example. As with the two-step ADC, the decision procedure in the SAR ADC is virtually divided into the two steps of a 2b-coarse and a 3b-fine decision with 1b redundancy (2b-3b architecture). Both ADCs have coarse decision thresholds of $\pm 1/4\ V_{REF}$ which are deviated from those of a

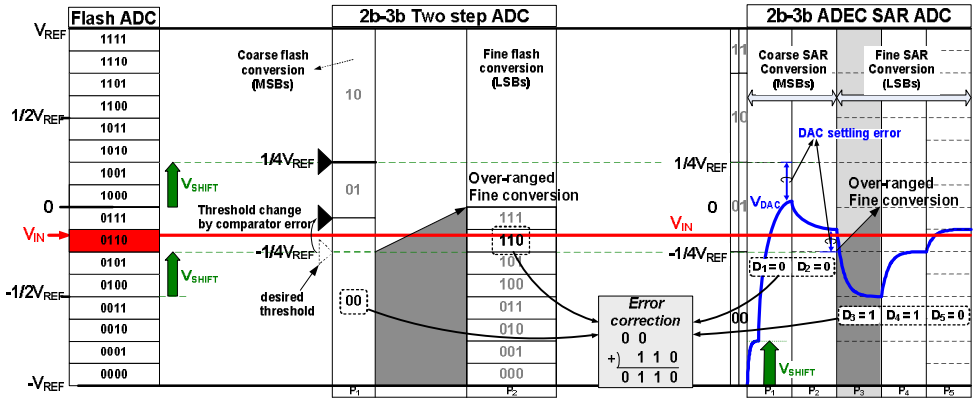


Fig. 4-16. Analogy of digital error correction in two-step and SAR ADCs

flash ADC by 0.5LSB of coarse resolution (= V_{LO}) for the ADEC operation. In SAR ADC, this threshold shift can be realized by starting the MSB decision with DAC level (V_{DAC}) at +1/4 V_{REF}, not the conventional center level.

There can be comparator errors in a coarse flash ADC in a two-step ADC and DAC settling errors in a SAR ADC. This is depicted in Fig. 4-16 by the comparator position shift (black triangle) and slow-settling V_{DAC} waveform. In the example, for a given input (V_{IN}), both ADCs generate incorrect MSBs of 00. In the following fine conversion process, the two-step ADC extends its reference range by a 0.5 LSB of coarse conversion resolution for decision redundancy. It then determines the 3b LSBs of 110 with an ideal fine flash ADC. Finally, the error-corrected full code of 0110 is achieved by adding MSBs and LSBs with one-bit overlap.

Redundancy in SAR ADC is implemented by inserting an additional decision step, P3 in the example. The desired fine conversion range is determined by the determined MSBs, as with the two-stage ADC, and the fine conversion starts by placing the V_{DAC} at

the center of it. Here, then, all of the threshold levels for coarse and fine decisions in the ADEC SAR are identical to those in a two-step ADC. Accordingly, as the effect of comparator error in the coarse ADC can be corrected in a two-step ADC by virtue of digital error correction, the code error during the coarse SA conversion occurring as a result of incomplete DAC settling is curable in the ADEC SAR ADC as long as the error amount is less than 0.5 LSB of the coarse resolution. This relaxed requirement of a DAC settling can speed up the SAR ADC, even with an increased number of conversion cycles.

4.1.4 Structure optimization

In the ADEC SAR ADC design, there must be a trade-off between the reduced DAC settling requirement and the time overhead due to the increased number of decision cycles. Thus, the ADEC SAR ADC can be designed with multiple redundant decision phases to optimize the conversion speed. To determine the speed-optimized architecture for the 10b ADC, the conversion speeds of several architectures have been compared with conventional designs. The total required time for 10b conversion was estimated, including all of the required times such as the input sampling time, DAC settling time, and comparator latching time. Additionally, the result was normalized to the speed of a conventional SAR ADC which has no redundancy. For this estimation, the input sampling time and average comparator decision time were assumed to be 4ns and 130ps, respectively, based on the proposed design and on the results of an earlier study [06.ISSCC.Chen]. Note that this work has an asynchronous SAR controller for further

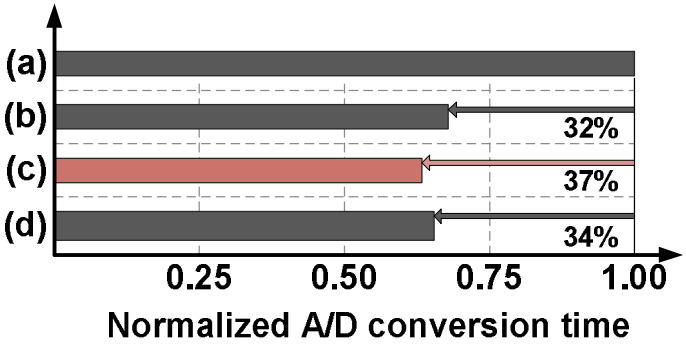


Fig. 4-17. Conversion time comparison for various SAR ADC architectures:

(a) conventional, (b) 6b-5b, (c) 4b-4b-4b, (d) 4b-3b-3b-3b structures

speed enhancement. Fig. 4-17 shows the comparison results with several sample architectures, showing 6b-5b with 1b redundancy, 4b-4b-4b with 2b redundancies, and 4b-3b-3b-3b with 3b redundancies. The comparison shows that the 4b-4b-4b architecture is the optimum choice among all, with a speed enhancement of 37%.

4.1.5 Effects of ADEC technique

A behavioral simulation was conducted to compare the dynamic linearity of the architectures mentioned above under an operating speed which guarantees only 4b-accurate DAC settling in MSB decision. Fig. 4-18 shows the simulation result. This figure shows that the conventional, and 6b-5b architectures have considerably large INL peaks, whereas the optimum choice shows less than 0.3 LSB errors. This demonstrates the effectiveness of the speed optimized 4b-4b-4b ADEC SAR ADC.

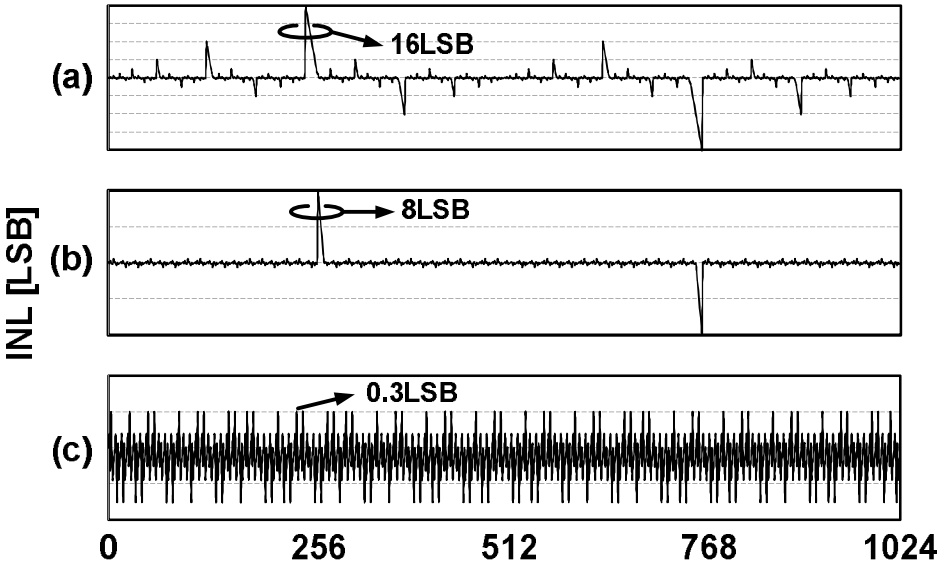


Fig. 4-18. INL comparison of differently configured SAR ADCs under 4b DAC settling: (a) conventional, (b) 6b-5b, (c) 4b-4b-4b structures

4.2 Implementation of 10b ADEC SAR ADC

4.2.1 Block diagram

Fig. 4-19 shows a single-ended version block diagram. The notable point is that sub-DACs are virtually divided into three stages as if an ADEC SAR ADC is the multi-step ADC like a pipeline ADC.

4.2.2 Timing diagram

The timing diagram for an ADEC SAR ADC is exactly the same with Fig. 3-18 in the section 3.4 of the chapter 3.

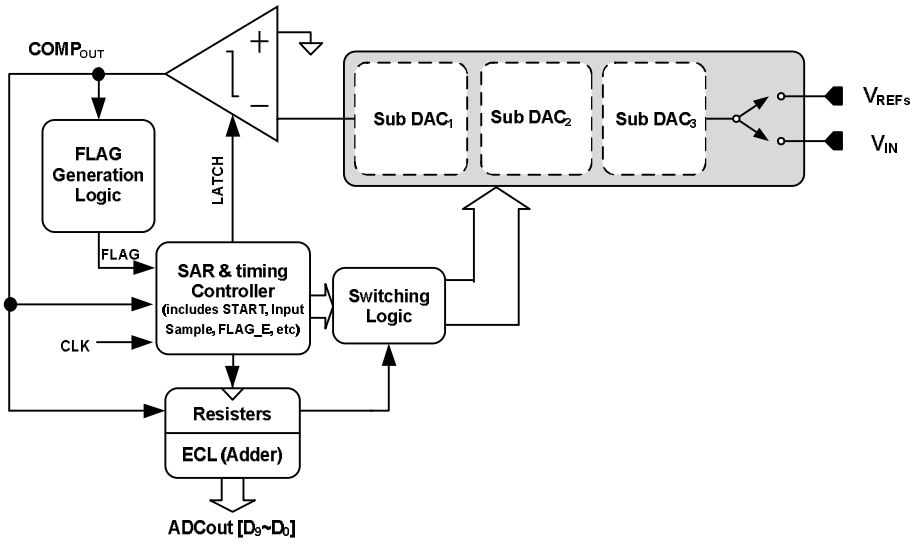


Fig. 4-19. Block diagram of an asynchronous ADEC SAR ADC

4.2.3 10b DAC structure and operation

A prototype 10b SAR ADC with 4b-4b-4b architecture was implemented. A single-ended version schematic of its DAC and comparator are shown in Fig. 4-20 with its switching table (real design is in fully differential) for a sampled input of +27/1024 V_{REF}. The binary-weighted capacitor DAC was virtually segmented into 3 sub-DACs (sub-$DAC_{1\sim3}$) for the ADEC operations. Here, only a 9b binary weighted DAC was designed for 10b SAR ADC by using a straightforward switching method as mentioned in section 3.1. The MSB is determined by connecting the bottom plates of all capacitors to the reference common level (V_{CM}) [09.ASSCC.Chen]. Thus, the DAC size is reduced by half, and as is the switching power consumption. The capacitors in sub-DAC_1 and sub-DAC_2 are split into two sub-capacitors ($C_i = C_{i\_1}$ and C_{i_2}, i = 4~9) to simplify the capacitor switching logic. This is explained later.

※ *DAC Switching table (V_{REF+} = +, V_{CM} = 0, V_{REF-} = -)*

	C_9		C_8		C_7		C_6		C_5		C_4	C_3	C_2	C_1	C_0	Code	Remarks
	2	1	2	1	2	1	2	1	2	1	2	1					
P_0	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}		
P_1	0	0	0	0	0	0	+	+	0	0	0	0	0	0	0	D_{11} = 1	Input Sampling
P_2	+	+	0	0	0	0	+	+	0	0	0	0	0	0	0	D_{10} = 0	Apply the V_{SHIFT1}
P_3	+	+	-	-	0	0	+	+	0	0	0	0	0	0	0	D_9 = 0	
P_4	+	+	-	-	-	-	+	+	0	0	0	0	0	0	0	D_8 = 0	
P_5	+	+	-	-	-	-	0	0	0	0	0	+	0	0	0	D_7 = 0	Redundancy I
P_6	+	+	-	-	-	-	-	-	0	0	0	+	0	0	0	D_6 = 0	
P_7	+	+	-	-	-	-	-	-	-	-	0	+	0	0	0	D_5 = 0	
P_8	+	+	-	-	-	-	-	-	-	-	-	+	0	0	0	D_4 = 1	
P_9	+	+	-	-	-	-	-	-	-	-	+	0	0	0	0	D_3 = 0	Redundancy II
P_{10}	+	+	-	-	-	-	-	-	-	-	+	-	0	0	0	D_2 = 1	
P_{11}	+	+	-	-	-	-	-	-	-	-	+	-	+	0	0	D_1 = 0	
P_{12}	+	+	-	-	-	-	-	-	-	-	+	-	+	-	0	D_0 = 1	

MSBs (4bits)

IMBs (4bits)

LSBs (4bits)

Fig. 4-20. Virtually segmented (4b-4b-4b) 10bit ADEC SAR ADC and its switching table

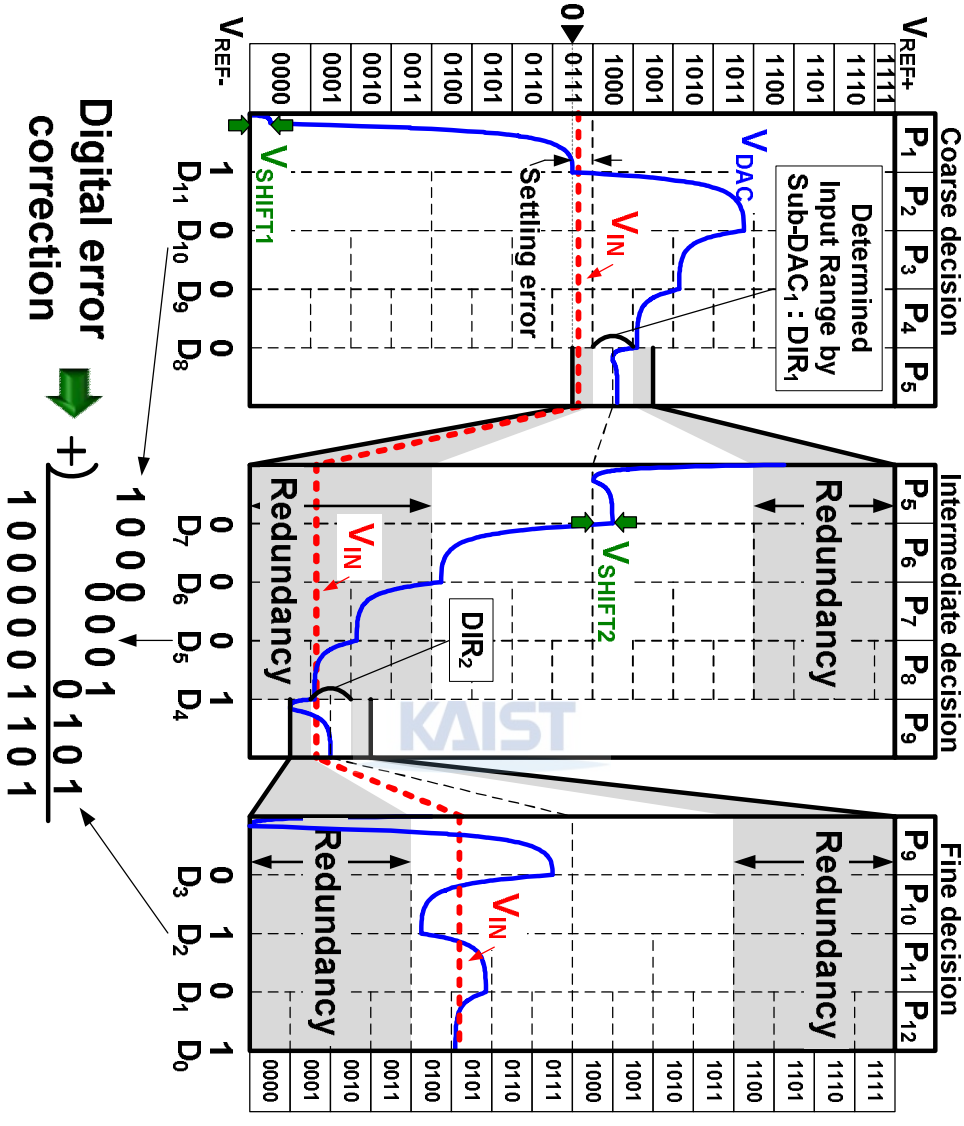


Fig. 4-21. DAC waveform with incomplete settling

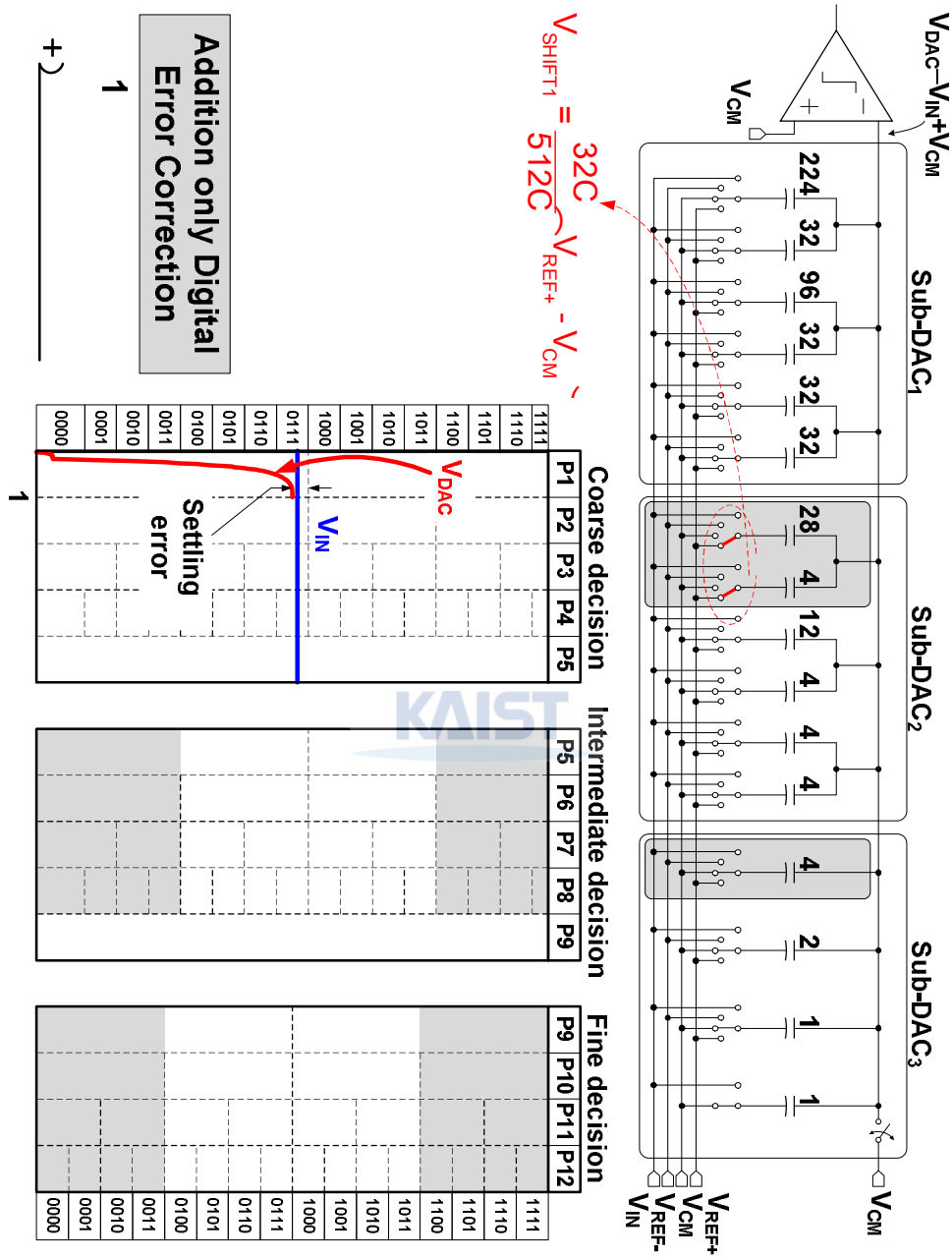


Fig. 4-22. Switching status of P_1 phase and DAC waveform

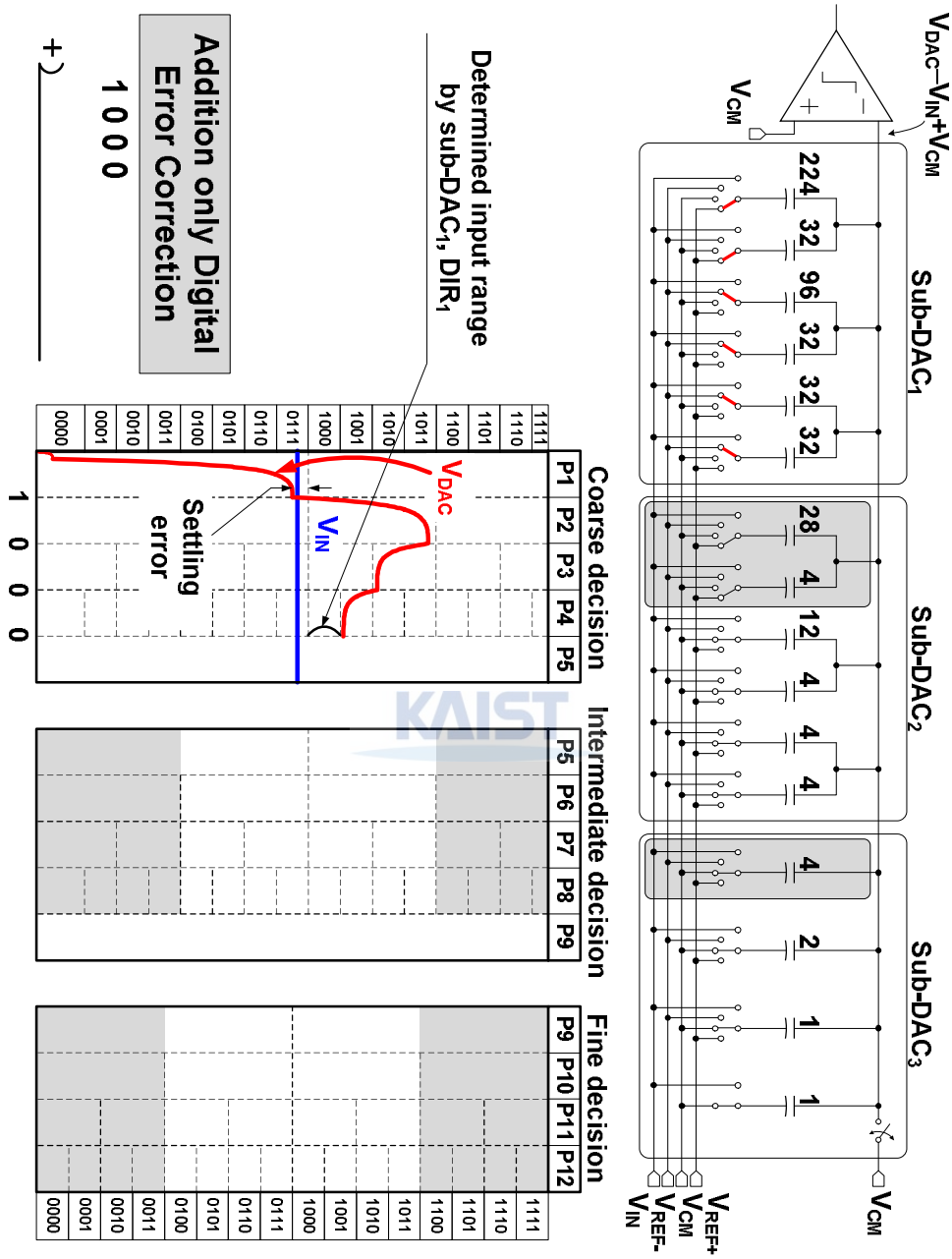


Fig. 4-23. Switching status by P_4 phase and DAC waveform

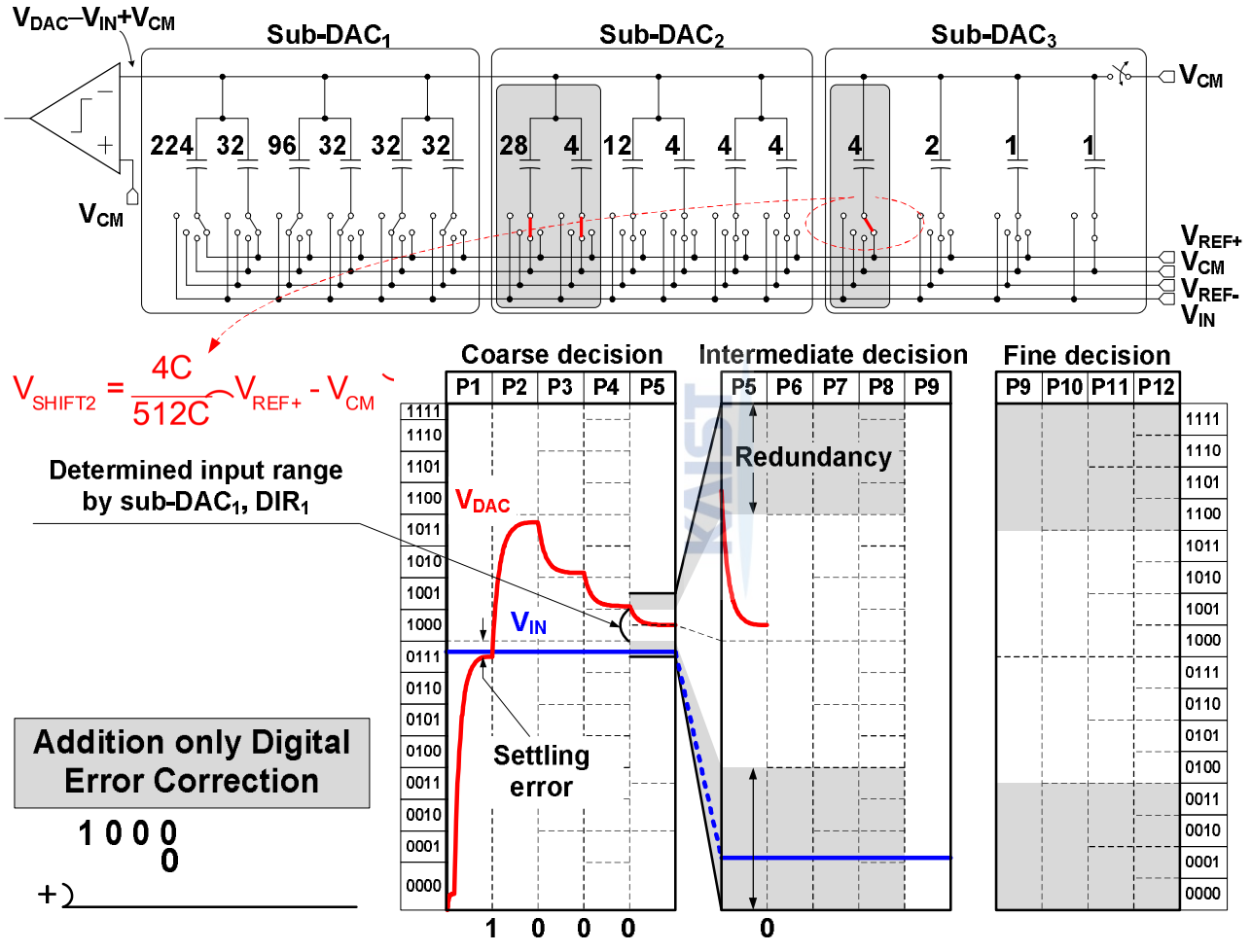


Fig. 4-24. Switching status by P_5 (redundant) phase and DAC waveform

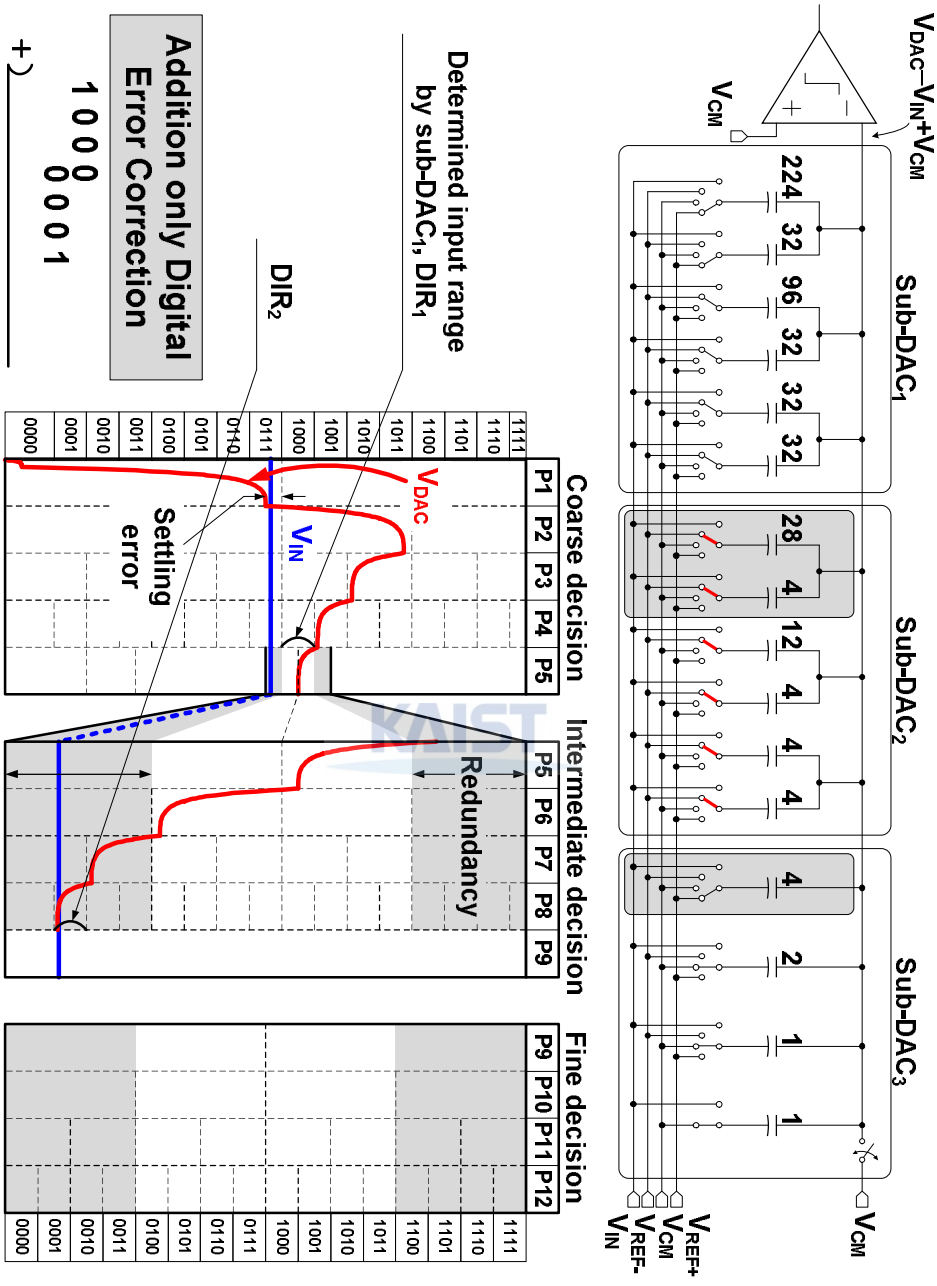


Fig. 4-25. Switching status by P_8 phase and DAC waveform

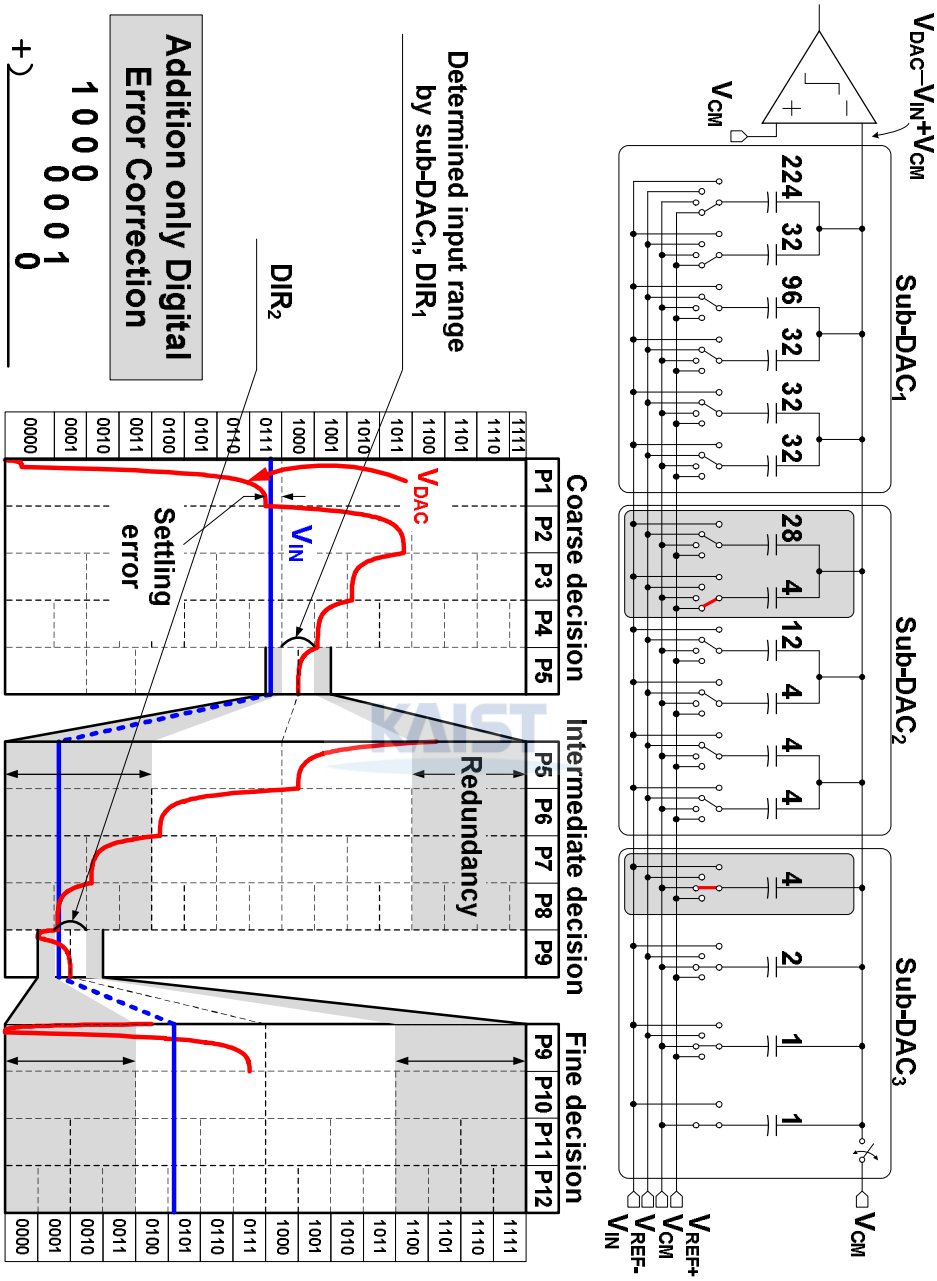


Fig. 4-26. Switching status by P_9 (redundant) phase and DAC waveform

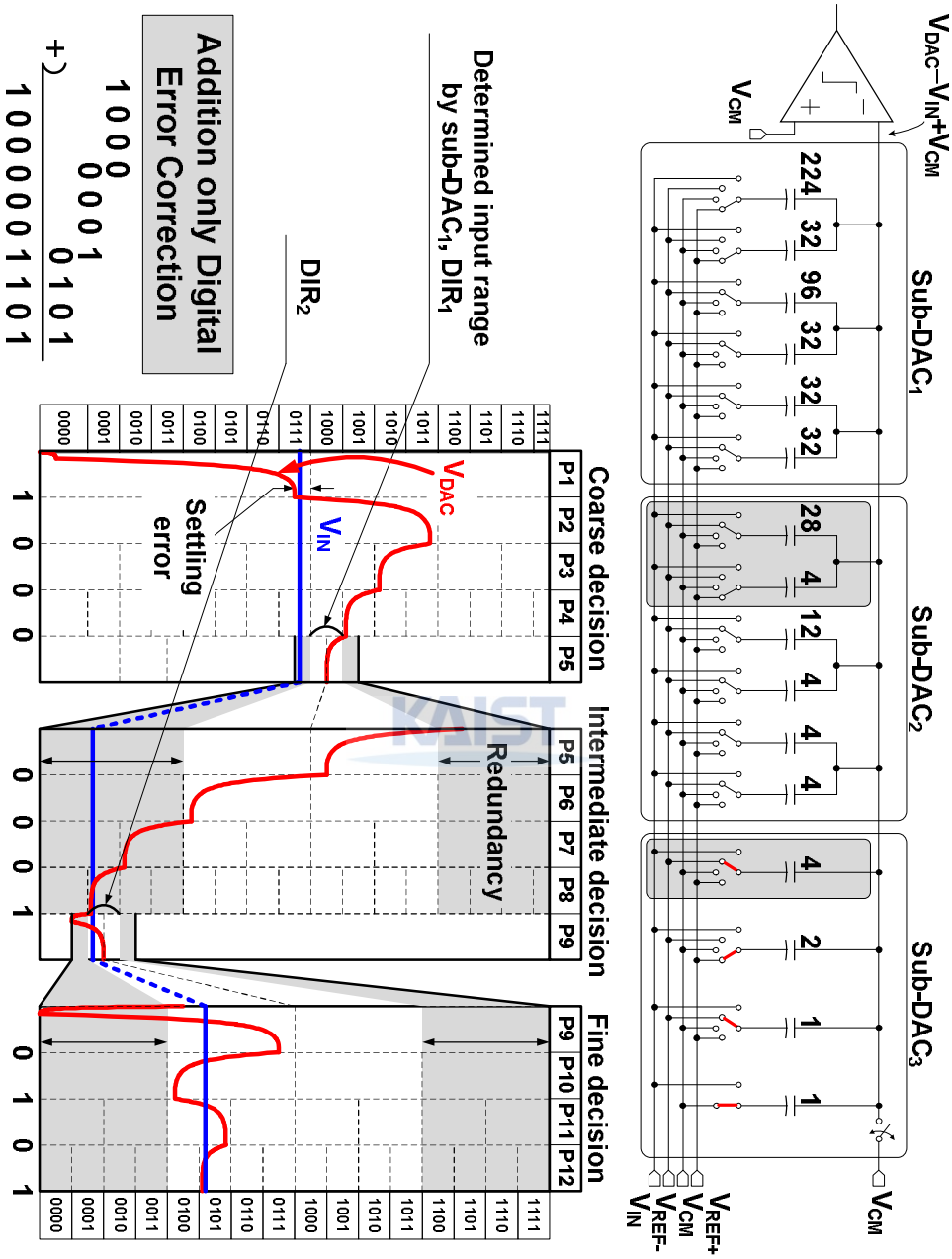


Fig. 4-27. Switching status by P_{12} (LSB) phase and DAC waveform

The DAC settling waveform (V_{DAC}) during the entire conversion process is shown in Fig. 4-21. First, V_{DAC} is shifted up by V_{SHIFT1} (= 32 LSB) by switching C_6 to V_{REF+}. At the same time, the MSB decision is conducted by connecting the rest capacitors to V_{CM}. Due to the incomplete settling of V_{DAC}, which is assumed to be less than 32 LSB, an incorrect decision is the result for D_{11}. The result is 1. Subsequently, the SA operation continues by utilizing the capacitors in sub-DAC_1, as shown in the table, until 4 MSBs are achieved. 1000 is determined for $D_{11}D_{10}D_9D_8$ in the example. Before sub-DAC_2 is used for an intermediate code decision, the first redundant phase P_5 is inserted. In this phase, C_6 (= $C_{6\_1} + C_{6\_2}$) returns to V_{CM} to prepare for use in the sub-DAC_2 operation. As a result, V_{DAC} is automatically located at the center of the determined input range (DIR_1). At the same time, another V_{DAC} shift, V_{SHIFT2} (= 4LSB), is performed for consecutive ADEC. This is done by switching C_3 from V_{CM} to V_{REF+}. By the following SA operations with sub-DAC_2, the intermediate bits (IMBs) are obtained as '$D_7D_6D_5D_4$ = 0001'. In the second redundant phase P_9, C_3 returns to V_{CM} for the same reason C_6 does in P_5. However, in this case, V_{DAC} drops to the lower boundary of DIR_2 during this operation. Therefore, V_{DAC} must be raised by 8 LSBs to correct the subsequent operations. This can be performed by additional capacitor switching. As the capacitors in sub-DAC_3 are untouchable for $D_3D_2D_1D_0$ decision purposes, sub-DAC_2 is reconfigured by selecting one 4C-valued capacitor which has been connected to V_{REF-}. It is switched to V_{REF+}. C_{4_1} (=4C) is used in this example. This is why the capacitors in sub-DAC_2 are split with 4C's and why those in sub-DAC_1 are split with 32C's. In this algorithm, capacitor rearranging is required only when the LSB from the previous stage (D_8 before sub-DAC_2 in use and D_4 before sub-DAC_1 does, in this design) is 1; thus, switch controller design for this is simple. After this operation, normal

SA operations are conducted with the $D_3D_2D_1D_0$ result of 0101. After all those sub-decisions, the three produced 4b data examples are added together with one-bit overlap, as shown in Fig. 4-21, leading to an error-corrected output of 1000001101. For better understanding, the important several phases from a switching table are illustrated from Fig. 4-22 to 4-27.

4.3 Measurement

A prototype ADC was fabricated in a 0.13μm CMOS process with a core size of 500 × 640μm^2 as shown in Fig. 4-28. The chip works under a 1.2V supply with reference voltages of 0.2V and 1.0V. Fig. 4-29 shows the measured DNL and INL plots and their peaks values were 0.8 and 1.5LSB, respectively. Fig. 4-30 shows the measured FFT result for an input frequency of 19.2MHz at a sampling rate of 40MHz. Fig. 4-31 and Fig. 4-32 show the measured dynamic performance. At an input signal of 2.5MHz, the sampling frequency is swept from 15MHz to 40MHz. Except for the 15MHz case, SFDR and SNDR show stable results in ranges of 50.6 ~53.2dB and 64 ~ 66.7 dB, respectively. Dynamic performance with an input frequency sweep at 40MS/s resulted in 52dB and 50.6dB SNDR for 2.5MHz and 20MHz of input, respectively. The relatively low SNDR from the measurement results from the poor DAC linearity, which itself stems from the routing parasitic capacitance. The total power consumption is 550μW and the ENOB is 8.4b. The resulting FOM is 42fJ/step.

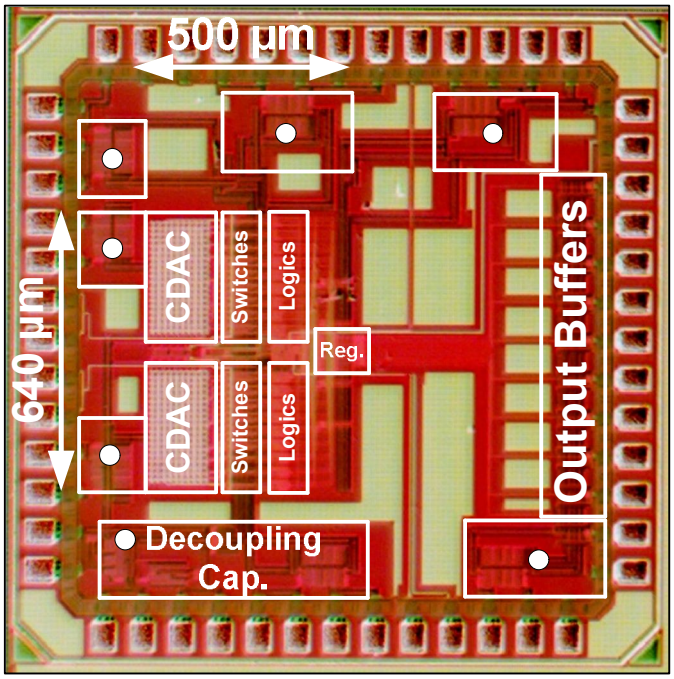


Fig. 4-28. Chip photograph

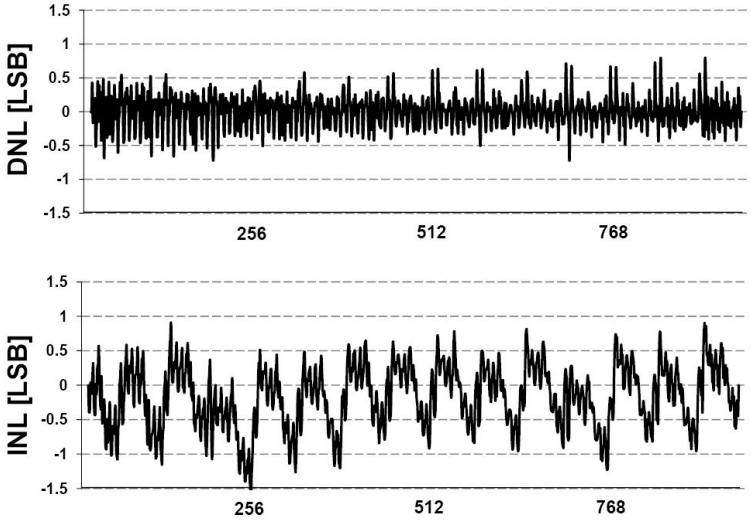


Fig. 4-29. Measured DNL and INL plots

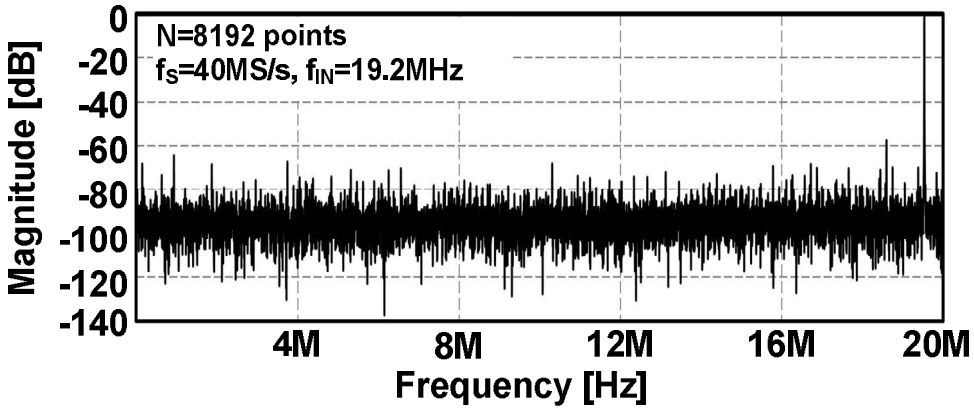


Fig. 4-30. Measured FFT result with 19.2MHz input at 40MS/s

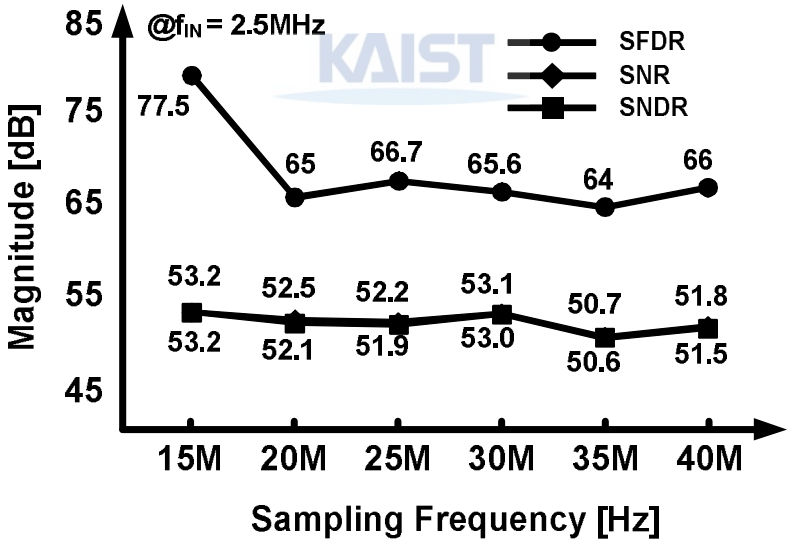


Fig. 4-31. Dynamic performances for various input frequencies

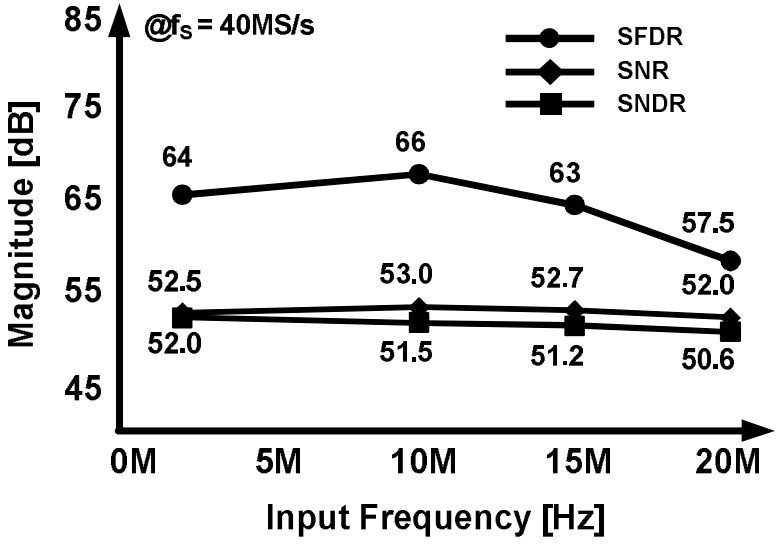


Fig. 4-32. Dynamic performances for various sampling rates

Process		0.13μm 1P8M CMOS
Supply		1.2V
Resolution		10b
Sampling rate		40MS/s
Power consumption	Comparator	155μW
	Digital	395μW
	Total	550μW
DNL		-0.78 ~ 0.72LSB
INL		-1.55 ~ 0.90LSB
SFDR @ 40MS/s		57.7dB @ f_{IN}=20MHz
SNDR @ 40MS/s		50.6dB @ f_{IN}=20MHz
Core area		500 x 640 μm^2
FOM		42fJ/conv.step

Table 4-1. Measured performance

4.4 Summary

This chapter 3 proposed a speed-optimized multi-step ADEC SAR ADC architecture capable of 37% speed enhancement with negligible hardware overhead. The proposed systematic operational principle of the ADEC SAR ADC can be simply extended for higher resolution SAR ADC for optimization of its power and speed.

5.Conclusion

On the basis of a survey on a SAR ADC, its trend was examined. A SAR ADC becomes very powerful due to its power efficiency and moderate speed with the enhancement of a CMOS technology. Besides, because circuit techniques for a SAR ADC are consistently developed and researched, the SAR ADC is more and more loved.

With this streaming, the three power efficient algorithms for SAR ADC were presented. First, the straightforward switching method with the other V_{CM} reference does not require the largest MSB capacitor in the DAC. The straightforward switching method is really power efficient more than any switching algorithm else, since it does not make the DAC be switched unnecessary along with eliminating the MSB capacitor. Second, the metastable-then-set (MTS) algorithm is proposed to reduce the number of decision cycles when the metastability occurs. The digital power from the SAR logic can be reduced proportionally to the number of the omitted decisions by the MTS algorithm. The less the metastability detector consumes current, the better power efficiency of the MTS algorithm is. Finally, the multi-step addition-only digital error correction (ADEC) algorithm makes SAR ADCs capable of 37% speed enhancement and is easily performed by adding codes coming from sub-DACs with 1b overlap. Since the ADEC algorithm is easy to understand and can be designed with negligible hardware overhead, the design of an ADEC SAR ADC is so simple that almost anyone can

reproduce this ADC.

The author hopes that the ADEC SAR ADC is called a ‘conventional SAR ADC’ in the near future.

6.Abstract (Korean)

SAR ADC를 위한 전력효율향상 알고리즘

본 논문은 전력효율향상을 위한 저전력 알고리즘을 가진 두 개의 asynchronous SAR ADC에 대한 것이다. 먼저 두 개의 ADC를 위해 개발된 알고리즘에 대해 각각 소개하자면, 다음과 같다.

첫째는, V_{CM}을 이용한 'Straightforward DAC 스위칭'방법으로써, 이는 SAR ADC에서 사용되는 내부의 DAC중 MSB를 담당하는 가장 큰 커패시터를 제거할 수 있기 때문에, SAR ADC의 가장 큰 면적을 필요로 하는 DAC의 면적을 반으로 줄일 수 있게 된다. 또한 입력신호 구동기, 기준전압 구동기가 보는 등가의 부하 커패시터가 작아지는 것을 의미하므로 각각의 세틀링을 위한 요구조건이 완화되며, 추가적으로 DAC 스위칭 전력소모가 줄어들게 된다. 큰 커패시터가 없어진 것은 그를 구동하는 스위치도 없어지는 것이고, 그 큰 스위치를 제어하는 큰 사이즈의 로직들도 없어지는 것이므로 추가적인 디지털 전력소모의 향상도 기대할 수 있게 된다. 둘째는, Metastable-Then-Set (MTS)알고리즘으로써, asynchronous SAR ADC는 필수적으로 해결해야 하는 비교기의 metastability문제를 해결하였다. Metastability는 비교기의 두 입력이 거의 같을 때, 비교기가 주어진 시간 안에 입력의 크기를 정확하게 판단해 내지 못하는 상태를 말하며,

metastability가 발생하면, SAR ADC의 전체동작을 멈추고 얻어내지 못한 해당 bit는 '1'로 나머지 하위비트는 '0'으로 디지털코드를 강제저장 한 후 A/D변환을 마침으로써 metastability를 해결하는 알고리즘이다. 이는 metastability문제를 해결한 기존의 해결책들과 달리, 남은 A/D변환과정을 멈추므로 디지털 스위칭 및 DAC 스위칭을 하지 않아도 되기 때문에, 10b 에 대하여 metastability가 일어날 수 있는 확률을 최대한 높여 약 10%의 디지털 전력소모를 줄일 수 있다. 셋째는, Addition-only Digital Error Correction (ADEC)으로써 기존의 SAR ADC를 구성하는 DAC를 가상의 여러 단으로 분리하고, 분리된 가상 DAC의 사이에 redundancy를 두어 세틀링 에러를 보정함으로써 정확한 결과를 얻어내는 알고리즘이다. 세틀링이 완전히 이뤄지지 않았다 하더라도, 이를 보정하는 알고리즘이므로 고의적으로 세틀링 시간을 짧게 설계함으로써, SAR ADC의 동작속도를 개선시킬 수 있게 된다.

본 논문은 위의 첫 번째와 두 번째 알고리즘을 갖고 동작하는 MTS SAR ADC와 첫 번째와 세 번째 알고리즘을 갖고 동작하는 ADEC SAR ADC에 대하여 기술하고 있다. Asynchronous 제어부를 가진 MTS SAR ADC는 I, Q 두 채널의 신호를 동시에 처리하도록 설계되었고, 각각의 ADC는 외부로부터 공급되는 하나의 기준전압을 공유하여 사용하도록 설계되었다. 공유된 기준전압의 사용은 DAC 세틀링을 방해하는 간섭현상이 발생할 수 있는데, 이를 해결하기 위해 flag-synchronization 방법을 사용하여 각 채널의 ADC가 동시에 세틀링을 시작하고 끝낼 수 있도록 설계하여 간섭을 최소화 하며, 각각의 기준전압을 사용하지

않아도 되도록 설계하였다. 10b MTS SAR ADC는 CMOS 0.13μm 공정으로 제작되었고, 1.2V의 전원을 갖는다. 17.5MS/s의 동작속도, 1.73MHz의 입력신호에 대해 최대 51.3dB의 SNDR의 성능을 갖고 있고, 측정된 아날로그와 디지털 전력소모는 각각 66μW 388μW로써 총 438μW를 소모하며, 79fJ/conv.step의 figure-of-merit을 보여준다. 다음의 10b asynchronous ADEC SAR ADC는 가상으로 분리된 3개의 sub-DAC을 갖고 sub-DAC사이에 잉여(redundant)코드결정구간을 넣음으로써 단지 4b DAC 세틀링 정확도를 갖는 조건에서도 불구하고 10b 선형성을 갖도록 설계되었다. 이는 37%의 동작속도 향상을 가져온다. ADEC SAR ADC는 MTS SAR ADC와 마찬가지로 CMOS 0.13μm 공정을 이용하여 제작되었고, 1.2V의 전원을 갖는다. 최대 40MS/s의 동작속도까지 동작하며, 50.6dB의 SNDR의 성능을 보여준다. 총 438μW의 전력을 소모하며, 42fJ/conv.step의 figure-of-merit을 갖는다.

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