Optimizing IP Management and Reuse to Gain Competitive Advantage

a PLM Whitepaper
Prepared by MatrixOne, Inc.

Executive Summary

Consumer and enterprise market demands are driving semiconductor innovation faster than ever before. Both markets constantly seek smaller electronic devices with greater functionality, interoperability, and dependability – all at very affordable prices. For example, today's mobile phones must work on multiple bands, deliver digital photos, display in color, include a long-life battery, and maintain a price point below one hundred U.S. Dollars. The pace of change and short shelf life for products means that delayed market introduction can have dire negative effects on a company's market position and profitability.

Semiconductor companies have responded to such extreme market demands by leveraging the exponential increase in silicon capacity and manufacturing advances to deliver smaller integrated circuits with increased performance at a lower cost. But for all the benefit for new applications that these new inegrated circuits (IC's) provide, there comes a sharp increase in chip costs, mostly due to the complex nature of the design.

Complex IC's are made up of multiple intellectual property (IP) blocks that must be widely characterized, tested, supported, and documented. Incorporating IP blocks into a 90-nanometer project requires the cooperation of a complex network of horizontal suppliers around the globe. Semiconductor companies' design organizations rely on Design Chains that can include internal design groups, external development partners, commercial IP and Library providers, ASIC/FPGA vendors, EDA and CAD tool providers, and foundries. As a result, engineering labor costs can exceed 30 million dollars for a 90-nanometer project. This is troubling because very few chip applications offer semiconductor companies the volume, margin and shelf life to justify such high costs.

To overcome high chip design costs in the IC environment, management of leading Semiconductor companies have dictated the establishment of programs for the reuse of IP, termed "Design Reuse." Through design reuse programs, semiconductor companies can drastically reduce chip development costs by reusing IP blocks that make up the core of an IC. Moreover, since much of the design chain can be avoided for reused IP, new product development efforts can be drastically streamlined.

The purpose of this paper is to describe the best practices that semiconductor companies have adopted to develop effective design reuse programs that leverage the extended design chain to speed time-to-market, deliver predictable success, gain competitive advantage, and increase profitability.

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Design Reuse Challenges

Design reuse success depends on a company's ability to manage both internally developed and third party IP so that it is visible, securely managed, and supported across the Design Chain. While IP is often considered an internal company property, design components from third party sources are often used to provide special functionality, technology outside of a company's core competency, and/or common, non-value-add portions of a design.

Given the complex nature of chip design chains, semiconductor companies can no longer depend upon special one-on-one relationships or ad hoc IP-sharing environments where engineers acquire their best IP through emails and phone calls in an informal knowledge-sharing environment. To achieve the full promise and competitive advantages that a design reuse program can provide, successful companies have established an enterprise-wide program of best practice processes and technology infrastructure to support their intricate design chains. In some cases, they have set up dedicated teams to design components for reuse, absent of a specific product goal.

Best Practices Design Reuse Program

To optimize design reuse, companies need to focus on a system for capturing, searching, and supporting design components. Consider how each of the following best practices contributes to a successful design reuse program.

- **Capture and Control** To start, designers will consider only IP that is known. Thus, the first requirement is a single source of IP data that shows all blocks ready for reuse, such as a company-wide, online catalog with a flexible classification hierarchy. Once the IP is classified, robust access controls are required down to the individual design component level.

- **Search and Navigate** Once IP is placed in a catalog, designers need the ability to search and navigate the catalog for design components, including the ability to search for parameters such as process geometry, bit width, methodology, and clock rates. They must also have the ability to determine if the virtual component has been proven in real silicon and whether it should be associated with all IP blocks.

- **Compare and Download** Upon finding a potential reusable IP, designers must be able to compare and select the best IP blocks for their design. Comparison by key design parameters becomes critical to identifying the right IP block. Upon IP block selection, designers need to easily download the design(s) into a private workspace while maintaining version control integrity on all downloaded files. This assures the designers will not waste valuable days on a faulty IP block.

- **Distribute and Support** A design reuse program should enable designers to securely distribute IP across the enterprise and to design partners. Since IP blocks are rarely "plug-and-play," designers need to receive support for the use of an acquired IP block.

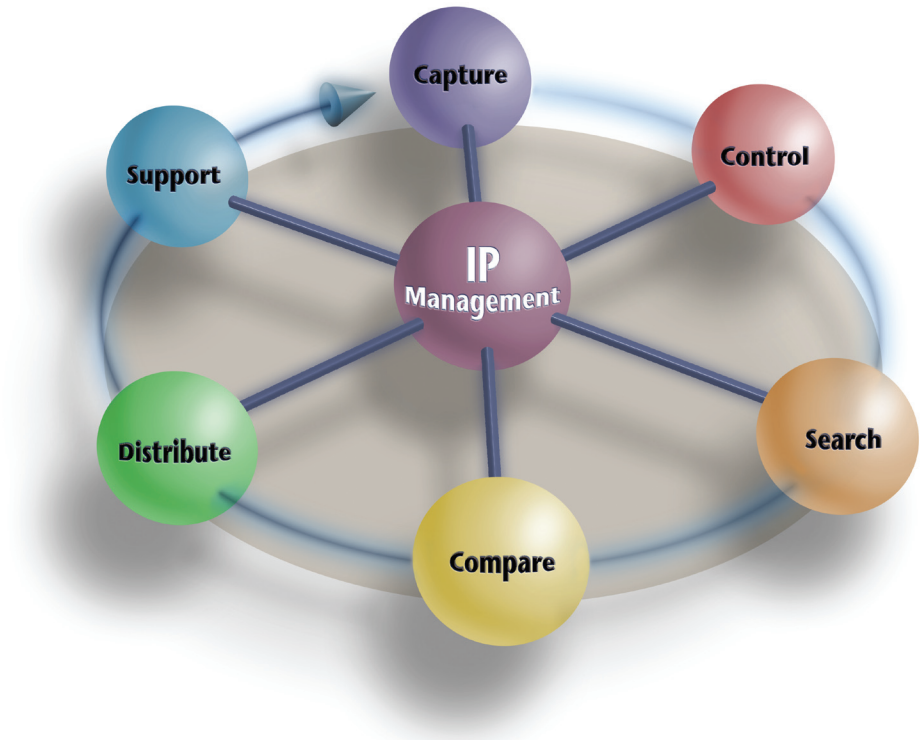
Designing for Reuse

In order to increase design productivity and lower costs, it is becoming increasingly important to define design methodologies that will ensure reuse is built into the design cycle of a chip (or core) from initial conception through to production. This involves creating standard methodologies across the organization for creation of reusable IP in IP Authoring, IP Qualification and Verification and Chip Integration processes.

These methodologies, and their associated flows, should also allow seamless access and integration to IP libraries, IP providers, cell libraries, multiple EDA tool databases, foundries, internal & external partners, verification and qualification processes and tools. This ensures that the chip designer is able to evaluate all existing and third party IP available to avoid costly purchase or duplication of an existing IP core, reducing both costs and cycle time.

Introducing MatrixOne IP Management Featuring MatrixOne IP Gear™

MatrixOne, Inc. has significant experience in design data management for high tech companies, supporting critical design programs for twenty-three of the world's twenty-five largest semiconductor companies. Market leaders leverage MatrixOne's IP management solution to optimize their global design chains, reduce costs, and speed time-to-market. The MatrixOne solution incorporates all the previously described best practices, enabling more simple system management and end-user adoption.



This diagram illustrates the MatrixOne IP Management solution and highlights the capabilities that it delivers to support the management and reuse of IP.

Capturing IP

In most design organizations, semiconductor IP is scattered throughout engineer's desktops and spread across multiple business units. This information is usually exchanged via email among engineers resulting in a very inefficient and costly process of handling important design information. MatrixOne's IP management solution is a web-based semiconductor catalog where organizations can capture all IP in a central location and make it widely available across the enterprise for reuse. Organizations can spend time designing new chips rather than trying to make sure they have the latest design information. Partners and suppliers can exchange their IP and feedback with internal product development teams for early concurrent development, drastically minimizing downstream development costs arising from product quality and incompatibility issues.

Controlling Access

Since IP is a valuable asset to an organization, it needs to be protected. MatrixOne's IP management solution has fine-grained access controls to allow global semiconductor companies to protect IP on a per component basis. Design organizations can provide access to components within the catalog to certain employees while restricting access to external design partners. This allows global semiconductor companies to ensure IP is properly secured on a per-user and per-component basis. Secure transmittal of design data is an important concern for acquired components, partner/customer components, and of course for a company's own valuable IP. Industry standard protocols for transmission, encryption, and security - such as SSL, XML, and HTTPS - ensure wide compatibility and speed deployment of the design chain.

Controlling the access of the variety of personnel who must be able to use the reuse catalog is a security concern as well. Partners, contractors, and consultants all require access to certain components while being restricted from others. Sensitive information and partnering relationships may require that even internal team members have limited access to the reuse catalog.

Granting varied levels of access is also a requirement, such as the ability to search without the ability to view a component's full design information or the ability to view but not create or modify components. In order to enable efficient access while ensuring multi-faceted security concerns are met, the reuse catalog will need to support a rigorous and sophisticated access control scheme.

Searching Effectively

Searching for IP is the primary inhibitor to effective design reuse programs. Even if companies have centralized their internal and external IP into a single catalog, finding relevant IP blocks and evaluating them against one another and against current product requirements represents a much deeper challenge. In order to decide which IP is relevant and which is not, companies need the ability to find IP quickly.

With the IP management solution, designers can easily navigate semiconductor IP classification taxonomy to find design components. Alternatively, users can perform a simple search to identify the components needed. Finally, parametric searching allows users to enter pre-defined IP parameter values such as clock speed, bus width, and technology size to narrow down the search.

Comparing Parameters

Once a set of IP blocks is narrowed down, comparison criteria enables the user to view different IP in side-by-side comparisons that display blocks' properties and attributes. Such a capability allows designers to find an exact match for their design plans, or in the earliest design stages, search for inexact matches that fall within a customer's specifications that may warrant a new design path. This saves costly custom design time and design chain expense. Additionally, the high-level of complexity of electronic design components requires more than simple descriptive information in order to make the final IP selection decision. Integration of the catalog with design knowledge bases, helpdesk information, and design use history enable the designer to complete the IP assessment and accurately identify the proper component for reuse.

Distributing Securely

Another important concern for a reuse system is the actual delivery of design elements once they have been selected by end users. The ubiquity of the Internet, falling bandwidth prices, and a wide array of Internet-based delivery mechanisms all combine to make the Web the ideal delivery choice for IP. But a design reuse system requires more than mere e-mail delivery of Zip files or FTP. These methods provide poor scalability and inadequate security.

Scalable delivery is critical to reuse, because a mature repository can quickly reach terabyte size. Low-end delivery mechanisms would prohibit effective transmission within such an environment and would require copies to be transmitted to each design site in order to keep them all synchronized. Despite today's low-cost bandwidth, transmission of multiple copies of the entire repository would be costly and place a burden on local storage resources. More importantly, the related time delay would prove costly for design teams in terms of market timing.

Finally, with the creation of new design elements constantly occurring at multiple sites in a chip design chain, maintaining a single synchronized version of the IP database at all sites would be nearly impossible with low-end mechanisms. A scalable solution requires automatic and incremental synchronization of the reuse database. Designers will not typically commit to long hours of IP reuse research if they believe they can design a block of IP faster from scratch.

Managing Issues

Entering design components into a reuse repository does not represent the end of a components' development. Ongoing support of the components, for both internally and externally developed IP, is an important consideration. Problems and usage questions are likely to arise when designers begin to incorporate reuse components into their designs. Additionally, management and designers are likely to update IP over time as they seek to resolve product issues and/or enhance functionality of designs. Issue tracking/resolution and component updates may be handled in a variety of ways. Informal systems might consist of email messages, history log files, and retrieval of updated design files by FTP. Such informal systems offer little in the way of tracking issues/solutions and notifying developers about the availability of requested updates. The best-in-class approach is to integrate help desk capabilities into the reuse repository so that issue tracking and known problem-solution databases become common, expected elements of the system. More proactive systems serve designers well by automatically notifying them of the availability of new or modified components and providing for the synchronization of updated component catalogs, making designers aware of all the latest component options.

Conclusion

The MatrixOne IP Management solution, featuring MatrixOne IP Gear®, helps semiconductor companies to successfully reuse internally developed and third party IP by enabling the establishment of an IP repository that is visible, securely managed, and supported across the Design Chain. Having such a solution in place benefits these companies as they seek to gain competitive advantage through lower new product development costs and faster time-to-market.

As chip design chains become increasingly disaggregated and complex, the value of IP management systems will only increase. Those companies who are adopting sound policies and systems that maximize reuse will enjoy an ever-increasing competitive advantage in the markets they serve.

About MatrixOne

MatrixOne, Inc. (NASDAQ: MONE) is a recognized leader in delivering collaborative Product Lifecycle Management (PLM) solutions. Together with our partners, we provide flexible solutions that unleash the creative power of global value chains to inspire innovations and speed them to market. MatrixOne's global customers represent the aerospace/defense, automotive, consumer products, general machinery, high technology and life sciences industries, and include GE, Procter & Gamble, Philips, Siemens, Agilent Technologies, Johnson Controls and Honda. MatrixOne is headquartered in Westford, Massachusetts with locations throughout the world.

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