



# Implementation of SOP and POS Form Logic Functions

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EECS: 1100 Digital Logic Design  
The University of Toledo

Lab Assignment #3

## 1. Objectives

- becoming familiar with two *standard* forms of logic functions: *Sum of Products (SOP)*, and *Product of Sums (POS)*,
- becoming familiar with two *canonical* forms of logic functions: *Sum of Minterms*, and *Product of Maxterms*,
- applying the algebraic manipulation method to transform standard to *canonical* forms,
- learning a procedure for deriving the truth table of a logic function which is known in algebraic form,
- learning how to derive the *minterm list* (decimal sum of minterms) form of a logic function whose truth table is known,
- learning how to derive the *maxterm list* (decimal product of maxterms) form of a logic function whose truth table is known,
- exercising two-level implementation of logic functions,
- becoming familiar with degenerate two-level logic circuits: AND-AND,
- developing skills in analyzing and testing the behavior of combinational logic circuits.

## 2. Prelab Assignment

### 2.1 SOP FORM OF LOGIC FUNCTIONS

2.1.1 Applying the algebraic manipulation method, derive the *sum of minterms* canonical form (expression) of the logic function  $f(D,C,B,A)$ , whose SOP form is given in equation (A.2-1)

$$f(D,C,B,A) = \bar{B} \cdot C + A \cdot \bar{D} \quad (\text{A.2-1})$$

Show the derivation process, and show the *sum of minterms* canonical expression of the function  $f(D,C,B,A)$ , as equation (2.1-1).

**Hint#1:** In the *sum of minterms* canonical form, every product term includes a literal of every variable of the function. Product terms of the SOP form which do not include a literal of a variable, say variable B, should be augmented by,

- AND-ing the product term which misses a literal of B with  $(B + \bar{B})$ ,
- subsequently applying the distributive property to eliminate the parenthesis.

2.1.2 Using the derived *sum of minterms* expression, prepare truth tables of the logic function  $f(D,C,B,A)$  and of its complement  $\bar{f}(D,C,B,A)$ , and show them both together as Table T2.1-1, including additionally corresponding *minterm* and *maxterm* expressions in all rows of the table.

2.1.3 Using the derived table T2.1-1, prepare the *minterm list form* (decimal Sum of Minterms form) of the logic function  $\bar{f}(D,C,B,A)$  and of its complement  $f(D,C,B,A)$ , and show them as equations (2.1-2) and (2.1-3) respectively.

2.1.4 Prepare a computer generated drawing of a two-level AND-OR logic circuit which implements the expression (A.2-1) of the function  $f(D,C,B,A)$ ; show the drawing as Figure 2.1-1(a).



2.1.5 Using integrated circuit components listed in section 3.2, design a physical layout of the logic circuit shown in Figure 2.1-1(a). Prepare a computer generated drawing of the layout and show it as Figure 2.1-1(b). Provide the IC package pinouts on both drawings of Figure 2.1-1.

**Hint#2** Pinouts (pin numbers) are available in Figure 2.5 of the course text book, pp.107-109, and in the TTL Data Book.

**2.2 DEGENERATE TWO-LEVEL AND-AND LOGIC CIRCUIT**

2.2.1 Prepare your own computer generated version of the logic circuit diagram shown in Figure A.2-1, and show the diagram as Figure 2.2-1(a).

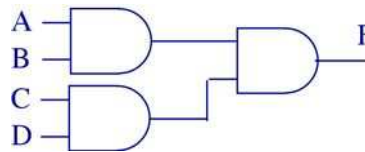


Figure A.2-1 Degenerate two-level AND-AND logic circuit implements the AND function.

2.2.2 Prepare a truth table of the logic function F implemented by the circuit of Figure A.2-1, and show it as table T2.2-1.

2.2.3 Use the derived table T2.2-1 to prepare the canonical sum of minterms and product of maxterms forms of the logic function F. Show the algebraic expression of the sum of minterms as equation (2.2-1), and show the decimal product of maxterms (maxterm list) expression as equation (2.2-2).

2.2.4 Using integrated circuit components of the collection listed in section 3.2, design a physical layout of the logic circuit shown in Figure 2.2-1(a). Prepare a computer generated drawing of the layout and show it as Figure 2.2-1(b). Provide the IC package pinouts on both drawings of Figure 2.2-1.

**2.3 POS FORM OF LOGIC FUNCTIONS**

2.3.1 Derive the POS standard form (expression) of the function  $f(D,C,B,A)$  applying the algebraic manipulation method to its SOP form given by equation (A.2-1). Show the derivation process and show the POS form of the function  $f(D,C,B,A)$  as the equation (2.3-1).

**Hint#3:** Apply repeatedly the postulate  $a + b \cdot c = (a + b) \cdot (a + c)$  to equation (A.2-1), considering as  $b \cdot c$  one of the products of the SOP expression and treating the sum of all remaining products as  $a$ .

2.3.2 Applying the algebraic manipulation method to POS form expression in equation (2.3-1), derive the *product of maxterms* canonical form (expression) of the logic function  $f(D,C,B,A)$ . Show the derivation process, and show the *product of maxterms* expression of  $f$  as equation (2.3-2).

**Hint#4:** In the *product of maxterms* canonical form, every sum term includes a literal of every variable of the function. Sum terms of the POS form which do not include a literal of a variable, say variable B, ought to be augmented by,

- OR-ing the sum term with  $B \cdot \bar{B}$ ,

- subsequently applying postulate  $a + b \cdot c = (a + b) \cdot (a + c)$  to distribute the product  $B \cdot \bar{B}$ .



- 2.3.3 Compare the maxterms of equation (2.3-2) to contents of table T2.1-1. Is the set of maxterms in equation (2.3-2) equal to the set of maxterms in those rows of T2.3-1 in which the value of  $f(D,C,B,A)$  is equal to logical 0? If that happens not to be the case, check all derivations and correct the error(s).
- 2.3.4 Prepare a computer generated drawing of a two-level OR-AND logic circuit which implements the expression (2.3-1) of  $f(D,C,B,A)$ , and show the drawing in Figure 2.3-1(a).
- 2.3.5 Compare the POS expression of equation (2.3-2) to expression (2.3-1) and logic circuit of Figure 2.3-1(a) to determine the numbers of 2-input OR-gates and 2-input AND-gates that would be required if one wanted to implement the expression (2.3-2) of the function  $f$ . Compare these numbers to those of the logic circuit of Figure 2.3-1.
- 2.3.6 Using integrated circuit components listed in section 3.2, design a physical layout of the logic circuit shown in Figure 2.3-1(a). Prepare a computer generated drawing of the layout and show it as Figure 2.3-1(b). Provide the IC package pinouts on both drawings of Figure 2.3-1.

**Hint#5:** Consider implementing the required four-input AND gate as the degenerate two-level AND-AND logic circuit of Figure A.2-1.

### 3. Lab Equipment and Circuit Components

#### 3.1 EQUIPMENT

- Proto board Global PB-104,
- Agilent E3631A DC power supply,
- Function generator: Agilent 33120A,  
(Replacement model: Agilent 33220A Function / Arbitrary Waveform Generator)
- Mixed-Signal oscilloscope Agilent 54645D,  
(Replacement model: Agilent DSO6012A Oscilloscope)
- Dell GxaEM computer system.

#### 3.2 LOGIC GATE AND CIRCUIT COMPONENTS

- IC component 7404, hex inverters (1)
- IC component 7408, quad 2-input AND gates (1)
- IC component 7432, quad 2-input OR gates (1)
- IC component 7493, ripple counter, (1)

### 4. Lab Assignment

#### 4.1 AND-OR IMPLEMENTATION OF $f(D,C,B,A)$

- 4.1.1 Using the physical layout diagram of Figure 2.1-1(b) as a reference, build on proto board the physical circuit which implements the function  $f(D,C,B,A)$ . As an auxiliary logic circuit, build additionally the binary counter which was used in Lab Assignment #1 to generate binary representations of integers 0 through 15. The same auxiliary circuit is repeated in Figure A.4-1. It will serve in this, and all subsequent Lab Assignments as a generator of all combinations of the input variables A,B,C, and D.

**Hint#6:** This is a convenient occasion to recognize that in logic circuits: numerical values and values of logic variables share the same representation.

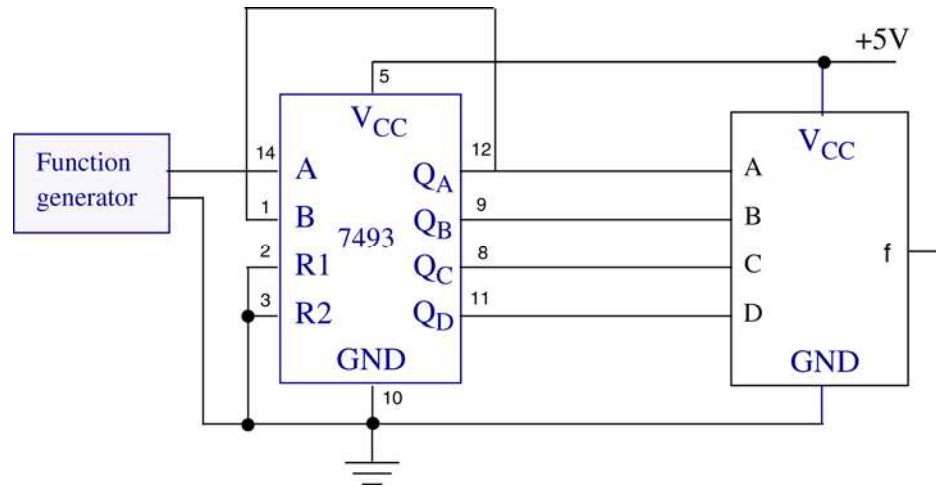


Figure A-4.1 The complete circuit for experimenting with AND-OR, AND-AND and OR-AND implementation of  $f(D,C,B,A)$ , using a black-box representation of the implemented circuit.

- 4.1.2 Connect digital channels D0 through D5 of the Mixed-Signal oscilloscope Agilent 54645D to circuit constructed under 4.1.1:
  - channel D0: to output of the function generator, Agilent 33120A,
  - channel D1: to input A of the circuit which implements  $f(D,C,B,A)$ ,
  - channel D2: to input B of the circuit which implements  $f(D,C,B,A)$ ,
  - channel D3: to input C of the circuit which implements  $f(D,C,B,A)$ ,
  - channel D4: to input D of the circuit which implements  $f(D,C,B,A)$ .
  - channel D5: to output of the circuit which implements  $f(D,C,B,A)$ .
 Establish a ground connection. Turn on digital channels D0 through D5, and rename them A, B, C, D, and f respectively.
- 4.1.3 Adjust the frequency of the function generator to 1MHz. Set the triggering mode of the Agilent 54645D to combination 0000 on channels D1 through D4. Hit the key Single on Agilent 54645D. Adjust the display of waveforms so that the first appearance of the combination of signal values 0000 on channels D1 through D4 is positioned at the left end of the screen, and that the whole screen shows ten percent more than just two periods of the signal at  $Q_D$ .
- 4.1.4 Verify correct functioning of the circuit by comparing the obtained waveform of the function  $f(D,C,B,A)$  to its truth table T2.1-1. In case the waveform and the truth table do not match, check the logic and the physical circuit diagram of Figure 2.1-1, and check the connections on the protoboard.
- 4.1.5 Save the Screen Image of the correct waveforms of the channels D0 through D5 to a file named L3\_415.tif on the Dell GxaEM computer system. (Alternatively, use the Screen Capture tool.)

#### 4.2 DEGENERATE TWO-LEVEL AND-AND LOGIC CIRCUIT

- 4.2.1 Using the physical layout diagram of Figure 2.2-1(b) as a reference, build on the proto board the corresponding physical circuit.
- 4.2.2 Connect the digital channels D0 through D5 of the Mixed-Signal oscilloscope Agilent 54645D to the circuit constructed under 4.2.1:
  - channel D0: to output of the function generator, Agilent 33120A,
  - channel D1: to input A of the degenerate two-level AND-AND circuit,



channel D2: to input B of the degenerate two-level AND-AND circuit  
channel D3: to input C of the degenerate two-level AND-AND circuit  
channel D4: to input D of the degenerate two-level AND-AND circuit.  
channel D5: to output F of the degenerate two-level AND-AND circuit.

Establish the ground connection. Turn on the digital channels D0 through D5, and label the channels D1 through D5 as A, B, C, D, and F respectively.

- 4.2.3 Adjust the frequency of the function generator to 1MHz. Set the triggering mode of the Agilent 54645D to combination 0000 on channels D1 through D4. Hit the key Single on Agilent 54645D. Adjust the display of waveforms so that the first appearance of the combination of signal values 0000 on channels D1 through D4 is positioned at the left end of the screen, and that the whole screen shows ten percent more than just two periods of the signal at  $Q_D$ .
- 4.2.4 Verify that the circuit functions correctly by comparing the obtained waveform of the output F to contents of the table T2.2-1
- 4.2.5 Save the Screen Image of the correct waveforms of the channels D0 through D5 to a file named L3\_425.tif on the Dell GxaEM computer system. (Alternatively, use the Screen Capture tool.)
- 4.2.6 What is the maximum number of inputs (fan-in) of an AND gate which can be implemented using the IC 7408? How many different implementations of the maximum fan-in AND gate can be constructed using the IC 7408?

#### 4.3 OR-AND IMPLEMENTATION OF $f(D, C, B, A)$

- 4.3.1 Using the physical layout diagram of Figure 2.3-1(b) as a reference, build on proto board the physical circuit which implements the function  $f(D,C,B,A)$ .
- 4.3.2 Connect the digital channels D0 through D5 of the Mixed-Signal oscilloscope Agilent 54645D to the circuit constructed under 4.3.1 as described under 4.1.2.
- 4.3.3 Operate the Agilent 54645D as described under 4.1.2.
- 4.3.4 Verify the correct functioning of the circuit by comparing the obtained waveform of the function  $f(D,C,B,A)$  to its truth table T2.1-1. In case the waveform and the truth table do not match, check the logic and the physical circuit diagram of Figure 2.3-1, and check the wire connections on protoboard.
- 4.3.5 Save the Screen Image of the correct waveforms of the channels D0 through D5 to a file named L3\_435.tif on the Dell GxaEM computer system. (Alternatively, use the Screen Capture tool.)

#### 4.4 TRANSFER OF CAPTURED WAVEFORMS.

Transfer (ftp) the files L3\_\*.tif from the Dell GxaEM computer system to your personal College of Engineering computer account.



## 5. Lab Report

To be considered complete, the Lab report #3 must contain the following,

1. Cover sheet - Lab style, filled out,
  - 1) The result of work under 2.1 through 2.3
  - 2) The result of work under 4.1 through 4.3.
4. A report on items not already included under 2. and 3. above, which includes:
  - a discussion of the insights gained through the conducted experiments,
  - textual description and graphical/tabular illustration of the design procedure(s),
  - description of implemented testing procedures,
  - conclusions reached as a result of performing the lab experiment,
  - comments and suggestions that might lead to easier and/or deeper understanding of the topics covered by the assignment.

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