NASA'S ALLIANCE WITH INDUSTRY IN DEFINING ITS ADVANCED ELECTRONIC PACKAGING AND INTERCONNECTION PROGRAM

by

Phillip R. Barela
Jet Propulsion Laboratory
California Institute of Technology

ABSTRACT

For years NASA's use of electronic packaging and the associated manufacturing processes has been extremely conservative. This conservatism has provided spaceflight hardware designs which are proven and robust but very costly. in previous times, the system level costs (primarily mass and volume) associated with flying these robust designs was justified based on the heritage of the hardware design and manufacturing processes. With the tightening budgets across the DoD and NASA, the use of this flight proven technology is being questioned in light of the rapidly advancing areas in electronic packaging. New and emerging technologies such as microelectro mechanical systems (MEMS), photonics, integrated structural electronics, area array packaging, direct chip and chip scale packaging are now planned to fly on NASA's near-term, flight missions.

The Jet Propulsion Laboratory is currently supporting NASA Headquarters-Code Q in defining its fiscal year 1996-98 Electronic Packaging and Advanced Interconnect research and development program, To address the issues pertaining to the unknown spaceflight quality of these new technologies, NASA is re-focusing its Advanced Packaging and interconnection Program towards cooperative teaming with industrial organizations with the primary focus of accelerating the time required to fly new electronic packaging and interconnection technologies. In addition, NASA is chartered with supporting the development and transfer of technology to non-NASA interests. These objectives are being met in two ways: 1) development of Cross Product Development Teams (CPDT) including industrial interests, academia and other government agencies; 2) by supporting industrial development of ncw standards and guidelines addressing new technologies. NASA has been supporting the development of some of the industrial roadmaps and uses these roadmaps to determine which areas of technology would benefit the most from NASA investment anti provide NASA cost-effective access to the technology. This validation and development effort by NASA will support the maturity level and mission readiness of these technologies for applications

outside of NASA. This effort furthers the infrastructure and confidence needed for new technologies to gain wide market acceptance.

In FY96, NASA Code Q's research and development activities, in the area of electronic packaging and interconnection, will address:

- MEMS
- Chip Scale Packaging
- MMIC Packaging
- Photonics
- COB on Flex
- BGA (continued)
- 2-D & 3-D dice attachment

These activit ics will focus on the manufacturing processes, materials, interconnect design and validation tools development for these technologies. These projects will also be focused on application development and not pure research.

This technical brief will discuss the developing structure of the Cross Product Development Teams, the primary objectives of NASA and the approach taken for each of the FY96 technical tasks. Dissemination of the project results, technical information and public access will also be addressed.

ACKNOWLEDGMENT

The research described in this publication is being carried out by the Jet Propulsion Laboratory, California institute of Technology, under a contract with the National Aeronautics and Space Administration.

Mr. Phillip R. Barela

Mr. Barela is presently the Technical Group Supervisor for the Applications Engineering Group, Quality Assurance Section, where he has worked for the last four years. Mr. Barela has served in numerous positions dealing with packaging design, failure analyses and manufacturing engineering at Gould Electronics, NavCom Defense Systems, Loral Electro-Optical Systems and the Jet Propulsion Laboratory. Mr. Barela has held positions as a Failure Analyst, Microelectronics Engineer and Manufacturing Engineer working with the package design and manufacture of hybrids (thick and thin), MCMs, COB, through hole, surface mount and mixed assembly technologies. In this capacity, he has started numerous product lines for low to medium volume military and space products. Mr. Barela has extensive experience with design and producibility issues relating to new and mature product lines for low to medium volume applications. Mr. Barela is a member of the SMTA, 1 PC, ITRI, SOCA, SME, is a certified Manufacturing Engineer and received his BS in Manufacturing Engineering.