凌通科技
Generalplus

GPL133A Confirmation Sheet

V1.2 11/24/2005

Customer		**Date**	
Project title		**Code No.**	
Project description			
Working voltage	☐2.4V ~ 3.6V (2-battery) ☐3.6V ~ 5.5V (3-battery)	**CPU Frequency:** **ROSC Frequency:**	_____MHz _____MHz
LCD Matrix	COM:_____ SEG: _____ Bias: _____ V_{LCD}: _____V		
32768Hz OSC	☐X'TAL ☐Unused (2Hz, 4Hz, ... Timer base not available)		
Components	☐GPLD112 ☐GPLD80 ☐GPLD801 ☐GPLD802		

Release code file (fill "00H" for unused area)

Binary filename:	**Binary file check sum:**
ROM Size: 256K bytes	☐Check
Zero Page RAM Size: 192 bytes, $40~$FF	☐Check
Data RAM Size: 3840 bytes, $100~$FFF	☐Check
LCD RAM Size: $100~$FFF	☐Check
LCD start address: _____, end address: _____.	
Stack: start address: _____, end address: _____.	
Interrupt vector: $FFFA-FFFF	☐Check

Low voltage detection	2.4V	☐enable	☐disable	2.6V	☐enable	☐disable

Mask option

Low voltage reset	2.3V	☐Enable	☐Disable

Watchdog ☐Enable ☐Disable

If watchdog is enabled, please check the followings:

(A). Watchdog jumper must be removed from the EV board. ☐Check

(B). Watchdog port must be cleared. ☐Check

Input / Output

Port0 (checked by "✓" or "✗")

	b0	b1	b2	b3	b4	b5	b6	b7
Input								
Output								

Port1 (checked by "✓" or "✗")

	b0	b1	b2	b3	b4	b5	b6	b7
Input								
Output								

Port2 (checked by "✓" or "✗")

	b0	b1	b2	b3	b4	b5	b6	b7
Input								
Output								

Port3 (checked by "✓" or "✗")

	b0	b1	b2	b3	b4	b5	b6	b7
Input								
Output								
				Eldrv0	Eldrv1	Tx		Rx

If Tx and Rx are selected, b5 and b7 cannot be I/O.
If Eldrv0 and Eldrv1 are selected, b3 and b4 cannot be I/O.

Hardware /Software

Program must be tested by EPROM on EMU board and piggyback.	☐Check
If Frosc > 7MHz, Port18 b3 must be set to "1".	☐Check
When system powers on, LCD control port and buffer must be initialized. Otherwise, the data of LCD driver will be randomly generated.	☐Check
DC-DC charge pump frequency must be in the range of 80K ~ 100KHz.	☐Check
When UART is applied, all configurations in $19 must be set up again and $19.5 must be set to "0" after reset operation ($19.5=1).	☐Check
Sleep procedure Make sure the FP interrupt is completed and then CPU must enter sleep mode within one frame-time (e.g. suppose frame rate is 60Hz; CPU must enter sleep mode within 1/60 second after the FP interrupt is completed).	☐Check
Make sure to clear wakeup port immediately after wake up.	☐Check

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Before entering into sleep mode, the CPS0, CPS1, and CPS2 in P_Port04H MUST be set to "0 0 0" respectively to turn off LCD clock. Fail to fill "0" into the above bits may result in current leakage during sleep mode. For rest conditions, the CPS0, CPS1, and CPS2 in P_Port04H CANNOT be set to "0 0 0" respectively.	☐Check ☐Check
Before entering sleep mode, 24VEN ($18.5) cannot be set to "1" (enabled). To enable 24VEN ($18.5), it should be set immediately after reset or wakeup.	☐Check
In tone mode, DACL0 and DACL1 ($12.3 and $12.4) must be set as "00".	☐Check

Test Program

The following test program area and test program vectors are reserved for GENERALPLUS. The user's program or data must not be in these ROM areas.

Test Program Area	CPU view: $C000 ~ $C7FF ROM area: $4000 ~ $47FF	☐Check
Test Program Vector	CPU view: $FFF2 ~ $FFF7	☐Check

General programming checklist

The general programming checklist intends to provide some general characteristics about GENERALPLUS devices. It is the customer's responsibility to check all the information in the list. No responsibility is assumed by GENERALPLUS for any non-checked box even this confirmation sheet has been approved by GENERALPLUS. Make sure the following conditions are met and verified:

CPU stack pointer must be reset after system power-on and wake-up.	☐Check
All RAM must be initialized after power on.	☐Check
Timer content must be initialized before timer interrupt is enabled.	☐Check
Do not enable interrupt before initializing RAM.	☐Check
The instructions of "SEI" and "CLI" must be removed from the IRQ and NMI service routines.	☐Check
Sleep port must be cleared and re-initialized before entering sleep mode.	☐Check
The used RAM not over the stack reserved area.	☐Check
Correct RAM/ROM size and start addresses.	☐Check
No current drain on I/O in sleep mode. No I/O remains floating in sleep mode.	☐Check
Non-used I/O ports should be masked off (for input process). Example (suppose PortA [7:4] are invalid): LDA PortA ; read I/O port A Data AND #0FH ; mask off high nibble	☐Check
Switch tone mode on as follows Step1. Select tone mode. Step2. Setting volume. If step2 is performed prior to step1, the volume is **unknown**.	☐Check

Document version

Programming guide title and version:

User's guide title and version:

Other documents (if any):

Development tool / board version

EV board version:

EV chip version:

Piggyback / demo board version:

Software / Hardware tools version:

Customer note	GENERALPLUS note
Name (print): _____ **Tel:** _____	**Name (print):** _____ **Tel:** _____
Signature: _____	**Signature:** _____

Note: Please send/fax this form to GENERALPLUS. GENERALPLUS will return it back with signature.

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