Data Sheet

IC timers 555 and 556

RS stock numbers 305-478, 305-838, 638-942, 638-958

A range of IC timers suitable for monostable or astable operation. In the monostable mode these timers are capable of producing accurate delays over a very wide range. In the astable mode a wide frequency coverage is coupled with variable duty cycle capability. These versatile devices provide effective solutions for many timing and pulse circuit applications. The 556 timer is a dual version of the 555 single timer. The C-MOS versions offer improved characteristics for particular applications. For further information on 555 timers and their applications, please refer to the Technical Library section of the current **RS** catalogue for suitable reference books.

Absolute maximum ratings - bipolar

Supply voltage	+18V
Output current	200mA
Power dissipation	600mW
Operating temperature	0 to +70°C
Storage temperature	–65 to +150°C
Lead temperature (60 sec)	+300°C

Features

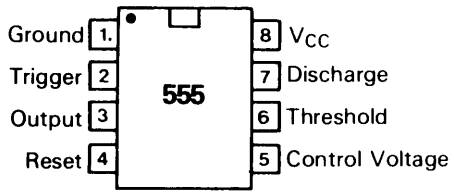
- Bipolar and C-MOS versions
- Low external component count
- Wide operating voltage range
- Low power and supply current.

Absolute maximum ratings - C-MOS

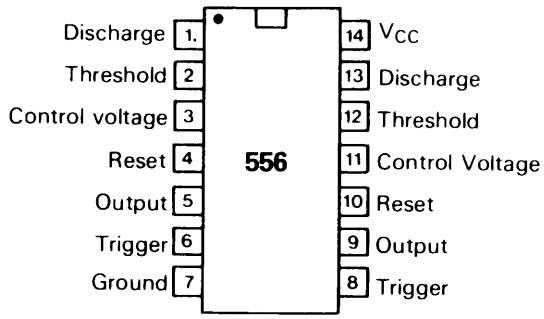
Supply voltage	+18V
Output current	100mA
Power dissipation, 555	200mW
556	300mW
Operating temperature	0 to +70°C
Storage temperature	-65 to +150°C
Lead temperature (60 sec)	+300°C

Note: Due to the SCR structure inherent in the C–MOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ +0.3V or less than V^- -0.3V may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supplyis established. In multiple systems, the supply of the C-MOS IC must be turned on first.

Bipolar pin out diagrams

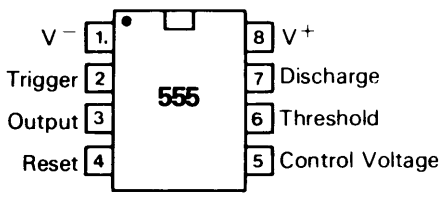


TOP VIEW

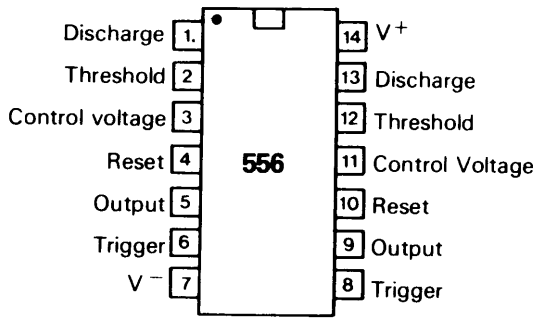


TOP VIEW

C-MOS pin out diagrams



TOP VIEW

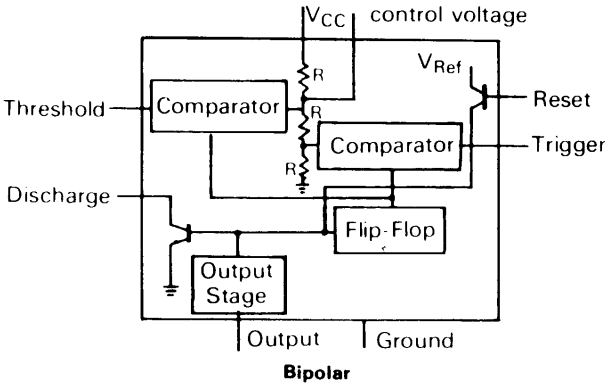


TOP VIEW

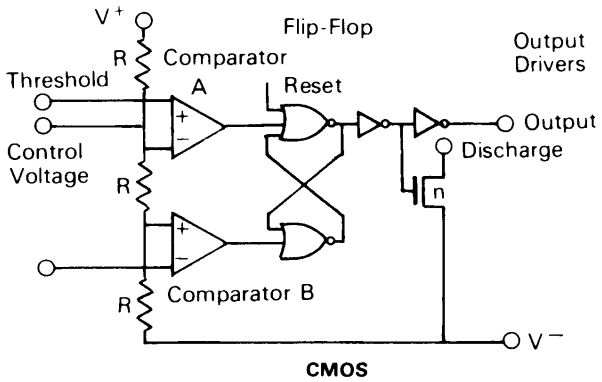
Electrical characteristics bipolar $T_A = 25°C$, $V_{CC} = 5$ to 15V unless specified

Parameter	Test Conditions	556			555			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage		4.5		16	4.5		16	V
Supply Current	$V_{CC} = 5$ V $R_L = \infty$		6	12		3	6	mA
	$V_{CC} = 15$ V $R_L = \infty$		20	30		10	15	mA
Timing Error (astable)	$R_A, R_B = 1$ kΩ to 100 kΩ							
	C = 0.1µF							
Initial accuracy	$V_{CC} = 15$V		2.25			2.25		%
Drift with temperature			150			150		ppm/°C
Drift with supply voltage			0.3					%/Volt
Threshold Voltage			2/3 V_{CC}			2/3 V_{CC}		V
Threshold Current (Ith)			30	100		100	250	nA
Trigger Voltage			$V_{CC}/3$			$V_{CC}/3$		V
Trigger Current			0.5			0.5		µA
Reset Voltage		0.4	0.7	1.0		0.7	1.0	V
Reset Current			0.1			0.1		mA
Control Voltage Level	$V_{CC} = 15$ V	9.0	10	11		10	11	V
	$V_{CC} = 5$V	2.6	3.33	4		3.33	4	V
Output Voltage (low)	$V_{CC} = 15$V $I_{SINK} = 10$mA		0.1	.25		0.1	.25	
	$I_{SINK} = 50$mA		0.4	.75		0.4	.75	V
	$I_{SINK} = 100$ mA		2.0	3.2		2.0	.25	V
	$V_{CC} = 5$V $I_{SINK} = 5$mA		.15	.25		.25	.35	V
Output Voltage (high)	$V_{CC} = 15$V $I_{SOURCE} = 100$ mA	12.75	13.3		12.75	13.3		V
	$I_{SOURCE} = 200$mA		12.5			12.5		
	$V_{CC} = 5$V $I_{SOURCE} = 100$mA	2.75	3.3		2.75	3.3		V
Rise Time of Output 10% to 90%		100			100		ns	
Fall Time of Output 10% to 90%		100			100		ns	
Discharge Leakage Current		20	100				nA	
Timing error (monostable)	$R_A = 2$kΩ to 100kΩ							
	C = 0.1µF							
Initial accuracy		0.75	3.0		1.0	3.0	%	
Drift with temperature		50			50		ppm/°C	
Drift with supply voltage		0.1	0.5		0.1	0.5	%/Volt	

Figure 1 Schematic diagrams



Bipolar



CMOS

Electrical characteristics - C-MOS T_A = 25°C, V+ to V- = 2V to 15V unless specified

Parameter	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	–20°C<T_A<+70°C	2		18	V
Supply Current	V^+ to V^- = 2V (555)		0.06	0.2	mA
	V^+ to V^- = 18V (555)		0.12	0.3	mA
	V^+ to V^- = 2V (556)		0.12	0.4	mA
	V^+ to V^- = 18V (556)		0.24	0.6	mA
Timing Error (astable)	R_A, R_B = 1 to 100 k C = 0.1µF				
Initial accuracy			2.0		%
Drift with temperature			50		ppm/°C
Drift with supply voltage	V^+ to V^- = 5V		1.0		%/Volt
Threshold Voltage			2/3 V+		V
Threshold Current (I_{th})	V^+ to V^- = 5V		0.01		nA
Trigger Voltage			V+/3		V
Trigger Current	V^+ to V^- = 5V		10		pA
Reset Voltage		0.4	0.7	1.0	V
Reset Current	V^+ to V^- = 5V		20		pA
Control Voltage Level	V^+ to V^- = 15V		10		V
	V^+ to V^- = 5V		3.33		V
Output Voltage (low)	I_{SINK} = 3.2mA				
	V^+ to V^- = 18V		0.1	0.4	V
	V^+ to V^- = 5V		0.15	0.4	V
Output Voltage (high)	V^+ to V^- = 18V, I_{SOURCE} = 1.0mA	17.25	17.8		V
	V^+ to V^- = 5V, I_{SOURCE} = 1.0mA	4.0	4.5		V
Rise Time of Output 10% to 90%	R_L = 10MΩ C_L = 7pF		40		ns
Fall Time of Output 10% to 90%	V^+ to V^- = 5V		40		ns
Discharge Leakage Current					nA
Timing error (monostable)	R_A, R_B = 1k to 100k C = 0.1µF				
Initial accuracy			2.0		%
Drift with temperature			50		ppm/°C
Drift with supply voltage	V^+ to V^- = 5V		1.0		%/Volt

Figure 2 Basic modes of operation

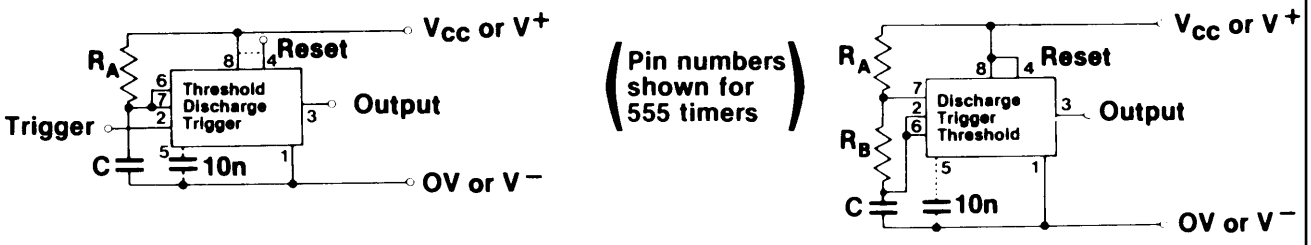
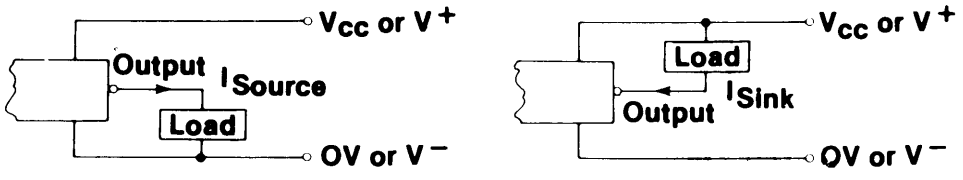


Figure 3 Load connection options



Operation

Trigger input

This input is used to initiate a monostable timing period. Triggering occurs on the negative going edge AB of the pulse shown in the diagram below, at a voltage level less that 1/3 of the V_{CC} or V^+ supply rail. The trigger pin must be returned to a level above 1/3 of the OV or V^- supply rail before the end of the set timing period 'T'. Should the trigger pulse interval 't' be greater than the timing period 'T' then the output will remain in the active state (output high) for time 't'. Once triggered the trigger input is disabled and any trigger pulses occurring during the timing period 'T' have no effect on the set time.

The necessity to return the trigger input to a voltage above 1/3 of the OV or V^- rail and because the trigger input impedance is very high and hence susceptible to external noise, a.c. coupling of this pin is desirable. The figure below shows an arrangement for a.c. coupling of the trigger input.

Figure 4a

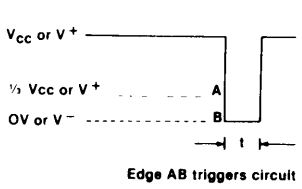
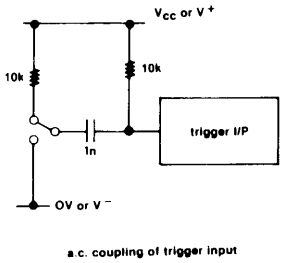


Figure 4b

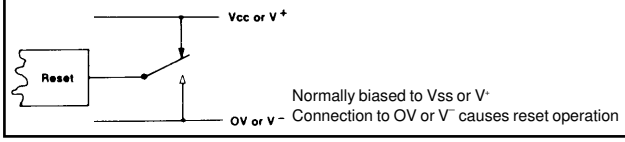


The minimum pulse width required for triggering and propagation delay versus voltage of trigger pulse are shown in Figure 6 for both the bipolar and C-Mos timers.

Reset input

The reset function is used to return the timer output to the steady state (output low) when interruption of a monostable timing period is required. When not required the reset should be connected to V_{CC} or V^+. This avoids a false reset occurring.

Figure 5 **Reset input**



Control voltage

As can be seen from the timer schematics on Page 2 the open circuit voltage at the control pin is set at 2/3 V_{CC} or V^+ by the internal resistors R. This resistor network sets the threshold comparator trip level at 2/3 supply and the trigger comparator at 1/3 supply. By imposing an external voltage on this pin the comparator reference levels may be shifted above or below the nominal levels hence affecting the timing in both the monostable and astable modes. In the monostable mode this pin can be swung between 45% to 90% of V_{CC} or V^+. In the astable mode a variation of 33% to 100% of the supply rail is possible. This feature extends the versatility of the timer to voltage controlled oscillators, pulse width modulators etc.

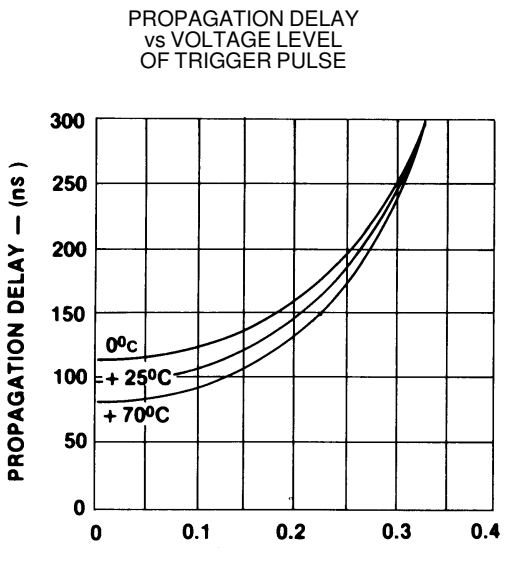
For applications where this facility is not required the control voltage terminal should be decoupled to OV by a 10nF capacitor.

The C-MOS IC's, in most applications, will not require the control voltage terminal to be decoupled and should be left unconnected.

Output

The output voltage dependence on load current in sink and source modes is shown in Figure 2.

Figure 6a **Input characteristics - bipolar 555, 556**



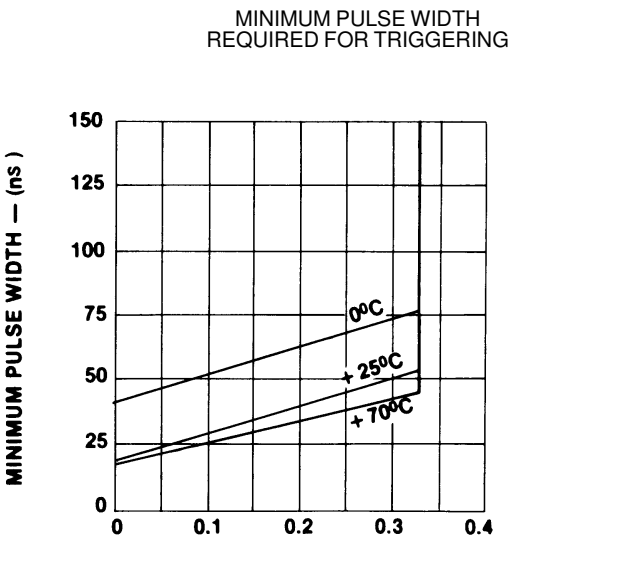
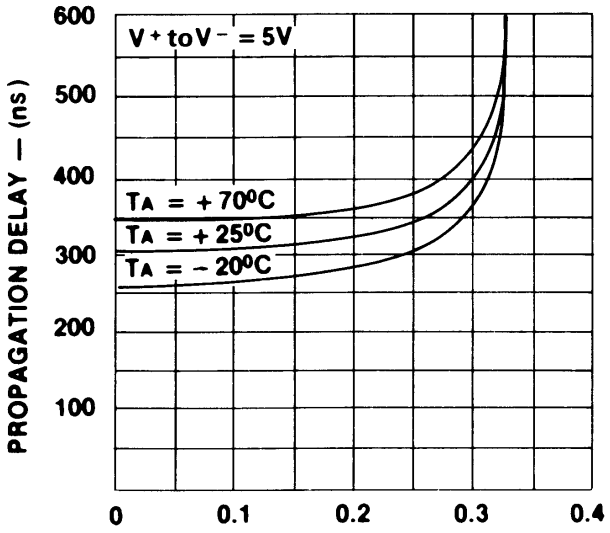


Figure 6b Input characteristics - C-MOS 555, 556

PROPAGATION DELAY
AS A FUNCTION OF
VOLTAGE LEVEL OF TRIGGER PULSE



MINIMUM PULSE WIDTH
REQUIRED FOR TRIGGERING

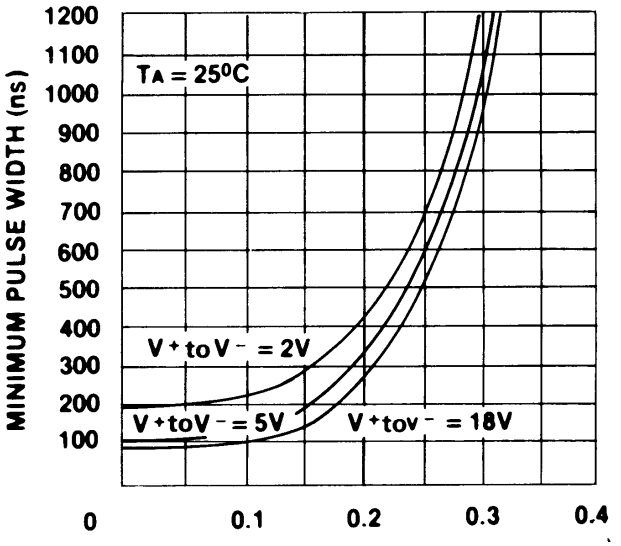
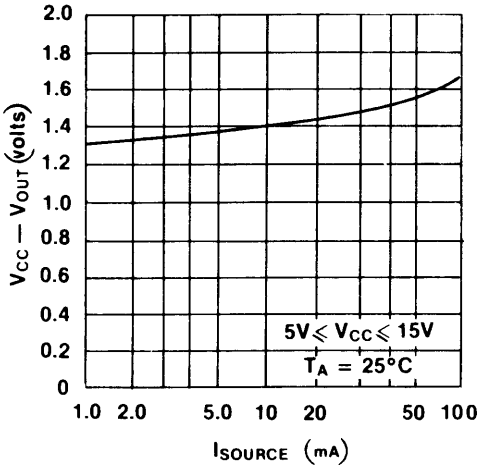


Figure 7a Output characteristics - bipolar 555, 556

HIGH OUTPUT VOLTAGE DROP
vs OUTPUT SOURCE CURRENT



LOW OUTPUT VOLTAGE
vs OUTPUT
SINK CURRENT

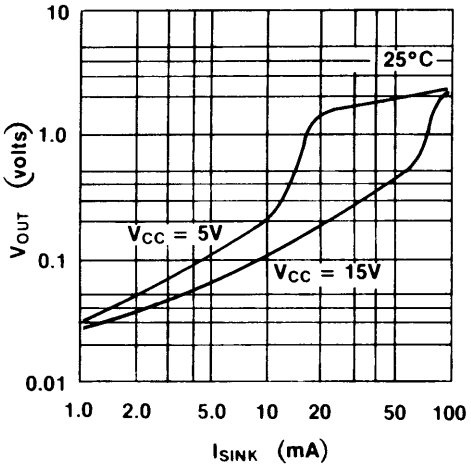
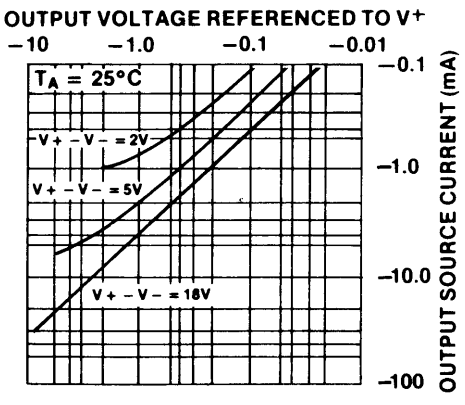
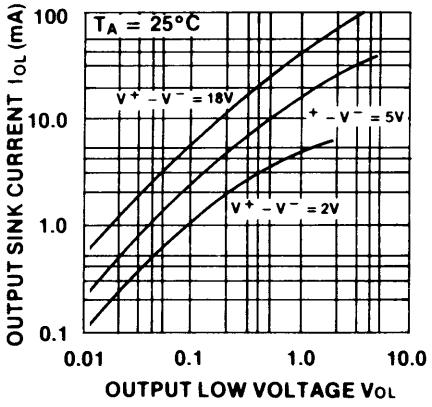


Figure 7b Output characteristics - C-MOS 555, 556

OUTPUT SOURCE CURRENT AS A
FUNCTION OF OUTPUT VOLTAGE



OUTPUT SINK CURRENT AS A
FUNCTION OF OUTPUT VOLTAGE



Timing formulae
Monostable operation:

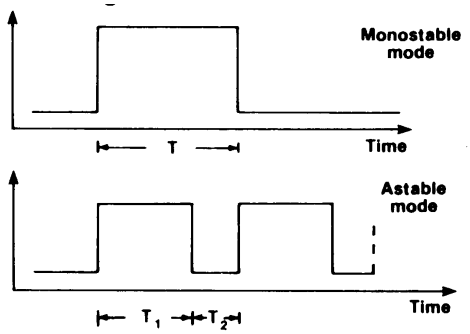
$T \approx 1.1\, R_A C$ sec C in F R_A in Ω

Astable operation:

$T_1 \approx 0.1\,(R_A + R_B)C$ sec C in F R_A & R_B in Ω
$T_2 \approx 0.7\, R_B C$ sec

$$f = \frac{1}{T_1 + T_2} \approx \frac{1.44}{(R_A + 2R_B)C} \text{ Hz}$$

Figure 8 Timing modes



The minimum recommended values for the timing resistors are R_A = 5kΩ & R_B = 3kΩ. These values are consistent with reliable operation at extremes of supply voltage, however, at intermediate levels lower value resistors may prove satisfactory.

The maximum value of these resistors is governed by the typical value of threshold current and varies for each of the timers.

$$R_A \text{ max. or } (R_A + R_B)\text{max.} = \frac{0.33V_s}{I_{th} \times 10^{-9}} \quad \Omega$$

where $V_s = V_{CC}$ or V+ to V- in volts

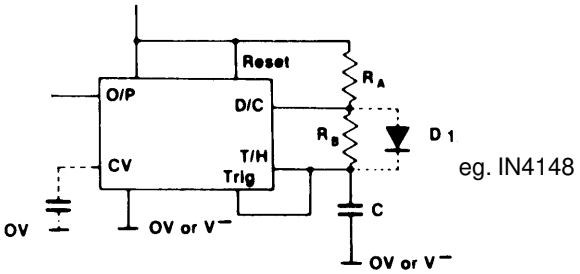
I_{th} = Threshold current in nA for the timer IC.

The duty cycle in the astable mode is:

$$\frac{T_1}{T_1 + T_2} = \frac{R_A + R_B}{R_A + 2R_B} \times 100\%$$

The minimum duty cycle using the recommended values is approximately 62%. By adding a diode across R_B the charging path for the timing capacitor C changes from $(R_A + R_B)$ to $(R_A + D_1)$ hence $t_1 < 0.7\,(R_A + R_B)$ and duty cycles from 5 to 95% are possible.

Figure 9 Duty cycle



Timing capacitor - Important

The capacitor employed must have a leakage current less than 0.1 I_{th} for satisfactory operation. Suitable types are silvered mica, polycarbonate, polystyrene, polypropylene, but not ceramic disc which are unstable in capacitance for RC network applications, or electrolytics due to high leakage current.

Technical hints

The bipolar timers have a 'totem pole' type output stage and during switching, large current spikes can appear on the supply line. Effective by-passing is necessary to eliminate noise retriggering the input and a 47μF tantalum capacitor mounted close to the device supply pins is suggested.

To prevent the possibility of double triggering when driving TTL loads a 1nF capacitor connected between the timer output and ground should be found suitable.

Applications

Figure 10 Time delay

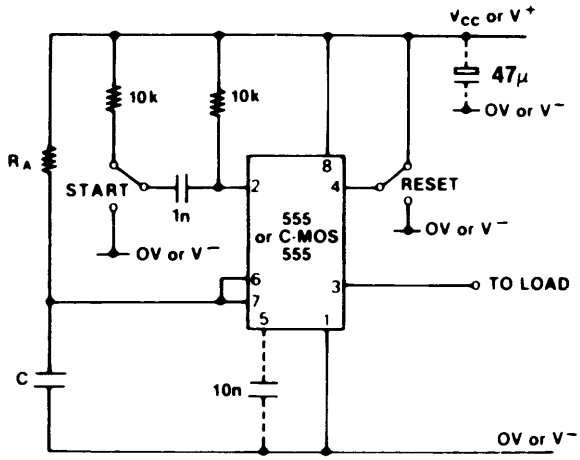


Figure 11 Load options

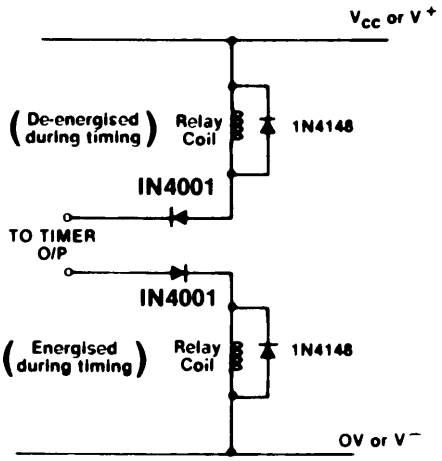
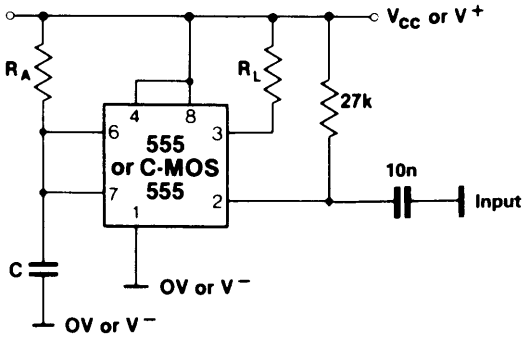


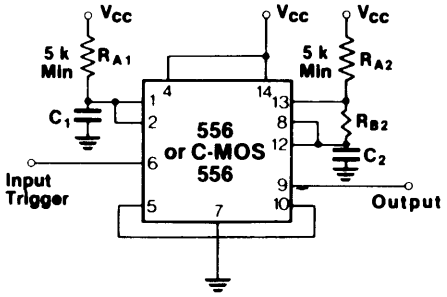
Figure 12 Touch control



The value of 27 kΩ resistor is suitable for industrial or public environments. With lower ambient noise, a higher value of resistor may be necessary.

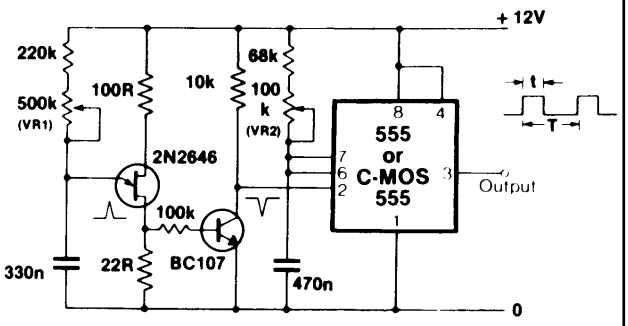
Figure 13 Tone burst generator

The 556 Dual Timer makes an excellent Tone Burst Generator. The first half is connected as a one shot and the second half as an oscillator.



The pulse established by the one shot turns on the oscillator allowing a burst of pulses to be generated

Figure 14 Simple pulse generator

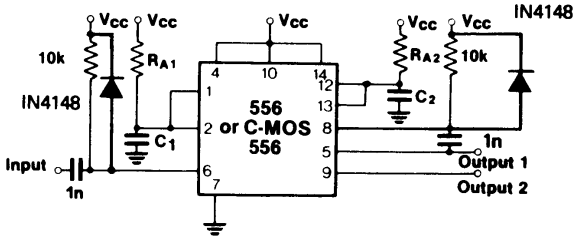


Pulse width (t) adjusted by VR2
Pulse repetition frequency ($1/_T$) adjustment by VR1
Circuit as shown gives

t = 20 → 80ms T = 100 → 250ms

Figure 15 Sequential timing

One feature of the Duel Timer is that by utilising both halves it is possible to obtain sequential timing. By connecting the output of the first half to the input of the second half via a 1nF coupling capacitor sequential timing may be obtained. Delay T_1 is determined by the first half and T_2 by the second half delay.



The first half of the timer is started by momentarily connecting pin 6 to ground. When it has timed out (determined by 1.1 $R_{A1}C_1$) the second half begins.
(Its time duration is determined by 1.1 $R_{A2}C_2$).

Figure 16 Missing pulse detector

Using the circuit shown below, the timing cycle is continuously reset by the pulse train. A change in frequency, or a missing pulse, allows completion of the timing cycle which causes a change in the output level. For this application, the time delay should be set to be slightly longer than the normal time between pulses.

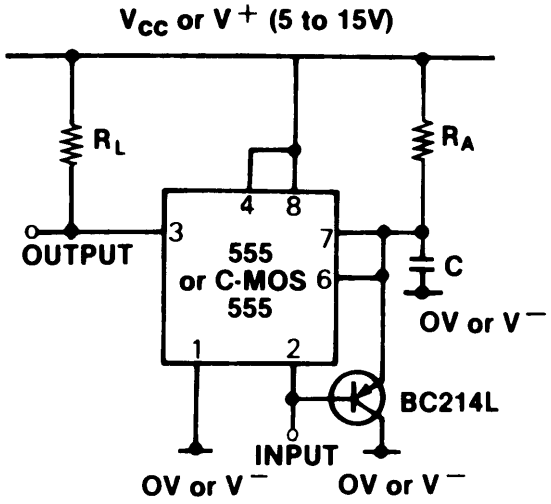


Figure 17 Pulse width modulation (PWM)

In this application, the timer is connected in the monostable mode as shown below. The circuit is triggered with continuous pulse train and the threshold voltage is modulated by the signal applied to the control voltage terminal (pin 5). This has the effect of modulating the pulse width as the control voltage varies.

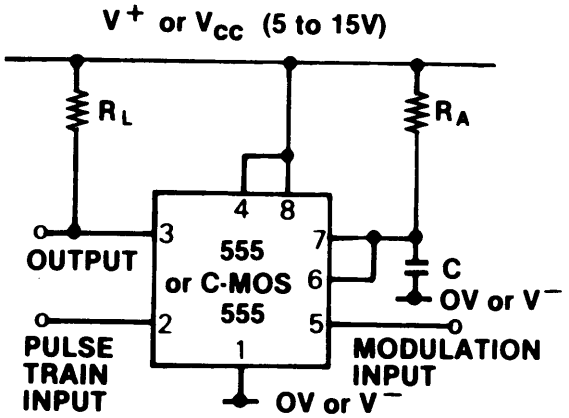


Figure 18 **Pulse position modulation (PPM)**
This application uses the timer connected for astable (free-running) operation, shown below, with a modulating signal again applied to the control terminal. Now the pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied.

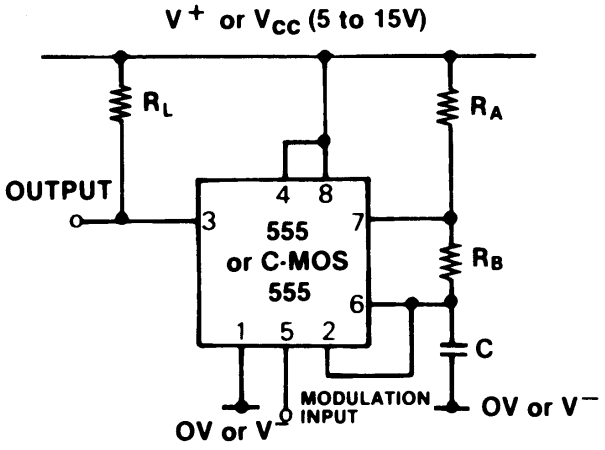


Figure 19a **Tachometer circuit**

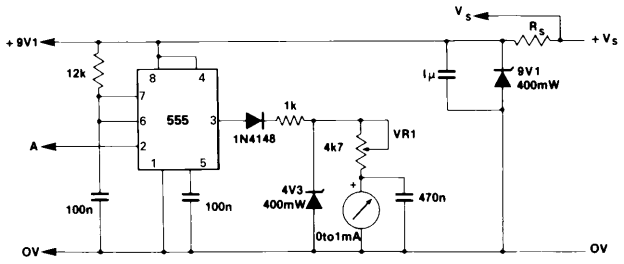
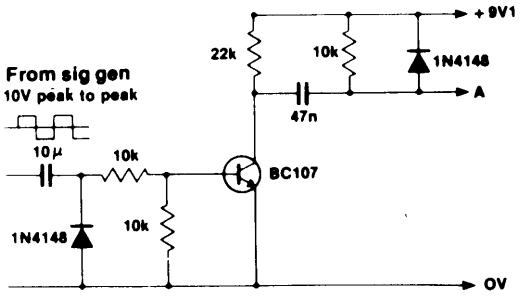


Figure 19b **Calibration interface**



To calibrate: adjust VR1 for known reading against signal generator using circuit shown and values in table.

Minimum input pulses from slotted opto switch or Proximity detector should be > 1ms.	At slow speeds needle will flicker. For very slow speeds use more than one hold on disc and multiply reading in table by number of holes.

Rpm	Tachometer pulse per sec (or Hz on sig. gen.)
600	10
1200	20
2400	40
3600	60
6000	100

Figure 20a **Interface with inductive proximity detector**

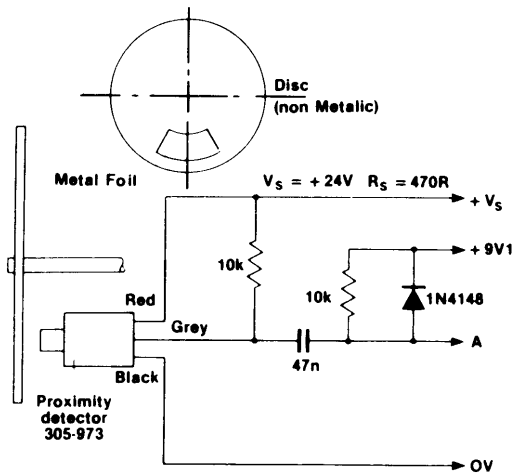


Figure 20b **Interface for use with slotted opto switch**