JEDEC STANDARD

Electrostatic Discharge (ESD) Sensitivity Testing, Machine Model (MM)

JESD22-A115C

(Revision of JESD22-A115B, March 2010)

NOVEMBER 2010

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or call (703) 907-7559 or www.jedec.org

Published by
©JEDEC Solid State Technology Association 2010
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

PRICE: Refer to www.jedec.org

Printed in the U.S.A.

PLEASE!

DON'T VIOLATE
THE
LAW!

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107
or call (703) 907-7559

SPECIAL NOTE

- **JESD22-A115 is a reference document; it is not a requirement per JESD47 (Stress Test Driven Qualification of Integrated Circuits).**

- **Machine Model as described in JESD22-A115 should not be used as a requirement for integrated circuit ESD qualification.**

- **Only HBM and CDM are the necessary ESD qualification test methods as specified in JESD47.**

TEST METHOD A115C

ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING, MACHINE MODEL (MM)

(From JEDEC Board Ballot JCB-97-10, and JCB-10-13, and JCB-10-60, formulated under the cognizance of JC-14.1 Committee on Reliability Test Methods for Packaged Devices.)

1 Scope

This method establishes a standard procedure for testing microcircuits using an electrostatic discharge (ESD) model known commonly in the industry as the Machine Model (MM). The objective is to provide reliable, repeatable MM ESD test results. There is limited data supporting the ability of this model to simulate discharges of machinery or to establish manufacturing handling practices. However, the model is useful for producing human-body model (HBM)-like ESD effects at lower voltages and for failure mode determination. The method produces results with are closely related to HBM and produces similar failure modes.

2 Apparatus

This test method requires the following equipment.

2.1 Simulator

An ESD Pulse Simulator and a Device Under Test (DUT) socket equivalent to the circuit of Figure 1. The simulator must be capable of supplying pulses with the characteristics required by Figure 2 and Figure 3.

2.2 Oscilloscope

The oscilloscope and amplifier combination shall have a 350 MHz minimum single-shot bandwidth and a visual writing speed of 4 cm/ns minimum.

2.3 Current probe

The current probe shall have a minimum pulse-current bandwidth of 350 MHz. A current probe (transformer and cable with a nominal length of 1 meter) with a 1 GHz bandwidth and a current rating of 12 amperes maximum pulse-current is recommended.

2.4 Evaluation Loads

An 18 AWG tinned copper wire is recommended for the short waveform verification test. The lead length should be as short as practicable to span the distance between the two farthest pins in the socket while passing through the current probe. The ends of the 18 AWG wire may be ground to a point where clearance is needed to make contact on fine pitch socket pins.

2 Apparatus (cont'd)

2.4 Evaluation Loads (cont'd)

A 500 ohm +/-1%, 1000 volt, low inductance resistor shall be used for initial system checkout and periodic system recalibration.

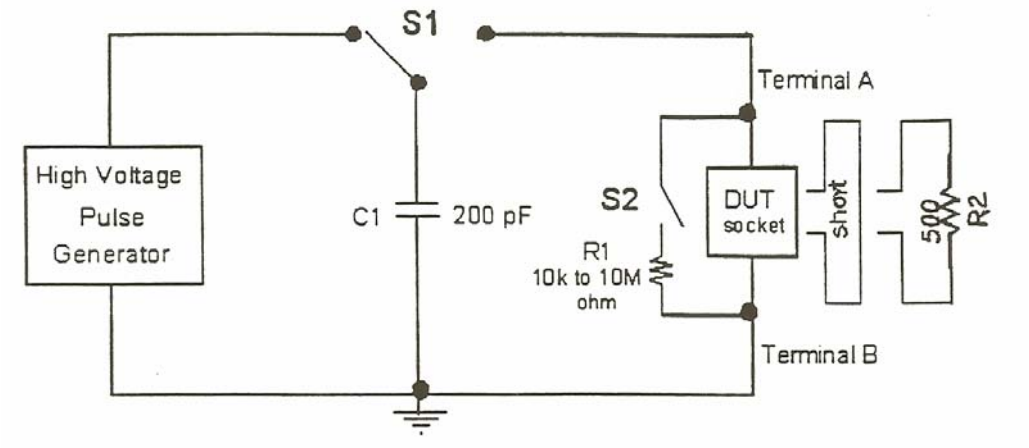

Figure 1 — Typical equivalent MM ESD circuit

NOTE 1 The performance of any simulator is influenced by its parasitic capacitance and inductance.

NOTE 2 Precautions must be taken in tester design to avoid recharge transients and multiple pulses.

NOTE 3 R2, used for initial equipment qualification and requalification as specified in 3.1, shall be a low inductance, 1000 volt, 500 ohm resistor with +/-1% tolerance.

NOTE 4 Stacking of DUT socket adaptors (piggybacking) is allowed only if the waveforms can be verified to meet the specifications in Table 1.

NOTE 5 Reversal of terminal A and B to achieve dual polarity is not permitted.

NOTE 6 S2 should be closed 10 to 100 milliseconds after the pulse delivery period to ensure the DUT socket is not left in a charged state.

NOTE 7 C1, 200 pF +/- 10%.

2 Apparatus (cont'd)

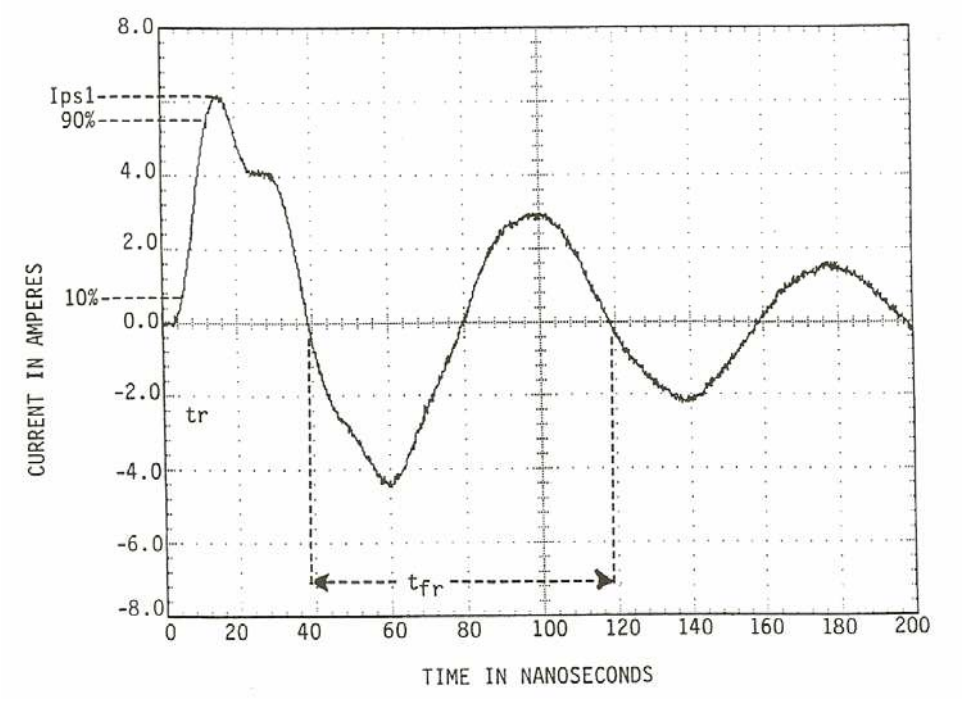

Figure 2 — Current Waveform through a shorting wire, 400 volt discharge

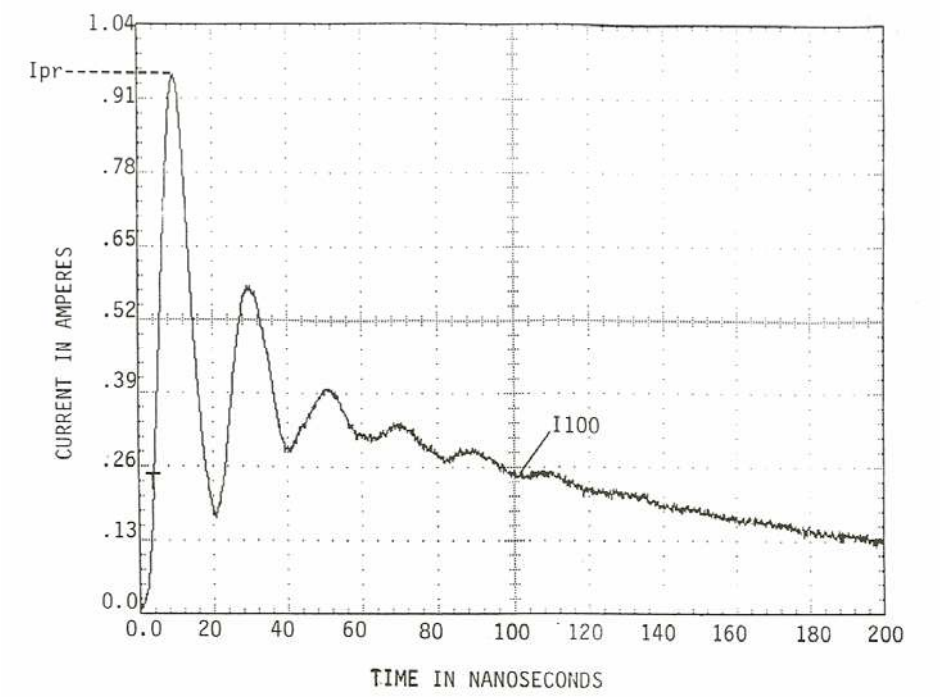

Figure 3 — Current waveform through a 500 ohm resistor, 400 volt discharge

3 Qualification, calibration, and waveform verification

3.1 Equipment qualification

Equipment calibration must be performed during initial acceptance testing. Recalibration is required whenever equipment repairs are made that may affect the waveform and a minimum of every 12 months. The tester must meet the requirements of Table 1 and Figure 2 at all voltage levels using the shorting wire and at the 400 volt level with the 500 ohm resistor (see Figure 3). The waveform measurements during calibration shall be made using the worst-case pin on the highest pin count board with a positive mechanical clamp socket. (Machine repeatability should be verified during initial equipment acceptance by performing a minimum of 5 consecutive positive and a minimum of 5 consecutive negative waveforms at a voltage level in Table 1.) The high-voltage relays and associated high-voltage circuitry shall be tested by the user of computer-controlled systems per the equipment manufacturer's instructions (system diagnostics). This test will check for any open or short relays.

Table 1 — Waveform specification

Voltage Level (V)	Positive Ipeak for Short, Ips1 (A)	Positive Ipeak for 500 Ohm* Ipr (A)	Current at 100 ns for 500 Ohm* I100 (A)	Maximum Ringing Current, I_R (A)	Resonance Frequency for Short, FR ($1/t_{fr}$) (Mhz)
100	1.5 - 2.0	N/A	N/A	Ips1 x 30%	11 - 16
200	2.8 - 3.8	N/A	N/A	Ips1 x 30%	11 - 16
400	5.8 - 8.0	I100 x 4.5 maximum	0.29+/-20%	Ips1 x 30%	11 - 16
* The 500 ohm load is used only during Equipment Qualification as specified in 3.1.					

3.1.1 Safety Training

During initial equipment set-up, the safety engineer or applicable safety representative, shall inspect the equipment in its operating location to ensure that the equipment is not operated in a combustible (hazardous) environment.

Additionally, all personnel shall receive system operational training and electrical safety training prior to using the equipment.

3 Qualification, calibration, and waveform verification (cont'd)

3.2 Worst-case pin

The worst-case pin combination for each socket and DUT board shall be identified and documented. It is recommended that the manufacturers supply the worst-case pin data with each DUT board. The pin combination with the waveform closest to the limits (see Table 1) shall be designated for waveform verification.

The worst-case pin combination shall be identified by the following procedure.

3.2.1 For each test socket, identify the socket pin with the shortest wiring path from the pulse generating circuit to the test socket. Connect this pin to Terminal B (where it will remain the referenced pin throughout the worst case pin search) and connect one of the remaining pins to Terminal A. Attach a shorting wire between these pins with the current probe around the shorting wire, as close to Terminal B as practicable.

3.2.2 Apply a positive 400 volt pulse and a negative 400 volt pulse and verify that the waveform meets the requirements defined in Table 1 for both positive and negative pulses.

3.2.3 Repeat steps 3.2.1 and 3.2.2 until all socket pins have been evaluated.

3.2.4 Determine the worst-case pin pair (within the limits and closest to the minimum or maximum parameter values as specified in Table 1) to be used for future waveform verification.

3.2.5 For initial board check-out, connect a 500 ohm resistor between the worst-case pins previously identified with the shorting wire in step 3.2.4. Apply a positive and negative 400 volt pulse and verify that the waveform meets the requirements defined in Table 1.

NOTE In case the test socket/test board has already been characterized for worst-case pin on HBM, then that pin combination is acceptable for use with MM waveform verification.

As an alternative to the worst-case pin search, the reference pin pair may be identified for each test socket of each test fixture. The reference pin combination shall be identified by determining the socket pin with the shortest wiring path from the pulse generating circuit to the test socket. Connect this pin to Terminal B and then connect the socket pin with the longest wiring path from the pulse generating circuit to the test socket to Terminal A (normally provided by the manufacturer). Attach a shorting wire between these pins with the current probe around the shorting wire. Follow the procedure in step 3.2.2. For the initial board check-out connect a 500 ohm resistor between the reference pins. Apply a positive and negative 400 volt pulse and verify that the waveform meets the parameters in Table 1.

3 Qualification, calibration, and waveform verification (cont'd)

3.3 Waveform verification

The waveform verification shall be performed at the beginning of each shift a tester is operated and when a socket/DUT board is changed. If at any time the waveforms do not meet the requirements defined in Figure 1 and Table 1 at the 400 volt level, the testing shall be halted until the waveform is in compliance. Additionally, the system diagnostics test as defined in 3.1 for automated systems shall be performed prior to the beginning of each shift testing is done. The period between waveform checks may be extended providing test data supports the increased interval. In case the waveform no longer meets the limits in Table 1, all ESD testing performed after the previous satisfactory waveform check will be considered invalid.

3.3.1 With the required DUT socket installed and with no part in the socket, attach a shorting wire in the DUT socket such that the worst-case pins are connected between Terminal A and Terminal B as shown in Figure 2. Place the current probe around the shorting wire.

3.3.2 Initiate a positive pulse at the 400 volt level per Table 1 and Figure 2. Verify that all parameters meet the limits specified in Table 1 and Figure 1.

3.3.3 Initiate a negative pulse at the 400 volt level per Table 1. Verify that all parameters meet the limits specified in Table 1 and Figure 1.

4 Characterization

The devices used for characterization testing must have completed all normal manufacturing operations.

4.1 Prior to ESD testing, dc parametric and functional testing at room temperature and, if applicable, high temperature shall be performed on all devices submitted for ESD testing. The test devices shall meet device data sheet requirements for these parameters.

4.2 A sample of 3 devices for each voltage level shall be characterized for the device ESD failure threshold using the voltage steps shown in Table 1. Finer voltage steps may optionally be used to obtain a more accurate measure of the failure threshold. ESD Testing should begin at the lowest step in Table 1. The ESD test shall be performed at room temperature.

4.3 Each sample of 3 devices shall be stressed at one voltage level using 1 positive and 1 negative pulses with a minimum of 0.5 second between pulses per pin for all pin combinations specified in Table 2. It is permitted to use a separate sample of 3 devices for each pin combination specified in Table 2. It is permitted to use the same sample (3) at the next higher voltage stress level if all parts pass the failure criteria specified in clause 5 after ESD exposure to a specified voltage level.

4 Characterization (cont'd)

4.4 Pin combinations, the pin combinations to be used are given in Table 2. The actual number of pin combinations depends on the number of power pin groups. Like named power pins (VCC1, VCC2, VSS1, VSS2, GND, etc.) that are directly connected by metal (inside the package) may be tied together and treated as one pin for Terminal B connection. Otherwise, each power pin must be treated as a separate power pin. Programming pins that do not draw current should be considered as I/O pins (example: Vpp pins on memory devices). Active discrete devices (FETs, transistors, etc.) shall be tested using all possible pin-pair combinations (one pin connected to Terminal A, another pin connected to Terminal B) regardless of pin name or function. All pins configured as "no connect" pins shall be verified as "no-connect" and left open (floating) at all times. Pins labeled "no-connect", that in fact are connected, shall be tested as non-supply pins.

Table 2 — Pin Combinations for Integrated Circuits

Pin Combination	Connect Individually to Terminal A	Connect to Terminal B (Ground)	Floating Pins (unconnected)
1	All pins one at a time, except the pin(s) connected to Terminal B	First power pin(s)	All pins except 1/PUT* and first power pin(s)
2	All pins one at a time, except the pin(s) connected to Terminal B	Second power pin(s)	All pins except PUT and second power pin(s)
3	All pins one at a time, except the pin(s) connected to Terminal B	Nth power pin(s)	All pins except PUT and Nth power pin(s)
4	Each Non-supply pin, one at a time	All other Non-supply pins collectively except PUT	All power pins
* 1/PUT - Pin under test.			

4.5 If a different sample group is ESD tested at each stress level, it is permitted to perform the dc parametric and functional ATE testing after all sample groups have been ESD tested.

5 Failure criteria

A part will be defined as a failure if, after exposure to ESD pulses, it no longer meets the device data sheet requirements using parametric and functional testing. If testing is required at multiple temperatures, testing shall be performed at the lowest temperature first.

Annex A (informative) Differences between JESD22-A115C and JESD22A-115B

This table briefly describes most of the changes made to entries that appear in this standard, JESD22-A115C, compared to its predecessor, JESD22-A115B (March 2010). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Clause	Description of Change
Cover	Added a “Special Note” to the forth page of the document

A.1 Differences between JESD22-A115B and JESD22A-115-A

Clause	Description of Change
1	Modified Scope to give users a better understanding of the relative merits and status of machine Model 9MM) testing.
4	Changed title from Classification testing to Characterization
4	First paragraph, replaced classification with characterization
6	This clause was removed in this revision.

Standard Improvement Form **JEDEC JESD22-A115C**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

JEDEC
Attn: Publications Department
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

Fax: 703.907.7583

1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

_____

Submitted by

Name: _____ Phone: _____

Company: _____ E-mail: _____

Address: _____

City/State/Zip: _____ Date: _____


JEDEC