### **General Description**

The MAX1480A/MAX1480B/MAX1480C/MAX1490A/ MAX1490B are complete, electrically isolated, RS-485/ RS-422 data-communications interface solutions in a hybrid microcircuit. Transceivers, optocouplers, and a transformer provide a complete interface in a standard DIP package. A single +5V supply on the logic side powers both sides of the interface.

The MAX1480B/MAX1480C/MAX1490B feature reducedslew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission at data rates up to 250kbps. The MAX1480A/MAX1490A driver slew rate is not limited, allowing transmission rates up to 2.5Mbps. The MAX1480A/B/C are designed for half-duplex communication, while the MAX1490A/B feature full-duplex communication.

Drivers are short-circuit current limited and protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into a highimpedance state. The receiver input has a fail-safe feature that guarantees a known output (RO low for the MAX1480A/B/C, RO high for the MAX1490A/B/C) if the input is open circuit.

The MAX1480A/MAX1480B/MAX1480C/MAX1490A/ MAX1490B typically withstand 1600V<sub>RMS</sub> (1 minute) or 2000V<sub>RMS</sub> (1 second). Their isolated outputs meet all RS-485/RS-422 specifications. The MAX1480A/B/C are available in a 28-pin DIP package, and the MAX1490A/B are available in a 24-pin DIP package.

#### **Applications**

Isolated RS-485/RS-422 Data Interface

Transceivers for EMI-Sensitive Applications

Industrial-Control Local Area Networks

Automatic Test Equipment

HVAC/Building Control Networks

### \_Next-Generation Device Features

- For Integrated ESD Protection MAX1480E/MAX1490E: ±15kV ESD-Protected, Isolated RS-485/RS-422 Data Interfaces
- For Space-Constrained Applications MAX3157: High CMRR, RS-485 Transceiver with ±50V Isolation

#### **Ordering Information**

PART <sup>†</sup>	TEMP RANGE	PIN-PACKAGE
MAX1480ACPI	0°C to +70°C	28 Wide Plastic DIP
MAX1480AEPI	-40°C to +85°C	28 Wide Plastic DIP

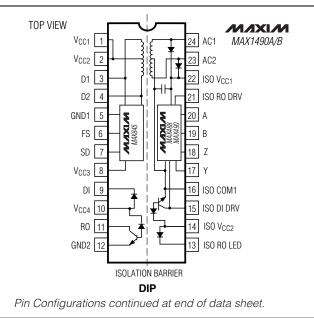
Ordering Information continued at end of data sheet.

<sup>†</sup>Data rate for "A" parts is up to 2.5Mbps. Data rate for "B" and "C" parts is up to 250kbps.

### **Selection Table**

PART	HALF/ FULL DUPLEX	FULL RATE		DRIVER ENABLE TIME (µS)
MAX1480A	Half	2.5	No	0.2
MAX1480B	Half	0.25	Yes	35
MAX1480C	Half	0.25	Yes	0.5
MAX1490A	Full	2.5	No	
MAX1490B	Full	0.25	Yes	—

### **Pin Configurations**



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\_ Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

### **ABSOLUTE MAXIMUM RATINGS**

With Respect to GND\_

Supply Voltage (V <sub>CC</sub> )0.3V to +6V	
Control Input Voltage (SD, FS)0.3V to (V <sub>CC</sub> + 0.3V)	
Receiver Output Voltage ( $\overline{RO}$ , $RO$ )0.3V to ( $V_{CC}$ + 0.3V)	
Output Switch Voltage (D1, D2)+12V	
With Respect to ISO COM_	
Control Input Voltage (ISO DE_)0.3V to (ISO V <sub>CC</sub> + 0.3V)	
Driver Input Voltage (ISO DI_)0.3V to (ISO V <sub>CC</sub> + 0.3V)	
Receiver Output Voltage (ISO RO_)0.3V to (ISO V <sub>CC</sub> + 0.3V)	
Driver Output Voltage (A, B, Y, Z)8V to +12.5V	
Receiver Input Voltage (A, B)8V to +12.5V	

LED Forward Current (DI, DE, ISO RO LED)	50mA
Continuous Power Dissipation ( $T_A = +70^{\circ}C$ )	
24-Pin Plastic DIP (derate 8.7mW°C above	e +70°C)696mW
28-Pin Plastic DIP (derate 9.09mW/°C abo	ve +70°C)727mW
Operating Temperature Ranges	
MAX1480_CPI/MAX1490_CPG	0°C to +70°C
MAX1480_EPI/MAX1490_EPG	40°C to +85°C
Storage Temperature Range	65°C to +160°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS**

 $(V_{CC} = 5V \pm 10\%, V_{FS} = V_{CC}, T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{CC} = 5V$  and  $T_A = +25^{\circ}C$ .) (Notes 1, 2)

PARAMETER	SYMBOL	COND	ITIONS	MIN	ТҮР	MAX	UNITS
	fswL	V <sub>FS</sub> = 0V			535		
Switch Frequency	fswh	$FS = V_{CC}$ or open			725		kHz
		MAX1480A,	$R_L = \infty$ , +25°C only		60	90	
		$DE' = V_{CC}$ or open	$R_L = 54\Omega$		120		
		MAX1480B,	$R_L = \infty$ , +25°C only		35	45	
		$DE' = V_{CC}$ or open	$R_L = 54\Omega$		95		
Operating Supply Current	Icc	MAX1480C,	$R_L = \infty$ , +25°C only		35	75	mA
Operating Supply Current	ICC	$DE' = V_{CC}$ or open	$R_L = 54\Omega$		95		IIIA
		MAX1490A	$R_L = \infty$ , +25°C only		100	150	
		MAX 1490A	$R_L = 54\Omega$		170		
	MAX	MAX1490B	$R_L = \infty$ , +25°C only		65	125	
		$R_{L} = 54\Omega$	$R_L = 54\Omega$		130		
Shutdown Supply Current (Note 3)	ISHDN	$SD = V_{CC_{-}}$			0.2		μA
	Vsdh	High		2.4			
Shutdown Input Threshold	V <sub>SDL</sub>	Low				0.8	V
Shutdown Input Leakage Current					10		рА
	VFSH	High		2.4			v
FS Input Threshold	V <sub>FSL</sub>	Low				0.8	
FS Input Pullup Current		FS low				50	μA
FS Input Leakage Current		FS high			10		рА
Input High Voltage	VIH	DE´, DI´		V <sub>CC</sub> 0	.4		V
Input Low Voltage	VIL	DE´, DI´				0.4	V
Isolation Resistance	RISO	$T_A = +25^{\circ}C, V_{ISO} = 50$	OVDC	100	10,000		MΩ
Isolation Capacitance	C <sub>ISO</sub>	$T_A = +25^{\circ}C, V_{ISO} = 50$	OVDC		10		pF
Differential Driver Output (No Load)	VOD1					8	V

### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{CC_} = 5V \pm 10\%, V_{FS} = V_{CC_}, T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{CC_} = 5V$  and  $T_A = +25^{\circ}C$ .) (Notes 1, 2)

PARAMETER	SYMBOL		CONDIT	IONS	MIN	ТҮР	MAX	UNITS
Differential Driver Output		$R = 50\Omega$ (RS	-422)		2			V
(With Load)	V <sub>OD2</sub>	$R = 27\Omega$ (RS	-485), Figu	re 4	1.5		5.0	V
Change in Magnitude of		$R = 27\Omega \text{ or } 5$	0Ω,	Differential			0.3	
Differential Output Voltage for Complementary Output States	$\Delta V_{OD}$	Figure 4	,	Common mode			0.3	V
Driver Common-Mode Output Voltage	Voc	$R = 27\Omega \text{ or } 5$	ίο $\Omega$ , Figure	4			4	V
			1/101 - 12	, MAX1480A/B/C			1	
Input Current (A. D)		DE' = 0V,		MAX1490A/B			0.25	mA
Input Current (A, B)		$ \text{SO I}_{\text{IN}}  = 0 \text{V}_{\text{CC}_{-}} = 0 \text{V}_{\text{or 5.5V}}$	N//Y1/8///B//	MAX1480A/B/C			0.8	
						0.2		
Pagaiver Input Pagistones	Dui	7////	10\/	MAX1480A/B/C	48			kΩ
Receiver Input Resistance	R <sub>IN</sub>	$-7V \le V_{CM} \le$	IZV	MAX1490A/B	12			
Receiver Differential Threshold Voltage	V <sub>TH</sub>	$-7V \le V_{CM} \le$	12V		-0.2		+0.2	V
Receiver Input Hysteresis	$\Delta V_{TH}$	$V_{CM} = 0V$				70		mV
Receiver Output/Receiver Output Low Voltage	V <sub>OL</sub>	Using resistor values listed in Tables 1 and 2				0.4	V	
Receiver Output/Receiver Output High Current	ЮН	V <sub>OUT</sub> = 5.5V				250	μA	
Driver Short-Circuit Current	ISO I <sub>OSD</sub>	$-7V \le V_0 \le 12$	2V (Note 4)			100		mA

### SWITCHING CHARACTERISTICS-MAX1480A/MAX1490A

 $(V_{CC} = 5V \pm 10\%, FS = V_{CC}, T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{CC} = 5V$  and  $T_A = +25^{\circ}C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNITS
Driver Input to Output	t <sub>PLH</sub>	Figures 5 and 7, $R_{DIFF} = 54\Omega$ , $C_{L1} = C_{L2}$		100	275	
Propagation Delay	<b>t</b> PHL	= 100pF		100	275	ns
Driver Output Skew	<b>t</b> SKEW	Figures 5 and 7, $R_{DIFF}$ = 54 $\Omega$ , $C_{L1}$ = $C_{L2}$ = 100pF		25	90	ns
Driver Rise or Fall Time	t <sub>R,</sub> t <sub>F</sub>	Figures 5 and 7, RDIFF = 54 $\Omega$ , CL1 = CL2 = 100pF		15	40	ns
Driver Enable to Output High (MAX1480A Only)	tzн	Figures 6 and 8, $C_L$ = 100pF, S2 closed		0.2	1.5	μs
Driver Enable to Output Low (MAX1480A Only)	tzL	Figures 6 and 8, $C_L$ = 100pF, S1 closed		0.2	1.5	μs
Driver Disable Time from Low (MAX1480A Only)	tLZ	Figures 6 and 8, $C_L$ = 15pF, S1 closed		0.2	1.5	μs
Driver Disable Time from High (MAX1480A Only)	t <sub>HZ</sub>	Figures 6 and 8, $C_L$ = 15pF, S2 closed		0.2	1.5	μs
Receiver Input to Output	t <sub>PLH</sub>	Figures 5 and 10, $R_{DIFF} = 54\Omega$ , $C_{L1} = C_{L2}$		100	225	ns
Propagation Delay	t <sub>PHL</sub>	= 100pF		100	225	115



### SWITCHING CHARACTERISTICS-MAX1480A/MAX1490A (continued)

(V<sub>CC</sub> = 5V ±10%, FS = V<sub>CC</sub>, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at V<sub>CC</sub> = 5V and T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	МАХ	UNITS
It <sub>PLH</sub> - t <sub>PHL</sub> I Differential Receiver Skew	<sup>t</sup> SKD	Figures 5 and 10, R <sub>DIFF</sub> = 54 $\Omega$ , C <sub>L1</sub> = C <sub>L2</sub> = 100pF		20		ns
Maximum Data Rate	fMAX	tPLH, tPHL < 50% of data period	2.5			Mbps
Time to Shutdown	<b>t</b> SHDN			100		μs
Shutdown to Driver Output High	tzh(shdn)	Figures 6 and 9, $C_L$ = 100pF, S2 closed		3	10	μs
Shutdown to Driver Output Low	tzl(SHDN)	Figures 6 and 9, $C_L$ = 100pF, S1 closed		3	10	μs

### SWITCHING CHARACTERISTICS-MAX1480B/MAX1480C/MAX1490B

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	МАХ	UNITS
Driver Input to Output	tplh	Figures 5 and 7, $R_{DIFF}$ = 54 $\Omega$ ,		2	3.0	μs
Propagation Delay	<b>t</b> PHL	$C_{L1} = C_{L2} = 100 pF$		2	3.0	μδ
Driver Output Skew	<sup>t</sup> SKEW	Figures 5 and 7, $R_{DIFF} = 54\Omega$ , $C_{L1} = C_{L2} = 100 pF$		900	1600	ns
Driver Rise or Fall Time	t <sub>R,</sub> t <sub>F</sub>	Figures 5 and 7, $R_{DIFF} = 54\Omega$ , $C_{L1} = C_{L2} = 100 pF$		1.0	2.0	μs
Driver Enable to Output High (MAX1480B Only)	tzн	Figures 6 and 8, $C_L$ = 100pF, S2 closed		35	100	μs
Driver Enable to Output Low (MAX1480B Only)	tzL	Figures 6 and 8, $C_L$ = 100pF, S1 closed		35	100	μs
Driver Disable Time from Low (MAX1480B Only)	tLZ	Figures 6 and 8, $C_L$ = 15pF, S1 closed		13	50	μs
Driver Disable Time from High (MAX1480B Only)	t <sub>HZ</sub>	Figures 6 and 8, $C_L$ = 15pF, S2 closed		13	50	μs
Driver Enable to Output High (MAX1480C Only)	tzн	Figures 6 and 8, $C_L$ = 100pF, S2 closed		0.5	4.5	μs
Driver Enable to Output Low (MAX1480C Only)	t <sub>ZL</sub>	Figures 6 and 8, C <sub>L</sub> = 100pF, S1 closed		0.5	4.5	μs

 $(V_{CC} = 5V \pm 10\%, FS = V_{CC}, T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{CC} = 5V$  and  $T_A = +25^{\circ}C$ .)

#### SWITCHING CHARACTERISTICS—MAX1480B/MAX1480C/MAX1490B (continued)

 $(V_{CC_{-}} = 5V \pm 10\%, FS = V_{CC_{-}}, T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{CC_{-}} = 5V$  and  $T_A = +25^{\circ}C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Disable Time from Low (MAX1480C Only)	t <sub>LZ</sub>	Figures 6 and 8, $C_L$ = 15pF, S1 closed		2.0	4.5	μs
Driver Disable Time from High (MAX1480C Only)	tHZ	Figures 6 and 8, $C_L$ = 15pF, S2 closed		2.0	4.5	μs
Receiver Input to Output	t <sub>PLH</sub>	Figures 5 and 10, $R_{DIFF} = 54\Omega$ ,		2	3.0	
Propagation Delay	<b>t</b> PHL	$C_{L1} = C_{L2} = 100 pF$		2	3.0	μs
lt <sub>PLH</sub> - t <sub>PHL</sub> I Differential Receiver Skew	<sup>t</sup> SKD	Figures 5 and 10, $R_{DIFF} = 54\Omega$ , $C_{L1} = C_{L2} = 100 pF$		1200		ns
Maximum Data Rate	fMAX	tPLH, tPHL < 50% of data period	0.25			Mbps
Time to Shutdown	<sup>t</sup> SHDN			100		μs
Shutdown to Driver Output High	tzh(SHDN)	Figures 6 and 9, C <sub>L</sub> = 100pF, S2 closed		35	100	μs
Shutdown to Driver Output Low	tzl(SHDN)	Figures 6 and 9, $C_L$ = 100pF, S1 closed		35	100	μs

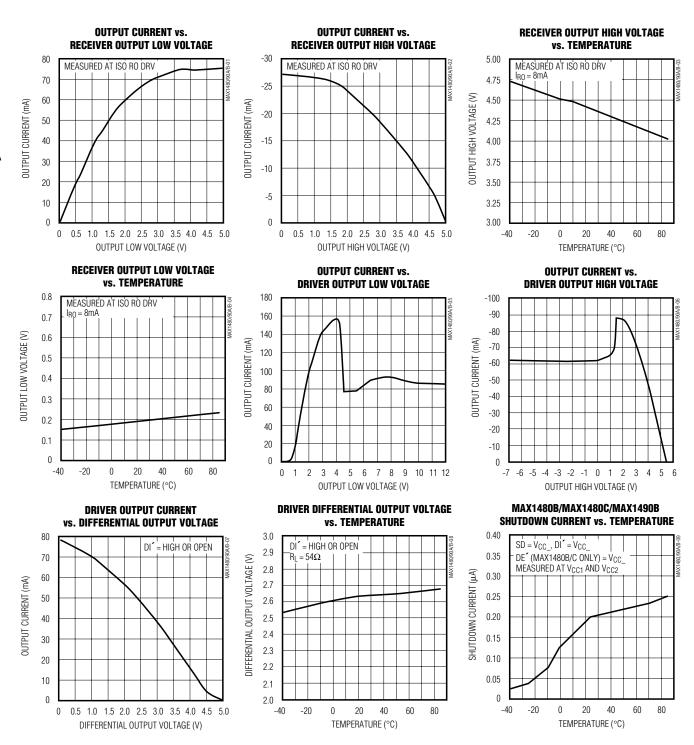
Note 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to logicside ground (GND\_), unless otherwise specified.

Note 2: For DE<sup>r</sup> and DI<sup>r</sup> pin descriptions, see *Detailed Block Diagram and Typical Application Circuit* (Figure 1 for MAX1480A/ MAX1480B/MAX1480C, Figure 2 for MAX1490A/MAX1490B).

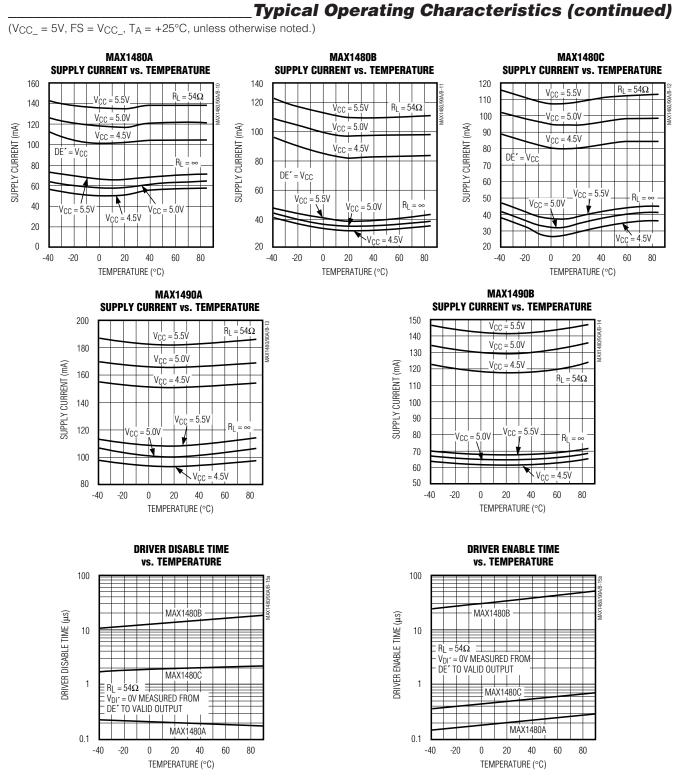
Note 3: Shutdown supply current is the current at V<sub>CC1</sub> and V<sub>CC2</sub> when shutdown is enabled.

**Note 4:** Applies to peak current (see *Typical Operating Characteristics*). Although the MAX1480A/B/C and MAX1490A/B provide electrical isolation between logic ground and signal paths, they do not provide isolation between external shields and the signal paths (see *Isolated Common Connection* section).

(V<sub>CC</sub> = 5V, FS = V<sub>CC</sub>,  $T_A$  = +25°C, unless otherwise noted.)



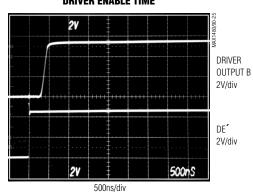
# **Typical Operating Characteristics**



#### **Typical Operating Characteristics (continued)** $(V_{CC_} = 5V, FS = V_{CC_}, V_{DI}' = 0V, DE' toggled 0V to 5V at 5kHz, T_A = +25°C, unless otherwise noted.)$ **MAX1480A MAX1480A DRIVER DISABLE TIME DRIVER ENABLE TIME** 21 21 DRIVER DRIVER OUTPUT B OUTPUT B 2V/div 2V/div DF' DE 2V/div 2V/div 200nS 200nS 21 21 200ns/div 200ns/div **MAX1480B MAX1480B DRIVER DISABLE TIME DRIVER ENABLE TIME** 2 2 DRIVER DRIVER OUTPUT B OUTPUT B 2V/div 2V/div

DRIVER ENABLE TIME



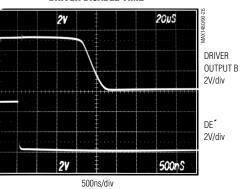




5µs/div

505

21

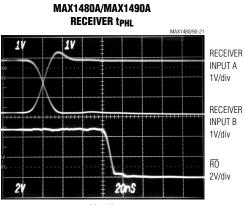


DE

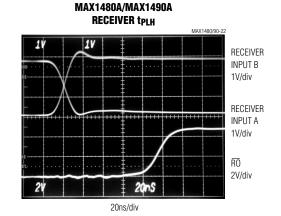
2V/div

### **Typical Operating Characteristics (continued)**

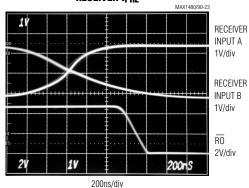
(V<sub>CC</sub> = 5V, FS = V<sub>CC</sub>, DE<sup> $\prime$ </sup> = V<sub>CC</sub>, V<sub>DI</sub><sup> $\prime$ </sup> = 0V to 5V at 1.25MHz, T<sub>A</sub> = +25°C, unless otherwise noted.)



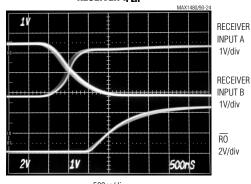
20ns/div



MAX1480B/MAX1480C/MAX1490B RECEIVER t<sub>Phl</sub>

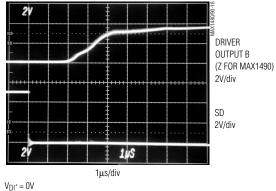


MAX1480B/MAX1480C/MAX1490B RECEIVER tplh



500ns/div

**POWER-UP DELAY TO DRIVER OUTPUTS VALID** 



V<sub>SD</sub> = 5V TO 0V AT 1kHz

### Pin Description

PI	N									
MAX1480A/B/C	MAX1490A/B	NAME	FUNCTION							
PINS ON THE	PINS ON THE NON-ISOLATED SIDE									
1, 2, 8, 10	1, 2, 8, 10	VCC1-VCC4	Logic-Side (nonisolated side) +5V Supply Voltages							
3, 4	3, 4	D1, D2	Internal Connections. Leave these pins unconnected.							
5	5	GND1	Logic-Side Ground. Connect to GND2 (pin 12).							
6	6	FS	Frequency Select Input. If FS = $V_{CC}$ or is open, switch frequency is high; if FS = GND, switch frequency is low. For optimal performance and minimal supply current, connect FS to $V_{CC}$ or leave unconnected.							
7	7	SD	Shutdown Input. Ground for normal operation. When high, the power oscillator is disabled.							
9	9	DI	Driver Input. With DE <sup>´</sup> high (MAX1480A/B/C only), a low on DI <sup>´</sup> forces output A low and output B high. Similarly, a high on DI <sup>´</sup> forces output A high and output B low. Drives internal LED cathode through a resistor (Table 1 of Figure 1 for MAX1480A/B/C, Table 2 of Figure 2 for MAX1490A/B).							
11	_	DE	Driver-Enable Input. The driver outputs, A and B, are enabled by bringing DE' high. The driver outputs are high impedance when DE' is low. If the driver outputs are enabled, the device functions as a line driver. While the driver outputs are high impedance, the device functions as a line receiver. Drives internal LED cathode through a resistor (Table 1 of Figure 1).							
_	11	RO	Receiver Output. If A > B by 200mV, RO will be high; if A < B by 200mV, RO will be low. Open collector; must have pullup to V <sub>CC</sub> (Table 2 of Figure 2).							
12	12	GND2	Logic-Side Ground. Connect to GND1 (pin 5).							
13	_	RO	Receiver Output. If A > B by 200mV, RO will be low; if A < B by 200mV, $\overline{RO}$ will be high. Open collector; must have pullup to V <sub>CC</sub> (Table 1 of Figure 1).							
14		VCC5	Logic-Side (non-isolated side) +5V Supply Voltage							
PINS ON THE	ISOLATED RS-4	85/RS-422 SIDE								
15	13	ISO RO LED	Isolated Receiver Output LED. Internal LED anode in MAX1480A/B/C and LED cathode in MAX1490A/B. Connect to ISO RO DRV through a resistor (Table 1 of Figure 1 for MAX1480A/B/C; Table 2 of Figure 2 for MAX1490A/B).							
16		ISO COM2	Isolated Common. Connect to ISO COM1 (pin 20).							
17	_	ISO DE DRV	Isolated Driver-Enable Drive. The driver outputs, A and B, are enabled by bring- ing DE <sup>´</sup> high. The driver outputs are high impedance when DE <sup>´</sup> is low. If the driv- er outputs are enabled, the device functions as a line driver. While the driver outputs are high impedance, the device functions as a line receiver. Open- collector output; must have pullup to ISO V <sub>CC</sub> and be connected to ISO DE IN for normal operation (Table 1 of Figure 1).							
18	14	ISO V <sub>CC2</sub>	Isolated Supply Voltage. Connect to ISO $V_{CC1}$ (pin 26 for MAX1480A/B/C, or pin 22 for MAX1490A/B).							
19	15	ISO DI DRV	Isolated Driver-Input Drive. With DE´ high (MAX1480A/B/C only), a low on DI´ forces output A low and output B high. Similarly, a high on DI´ forces output A high and output B low. Connect to ISO DI IN (on the MAX1480A/B/C only) for normal operation. Open-collector output; connect a pullup resistor to ISO V <sub>CC</sub> _ (Table 1 of Figure 1 for MAX1480A/B/C; Table 2 of Figure 2 for MAX1490A/B).							
20	16	ISO COM1	Isolated Common. For MAX1480A/B/C, connect to ISO COM2 (pin 16) (Figures 1 and 2).							





### Pin Description (continued)

PI	N								
MAX1480A/B/C	MAX1490A/B	NAME	FUNCTION						
PINS ON THE IS	PINS ON THE ISOLATED RS-485/RS-422 SIDE (continued)								
—	17	Y	Noninverting Driver Output						
—	18	Z	Inverting Driver Output						
—	19	В	Inverting Receiver Input						
—	20	A	Noninverting Receiver Input						
21		ISO DE IN	Isolated Driver-Enable Input. Connect to ISO DE DRV for normal operation.						
22		ISO DI IN	Isolated Driver Input. Connect to ISO DI DRV for normal operation.						
23		A	Noninverting Driver Output and Noninverting Receiver Input						
24	21	ISO RO DRV	Isolated Receiver-Output Drive. Connect to ISO RO LED through a resistor (Table 1 of Figure 1 for MAX1480A/B/C, Table 2 of Figure 2 for MAX1490A/B).						
25		В	Inverting Driver Output and Inverting Receiver Input						
26	22	ISO VCC1	Isolated Supply Voltage Source						
27, 28	23, 24	AC2, AC1	Internal Connections. Leave these pins unconnected.						

**Note:** For DE<sup>´</sup> and DI<sup>´</sup> pin descriptions, see *Detailed Block Diagram and Typical Application Circuit* (Figure 1 for MAX1480A/B/C, Figure 2 for MAX1490A/B).

### **Detailed Description**

The MAX1480A/MAX1480B/MAX1480C/MAX1490A/ MAX1490B are complete, electrically isolated, RS-485/ RS-422 data-communications interface solutions. Transceivers, optocouplers, a power driver, and a transformer in one standard 28-pin DIP package (24pin for the MAX1490A/B) provide a complete interface. Signals and power are internally transported across the isolation barrier (Figures 1, 2). Power is transferred from the logic side (nonisolated side) to the isolated side of the barrier through a center-tapped transformer. Signals cross the barrier through high-speed optocouplers. A single +5V supply on the logic side powers both sides of the interface. The MAX1480A/B/C offer half-duplex communications while the MAX1490A/B feature full-duplex communication. The functional input/output relationships are shown in Tables 3-6.

The MAX1480B/MAX1480C/MAX1490B feature reducedslew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free transmission at data rates up to 250kbps. The MAX1480A/MAX1490A driver slew rate is not limited, allowing transmission rates up to 2.5Mbps.

The MAX1480B/MAX1480C/MAX1490B shutdown feature reduces supply current to as low as  $0.2\mu$ A by using the SD pin (see *Low-Power Shutdown Mode* section).

Use the FS pin to select between high and low switching frequencies for the isolated power driver. The driver switches at the lower frequency 535kHz when FS is low, and at the higher frequency 725kHz when FS is high. The FS pin has a weak internal pull-up that switches the device to the high-frequency mode when FS is left unconnected. With FS high or open, no-load supply current is reduced by approximately 4mA, and by up to 8mA when fully loaded. For optimal performance and minimal supply current, connect FS to V<sub>CC</sub> or leave unconnected.

Drivers are short-circuit current limited and are protected against excessive power dissipation by thermal shutdown circuitry that puts the driver outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high RO (logic-low RO) output if the input is open circuit.

On the MAX1480A/B/C, the driver outputs are enabled by bringing DE<sup>+</sup> high. Driver-enable times are typically 0.2µs for the MAX1480A, 35µs for the MAX1480B, and 0.5µs for the MAX1480C. Allow time for the devices to be enabled before sending data (see the Driver Enable Time vs. Temperature graph in the *Typical Operating Characteristics*). When enabled, driver outputs function as line drivers. Driver outputs are high impedance when DE<sup>+</sup> is low. While outputs are high impedance, they function as line receivers.



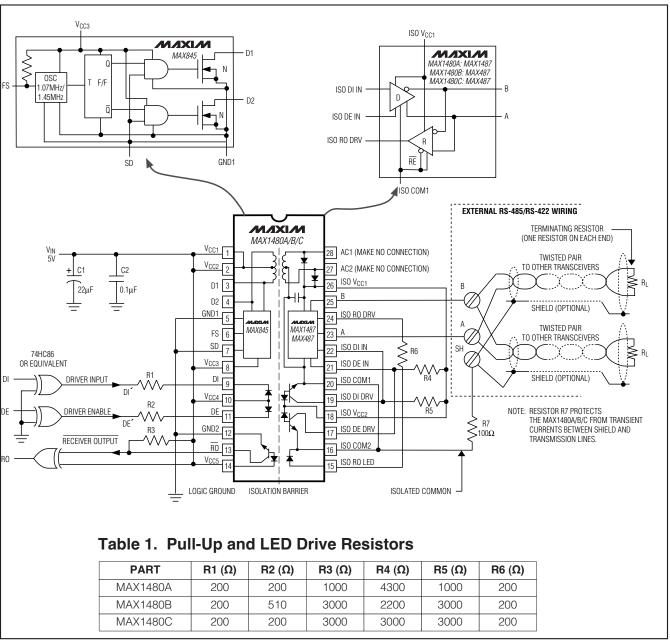


Figure 1. MAX1480A/MAX1480B/MAX1480C Detailed Block Diagram and Typical Application Circuit

The MAX1480A/MAX1480B/MAX1480C/MAX1490A/ MAX1490B typically withstand 1600V<sub>RMS</sub> (1 minute) or 2000V<sub>RMS</sub> (1 second). The logic inputs can be driven from TTL/CMOS-logic with a series resistor, and the received data output can directly drive TTL or CMOS-logic families with only resistive pullup.

#### Low-Power Shutdown Mode

The SD pin shuts down the oscillator on the internal power driver. With the primary side in shutdown, no power is transferred across the isolation barrier. The DI and DE optocouplers, however, still consume current if the drive signals on the nonisolated side are low. Therefore, leave DI' and DE' high or floating when in shutdown mode.



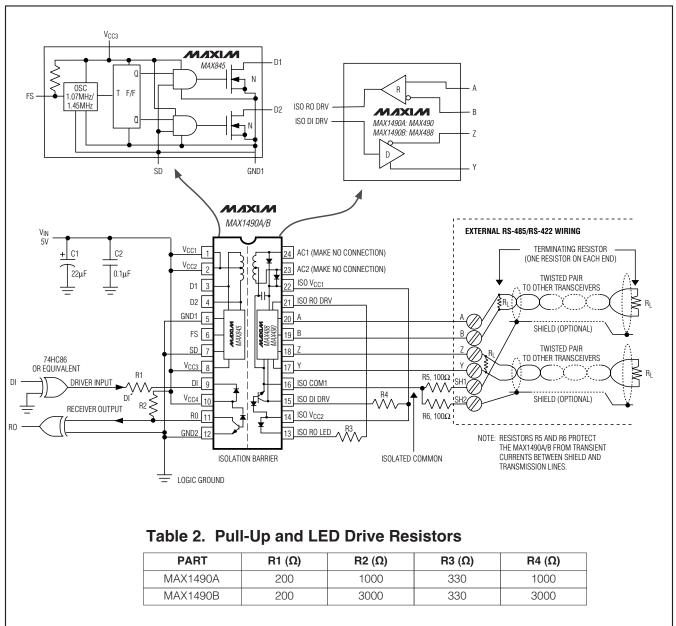


Figure 2. MAX1490A/MAX1490B Detailed Block Diagram and Typical Application Circuit

Under these conditions, the MAX1480B/MAX1480C/ MAX1490B supply current is reduced to as low as 0.2µA.

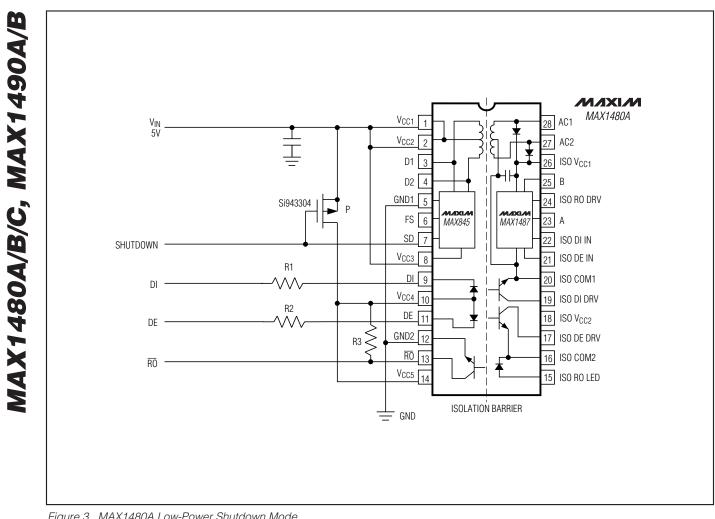
The high-speed optocouplers on the MAX1480A/ MAX1480C/MAX1490A consume an additional 10mA through V<sub>CC5</sub> (V<sub>CC4</sub> for the MAX1490A). Therefore, to completely shut down these devices, use an external Pchannel MOSFET as shown in Figure 3. In normal opera-

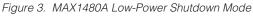
tion, SD is low, turning the MOSFET on and thereby providing power to all the V<sub>CC</sub> pins. When SD is pulled high, the power oscillator is disabled and the switch is turned off, disconnecting power from the DI and DE optocouplers. In normal operating mode, the switch carries only the optocoupler currents, so an on-resistance of several ohms will not significantly degrade efficiency.



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MAX1480A/B/C, MAX1490A/B





### **Test Circuits**

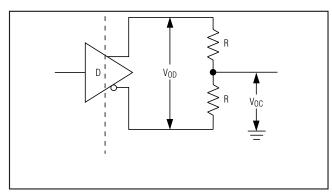
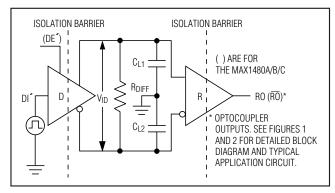


Figure 4. Driver DC Test Load







### Test Circuits (continued)

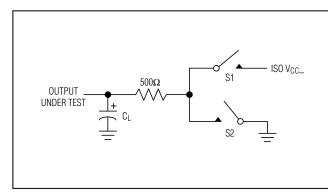


Figure 6. Driver Timing Test Load

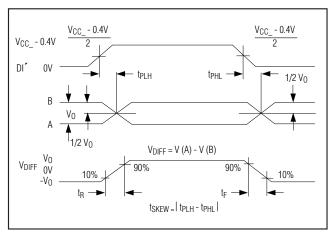


Figure 7. Driver Propagation Delays and Transition Times

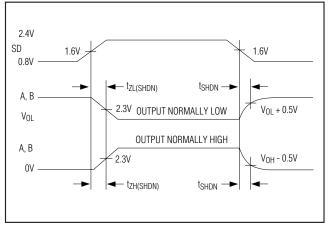


Figure 9. Times to/from Shutdown

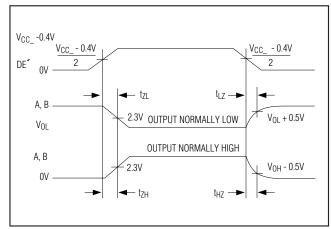
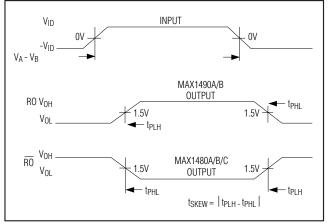


Figure 8. Driver Enable and Disable Times





### Switching Waveforms

#### MAX1480B/MAX1480C/MAX1490B: Reduced EMI and Reflections

The MAX1480B/MAX1480C/MAX1490B are slew-ratelimited, minimizing EMI and reducing reflections caused by improperly terminated cables. Figure 11 shows both the driver output waveform of a MAX1480A/MAX1490A transmitting a 150kHz signal and the Fourier analysis of that waveform. High-frequency harmonics with large amplitudes are evident. Figure 12 shows the same information for the slew-ratelimited MAX1480B/MAX1480C/MAX1490B transmitting the same signal. The high-frequency harmonics have much lower amplitudes, and therefore the potential for EMI is significantly reduced.

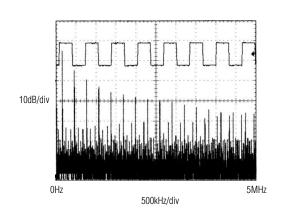


Figure 11. Driver Output Waveform and FFT Plot of MAX1480A/MAX1490A Transmitting a 150kHz Signal

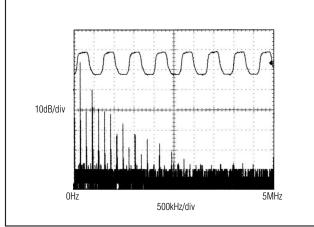


Figure 12. Driver Output Waveform and FFT Plot of MAX1480B/MAX1480C/MAX1490B Transmitting a 150kHz Signal

#### **Function Tables**

#### Half-Duplex Devices (MAX1480A/MAX1480B/MAX1480C)

#### Table 3. Transmitting

INPUTS*		OUTPUTS	
DE	DÍ	В	Α
1	1	0	1
1	0	1	0
0	Х	High-Z	High-Z

X = Don't care

High-Z = High impedance

#### Table 4. Receiving

INPUTS*		OUTPUT
DE	V <sub>A</sub> - V <sub>B</sub>	(RO)
0	≥ +0.2V	0
0	≤ -0.2V	1
0	Open	0

#### Full-Duplex Devices (MAX1490A/MAX1490B)

#### Table 5. Transmitting

INPUT*	OUTPUTS	
(DI´)	Z	Y
1	0	1
0	1	0

\* For DE<sup>\*</sup> and DI<sup>\*</sup> pin descriptions, see *Detailed Block Diagram and Typical Application Circuit* (Figure 1 for MAX1480A/B/C, Figure 2 for MAX1490A/B).

#### Table 6. Receiving

INPUT (VA - VB)	OUTPUT (RO)
≥ +0.2V	1
≤ -0.2V	0
Open	1

MAX1480A/B/C, MAX1490A/B

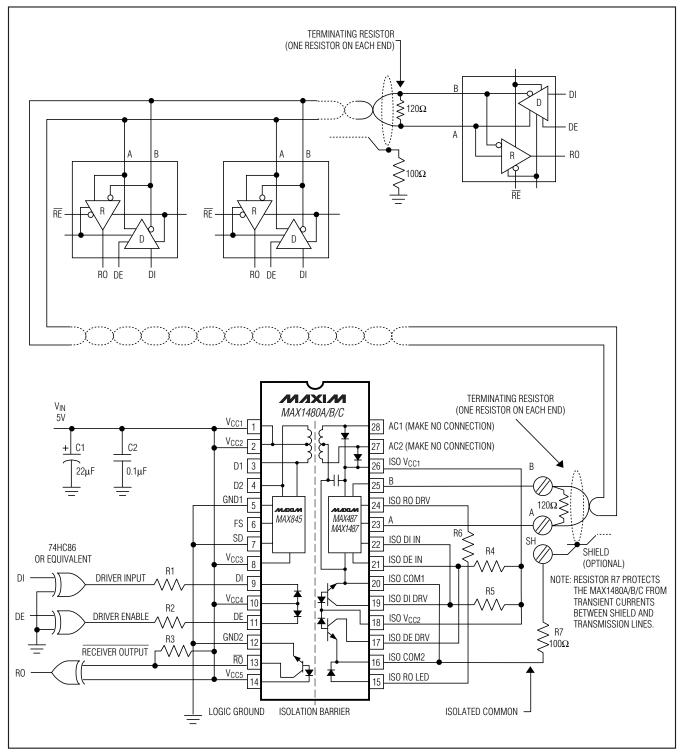


Figure 13. Typical Half-Duplex RS-485/RS-422 Network

MAX1480A/B/C, MAX1490A/B

#### **Driver Output Protection**

There are two mechanisms to prevent excessive output current and power dissipation caused by faults or by bus contention. A foldback current limit on the output stage provides immediate protection against short circuits over the entire common-mode range (see the *Typical Operating Characteristics*). In addition, a thermal shutdown circuit forces the driver outputs into a high-impedance state if the die temperature rises excessively.

#### **Propagation Delay Skew**

Typical propagation delays are shown in the *Typical Operating Characteristics* using the test circuit of Figure 5. Propagation delay skew is simply the difference between the low-to-high and high-to-low propagation delay. Small driver/receiver skew times help reduce EMI and reflections by maintaining balanced differential signals.

The receiver skew time,  $|t_{PLH} - t_{PHL}|$ , is typically under 100ns for the MAX1480A/MAX1490A and under 1µs for the MAX1480B/MAX1480C/MAX1490B.

The driver skew time is typically 25ns for the MAX1480A/MAX1490A and 100ns for the MAX1480B/ MAX1480C/MAX1490B.

#### **Applications Information**

DI and DE are intended to be driven through a series current-limiting resistor. Directly grounding these pins destroys the device.

The MAX1480A/MAX1480B/MAX1480C are designed for bidirectional data communications on multipoint bus-transmission lines. The MAX1490A/MAX1490B are designed for full-duplex bidirectional communications that are primarily point-to-point. Figures 13 and 14 show half-duplex and full-duplex typical network application circuits, respectively. To minimize reflections, terminate the line at both ends with its characteristic impedance, and keep stub lengths off the main line as short as possible. The slew-rate-limited MAX1480B/ MAX1480C/MAX1490B are more tolerant of imperfect termination and stubs off the main line.

#### **Layout Considerations**

The MAX1480A/MAX1480B/MAX1480C/MAX1490A/ MAX1490B pinouts enable optimal PC board layout by minimizing interconnect lengths and crossovers.

 For maximum isolation, the "isolation barrier" should not be breached except by the MAX1480A/ MAX1480B/MAX1480C/MAX1490A/MAX1490B.

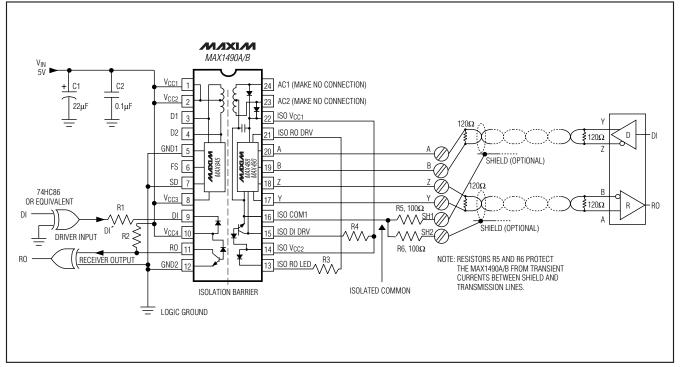


Figure 14. Typical Full-Duplex RS-485/RS-422 Network

Connections and components from one side should not be located near those of the other side.

- A shield trace connected to the ground on each side of the barrier can help intercept capacitive currents that might otherwise couple into the signal path. In a double-sided or multilayer board, these shield traces should be present on all conductor layers.
- Try to maximize the width of the isolation barrier wherever possible; a clear space of at least 0.25 inches between ground and isolated common is suggested.

#### **Pullup and LED Drive Resistors**

The MAX1480A/MAX1480B/MAX1480C/MAX1490A/ MAX1490B are specified and characterized using the resistor values shown in Table 1 of Figure 1 and Table 2 of Figure 2. Altering the recommended values can degrade performance. The DI and DE (MAX1480A/B/C only) inputs are the cathodes of LEDs whose anodes are connected to the supply. These points are best driven by a CMOS-logic gate with a series resistor to limit the current. The resistor values shown in Tables 1 and 2 are recommended when the 74HC86 gate or equivalent is used. These values may need to be adjusted if a driving gate with dissimilar series resistance is used.

All pull-up resistors are based on optocoupler specifications in order to optimize the devices' data-transfer rates.

#### **Isolated Common Connection**

The isolated common may be completely floating with respect to the logic ground and the effective network ground. The receiver input resistors will cause the isolated common voltage to go to the mean voltage of the receiver inputs. If using shielded cable, connect the isolated common to the shield through a 100 $\Omega$  resistor. In the case of the MAX1490, each shield should have its own 100 $\Omega$  resistor (Figures 1, 2, 13, and 14).

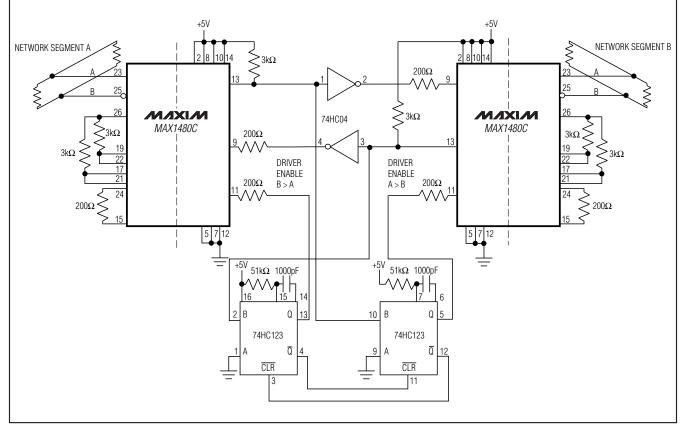


Figure 15. Doubly Isolated RS-485 Repeater

MAX1480A/B/C, MAX1490A/B

#### **Doubly Isolated RS-485 Repeater**

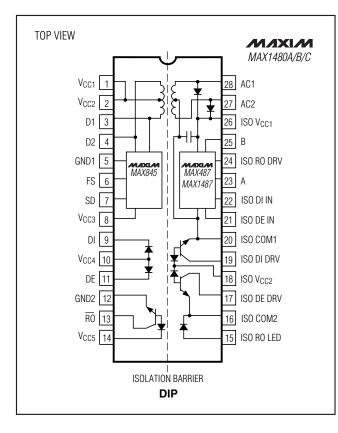
The RS-422/RS-485 standard is specified for cable lengths up to 4000 feet. When approaching or exceeding the specified maximum cable length, a groundpotential difference of several tens of volts can easily develop. This difference can be either DC, AC, at power-line frequency, or any imaginable noise or impulse waveform. It is typically very low impedance so that if a connection between the two grounds is attempted, very large currents may flow. These currents are by their nature unstable and unpredictable. In addition, they may cause noise to be injected into sensitive instrumentation and, in severe cases, might actually cause physical damage to such equipment.

Figure 15 shows a half-duplex (two-wire), bidirectional, party-line repeater system that prevents interference and/or damage from ground-potential differences. Two MAX1480A/MAX1480B/MAX1480C isolated RS-485 transceivers are used to isolate each of the network segments from the electrical environment of the repeater. The MAX1480A/MAX1480B/MAX1480B/MAX1480C also regenerate bus signals that may have been degraded by line attenuation or dispersion.

In the idle state, both transmitters are disabled, while all receivers in the system are enabled. If any device on the system has information for any other device, it starts sending its data onto the bus. Each data transmission on the bus retriggers the one-shot, keeping the sending transmitter enabled until there are no more transmissions. All receivers receive all data; if this is undesirable, the protocol must allow for an address field so receivers can ignore data not directed to them.

Each node must refrain from transmitting when data already exists on the bus, and must resend data that is corrupted by the collisions that inevitably occur with a party-line system. With the repeater of Figure 15, there might be transmitters up to 8000 feet apart. That represents more than  $8\mu s$  (assuming 1ns/foot of delay) in which two nodes could be transmitting simultaneously.

The circuit in Figure 15 can be used either directly as shown, with the slew-rate-limited MAX1480B/MAX1480C, for data transfer rates up to 250kbps, or with the MAX1480A for data rates up to 2.5Mbps (see Table 1 for pullup and LED resistor values when using the MAX1480A or MAX1480B). If dual-port isolation is not needed, one of the MAX1480C devices can be replaced by a MAX487 for 250kbps applications.



### Pin Configurations (continued)

### Ordering Information (continued)

PART <sup>†</sup>	TEMP RANGE	PIN-PACKAGE
MAX1480BCPI	0°C to +70°C	28 Wide Plastic DIP
MAX1480BEPI	-40°C to +85°C	28 Wide Plastic DIP
MAX1480CCPI	0°C to +70°C	28 Wide Plastic DIP
MAX1480CEPI	-40°C to +85°C	28 Wide Plastic DIP
MAX1490ACPG	0°C to +70°C	24 Wide Plastic DIP
MAX1490AEPG	-40°C to +85°C	24 Wide Plastic DIP
MAX1490BCPG	0°C to +70°C	24 Wide Plastic DIP
MAX1490BEPG	-40°C to +85°C	24 Wide Plastic DIP

<sup>†</sup>Data rate for "A" parts is up to 2500kbps. Data rate for "B" and "C" parts is up to 250kbps.

### Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 PDIP	P28M-1	<u>21-0044</u>

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