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ANALYTIC DESIGN OF CYCLIC LOW ENERGY ADC WITH SUB-OPTIMAL ESTIMATES CALCULATION

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Abstract – Principles of complex software and hardware design of the sub-optimal low-energy cyclic ADC (CADC) are presented. The extended conversion algorithm for estimates computing is discussed. Upper boundaries of CADC resolution, rate of conversion and the ways they can be achieved are analyzed. Properties and general advantage of sub-optimal CADC are discussed and investigated in simulation experiments.

Keywords: low-energy ADC, sub-optimal adaptive conversion, upper boundary of resolution

1. INTRODUCTION

The objective of micro ADC design is an obtaining the highest resolution and speed of conversion under minimal complexity, size, power consumption and cost of device. these requirements are best satisfied by the cyclic (multi-pass) ADC [1-3] which form the input signal estimates cyclically, using minimal number of repeating operations realized by a minimal number of elements. The structure of CADC is presented in Fig. 1. They work as follows:

Each sample $V^{(m)}$ (m=1,2,…) formed by the sample-and-hold block (S&H) is stored at the input of subtracting block (S) during the time T necessary for completing n cycles of conversion. In each cycle $k = 1,...,n$, block (R) registers and stores following iterations if estimates $\hat{V}_k$ of the sample V. Using digit-to-analogue converter (DAC), analogue equivalent $\hat{V}_{k-1,t}$ of this estimate, with the one-step delay, enters the second input of the summating block S.

The residual signal e_t is routed, through the amplifier A, to the input of auxiliary internal low-bit ADC ($\mathrm{ADC_{In}}$), and the result of internal conversion $\tilde{y}_{k+1} = C\, e_{k+1} + \xi_{k+1}$, ($\xi_k$ is the quantization noise) enters the block R. Using previous estimate $\hat{V}_k$ and current observation $\tilde{y}_{k+1}$, block R forms new estimate $\hat{V}_{k+1}$, and the cycle repeats.

In general case, work of each CADC can be described by the relationship:

$$\hat{V}_k = \hat{V}_{k-1} + L_k \tilde{y}_k \quad (k=1,...,n) \tag{1}$$

where coefficients L_k refer to the chosen method of estimates forming. Properties of algorithm (1) depend on the employed engineering solutions, choice of parameters of the analog part, on the signals they are applied etc. On these reasons, real performance of CADC can be much lower than that potentially achievable using the same elements.

One can see that recurrent formula (1) has the form identical to the general form of recurrent algorithms, widely and efficiently used for estimation of signal parameters in the presence of noises. Methods of these algorithms optimization are well known [4,5] and, being modified and completed by additional conditions, are used in the present work for the concurrent complex optimization of CADC software and hardware.

The result is a group of relationships determining the construction of analog part and software of the converters, which may operate with a rate and resolution close to theoretically achievable. However, direct application of these methods to CADC optimization meets serious difficulties caused by twice-nonlinearity of CADC - its step-wise form of characteristic and always-limited input range.

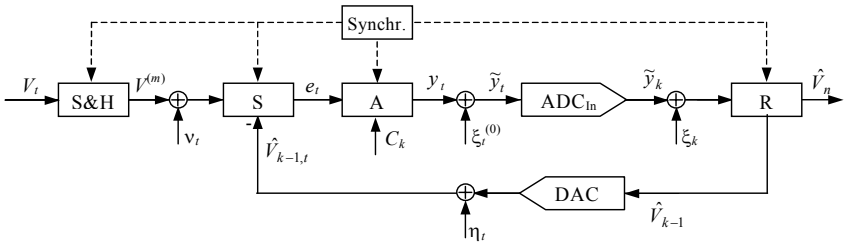

Fig 1: General structure of CADC.

2. COMPLEX OPTIMIZATION PROBLEM

To improve the performance of CADC, we propose:

- to replace the registering block R by microprocessor or special computing block;
- to replace the estimates $\hat{V}_k$ forming or registering by their *calculation* using properly modified extended algorithms [6-10] for joint optimal adaptive observation and estimation of input signal. These algorithms have a number of important advantages over conventional ones;
- to use the calculated optimal prognoses of the input signal values for compensation and forming the residual signal $e_k = V - \hat{V}_{k-1,} + v_k$ (further, the discrete time analysis is performed).

Following particularities of CADC's work should to be taken also into account during their optimization and design:

1. The limited input range of ADC_{In} - the source of possible CADC saturation and rough errors of conversion.
2. Step-wise transfer function of low-bit ADC_{In},- the source of powerful quantization noise.
3. Dependence of coefficients L_k in (1) on the architecture of the converter, parameters of its analogue part , and the way of estimates forming.

It is assumed that amplitudes V of the converted samples are normally distributed with the mean V_0 and variance σ_0^2. Full noise ν_t at the output is a sum of the noise η_t in the feedback chain - DAC noise, possible external noise, and the noise of summer (ν_t is assumed to be white, zero mean gaussian noise with the variance σ_ν^2).

Denoting the saturation levels of ADC_{In} as $\pm D$, the gain of amplifier as C_k, one can write the static model of "S+A+ADC_{In}" unit as follows:

$$\tilde{y}_k = \begin{cases} C_k(y_k - \hat{V}_{k-1}) + \hat{\imath}_k, & \left| y_k - \hat{V}_{k-1} \right| \le D/C_k \\ D\,sign(y_k - \hat{V}_{k-1}) + \hat{\imath}_k, & \left| y_k - \hat{V}_{k-1} \right| \le D/C_k \end{cases}, \qquad (2)$$

Here $y_k = V + v_k$ is an unknown component if input signal, and $\hat{V}_{k-1,}$ - the calculated value of its prognosis to k-th cycle of conversion; $e_k = V - \hat{V}_{k-1,} + v_k$ is the residual error after compensation of input signal. Variance σ_ξ^2 of quantization noise is estimated by commonly used relationship $\sigma_\xi^2 = \Delta^2/12 = D^2 2^{-2N_{ADC}}/3$. The amplifier noise $\xi_t^{(0)}$, much less powerful then quantization noise, is omitted.

2.1. Problem of saturation

The limited input range of CADC is a source of possible saturation of the input signal that results in appearance of rough errors in estimates and practical lost of any information about distorted sample. To analyze and exclude saturation errors in converters, the statistical fitting condition [6,7] is used. It has the form of constraint on the probability of CADC saturation:

$$\Pr_k^{sat} = \Pr\left\{ C_k \mid e_k \mid \le D \,\middle|\, \tilde{y}_1^{k-1} \right\} < 1 - \mu \qquad (3)$$

This inequality defines the "permitted" values of "A+ADC_{In}" unit parameters, which guarantee the probability of ADC_{In} saturation will be less of small given μ. for each k=1,...,n. Value μ is chosen by designers according to requirements to the quality of conversion ($10^{-4} < \mu < 10^{-15}$).

Setting the parameters of analog part, for each k =1,2,... to the values to satisfying fitting condition (3), results in a saturation of CADC will be practically eliminated. This permits us to replace the nonlinear model (2) by the linear one: $\tilde{y}_k = C_k e_k + \xi_k$ and analyze the converter using conventional methods of linear theory of optimization and statistical synthesis [4,5].

2.2. Complex algorithm of conversion

Derivation of extended sub-optimal algorithm for concurrent computing the estimates $\hat{V}_k$ and amplifier A adjusting gives the following group of relationships [6-8]:

$$\hat{V}_k = \hat{V}_{k-1} + L_k \tilde{y}_k ; \qquad (4)$$

$$L_k = \frac{C_k P_k}{\sigma_\xi^2 + C_k^2 \sigma_\nu^2} \qquad (5)$$

$$P_k = \frac{\sigma_\xi^2 + C_k^2 \sigma_\nu^2}{\sigma_\xi^2 + C_k^2 (\sigma_\nu^2 + P_{k-1})} P_{k-1} \qquad (6)$$

$$C_k = \frac{D}{\alpha \sqrt{\sigma_\nu^2 + P_{k-1}}} \qquad (7)$$

where α satisfy the equation: $\Phi(\alpha) = (1-\mu)/2$ where $\Phi(\alpha)$ is known gaussian error function, and initial conditions are as follows: $\hat{V}_0 = V_0$; $P_0 = \sigma_0^2$.

For each k, algorithm (4)-(7) minimizes the mean square error (MSE) of estimates $P_k = E[(V - \hat{V}_{k-1})^2]$. Values P_k, in this case, determines the lower theoretically achievable boundary of the conversion errors. Simultaneously, the analog part being adjusted according to (2), (7) excludes its possible saturation, for each k, with a probability not less of μ. Practical conditions of this μ value maintaining during each sample conversion are discussed in Section 4.

Formulas (5)-(6) can be rewritten in the equivalent form:

$$L_k = \frac{Q}{(1+Q^2)} \frac{P_{k-1}}{\sigma_\xi \sqrt{\sigma_\nu^2 + P_{k-1}}} \qquad (8)$$

$$P_k = (1+Q^2)^{-1} \left(\frac{\sigma_\nu^2 + P_{k-1}}{(1+Q^2)\sigma_\nu^2 + P_{k-1}} \right)^{-1} P_{k-1} ; \qquad (9)$$

where

$$Q^2 = \frac{C_k^2 E(e_k^2)}{\sigma_\xi^2} = \left(\frac{D}{\alpha \sigma_\xi} \right)^2 = \frac{3}{\alpha^2} 2^{2N_{ADC}} \qquad (10)$$

is a decimal signal-to-noise ratio (SNR) at the output of ADC_{In} that is at the CADC analog part output.

Formula (9) determines the theoretically achievable lower boundary of MSE of sub-optimal conversion at each cycle, and generalizes the evaluations given in [9,10]. Under $\sigma_\nu^2 << P_0$, that is fulfilled for each converter, there always exists the initial interval $1 \le k < n^*$, where MSE P_k diminishes *exponentially* with a growth of k

$$P_k = P_{k-1}(1+Q^2)^{-1} = \sigma_0^2 (1+Q^2)^{-k} \qquad (11)$$

For $k > n^*$, values P_k diminish more slowly, as hyperbolic functions of conversion cycles number. Point n^* can be estimated by formula:

$$n^* \approx \frac{2}{\log(1+Q^2)} \log\left(\frac{\sigma_0}{\sigma_v}\right) \quad (12)$$

is a number of cycles needed for the achievement of conversion accuracy of the $\hat{V}_k = V \pm \alpha\sigma_v$ order. This means, value n^* determines, in the main order, a speed of each sample conversion and, as result, the band-pass of CADC $f_{\max} \sim (n^* \Delta t)^{-1}$, where Δt is a time duration of a single cycle of conversion.

2.3. Resolution of converters (ENOB)

Being fulfilled at each k=1,2,... , fitting condition (3) guarantees a validity of following inequalities:

$$\Pr(|V_0 - V| \le \alpha\sigma_0) \ge 1 - \mu \quad (13)$$

$$\Pr(|V - \hat{V}_k| \le \alpha\sqrt{P_k}) \ge 1 - \mu \quad (14)$$

Formula (13) permits us to determine the CADC input range as the interval $[-V_{\max}, V_{\max}] = [V_0 - \alpha\sigma_0, V_0 + \alpha\sigma_0]$ of practically always appearing values of the input signal. Probability of appearance of the signal outside of this interval is less than μ.

Formula (14) determines the interval error at each cycle of conversion (confidence interval) $[\hat{V}_k - \alpha\sqrt{P_k}, \hat{V}_k + \alpha\sqrt{P_k}]$. For each k=0,1,2,... the probability that each sample value V lays in one of corresponding intervals $[\hat{V}_k - \alpha\sqrt{P_k}, \hat{V}_k + \alpha\sqrt{P_k}]$ is always not less than $1-\mu$. This allows us to consider the CADC as a device with more and more accurate, at each next cycle of conversion, scale of the measurement of input signal value. A number of the levels the CADC may resolve after k cycles is

$$M_k = \frac{2V_{\max}}{2\alpha\sqrt{P_k}} = \frac{\sigma_0}{\sqrt{P_k}} \quad (15)$$

Number of bits necessary for presentation of each resolved level among this set is

$$N_k = \log_2 M_k = \frac{1}{2}\log_2\left(\frac{\sigma_0^2}{P_k}\right) \text{ [bit]} \quad (16)$$

This is a binary expression for resolution of the converted which determines simultaneously the length of meaning bits in the codes of estimates at CADC output and, and most naturally correspond to the frequently used term "efficient number of bits" (ENOB).

Substituting (7) and (9) into formula (16), one can obtain the recurrent equation for resolution of sub-optimal CADC:

$$N_k = N_{k-1} + \frac{1}{2}\log_2\left(1 + \frac{C_k^2 P_{k-1}}{\sigma_\xi^2 + C_k^2\sigma_v^2}\right) =$$

$$= N_{k-1} + \frac{1}{2}\log_2(1+Q^2) - \frac{1}{2}\log_2\left(1 + Q^2\frac{\sigma_v^2}{\sigma_v^2 + P_{k-1}}\right) \quad (17)$$

According to (11), at the initial interval $1 \le k < n^*$ ENOB (resolution of CADC) N_k grows linearly with a number of iterations:

$$N_k = \frac{k}{2}\log_2(1+Q^2) \approx k(N_{ADC} - \log_2\alpha + 0.7925) \quad (18)$$

and for $k > n^*$ - logarithmically

$$N_k = \log\left(\frac{\sigma_0}{\sigma_v}\right) + \frac{1}{2}\log\left(1 + (k-n^*)Q^2\frac{\sigma_v^2}{\sigma_0^2}\right) \quad (19)$$

The rate of resolution N_k growth and diminution of MSE P_k is greater the greater are values of Q that is, according to (10), for greater N_{ADC} and lesser α. However, a tendency in CADC design is employment of low-bit ADC_{In} and shall N_{ADC}. Lesser α, in turn, causes greater risk of saturation. These dependencies should be taken into account in CADC design.

After n^* cycles, resolution of CADC reaches the value

$$N^* = \log_2\left(\frac{\sigma_0}{\sigma_v}\right) = \log_2\left(\frac{V_{\max}}{\alpha\sigma_v}\right) \quad (20)$$

which, together with the number n^*, may serve as evaluation of main order of expected CADC resolution and a rate of conversion.

3. INFORMATION PROPERTIES OF CONVERTERS

Definition of CADC resolution (16) and other useful results can be introduced using information theory approach to consideration of the work of converter [11].

3.1 Resolution and information capacity

Namely, according to known definition [12], information $I(V; \tilde{y}_1^k)$ about the samples V delivered by observations $\tilde{y}_1^k$ is equal to the value of removed uncertainty, i.e. difference between the prior $H(V)$ and posterior $H(V \mid \tilde{y}_1^k)$ entropy of the input signal samples:

$$I(V, \tilde{y}_1^k) = H(V) - H(V \mid \tilde{y}_1^k) \quad (21)$$

Taking into account that in gaussian case

$$p(V) = (2\pi\sigma_0^2)^{-\frac{1}{2}} \exp\left(-\frac{1}{2\sigma_0^2}(V - V_0)^2\right); \quad (22)$$

$$p(V \mid \tilde{y}_1^k) = (2\pi P_k)^{-\frac{1}{2}} \exp\left(-\frac{1}{2P_k}[V - \hat{V}_k(\tilde{y}_1^k)]^2\right) \quad (23)$$

one can easily calculate value (21):

$$I(V, \tilde{y}_1^k) = \frac{1}{2}\log_2\left(\frac{\sigma_V^2}{P_k}\right) = I[V, \hat{V}_k(\tilde{y}_1^k)] \text{ [bit]} \quad (24)$$

Comparison of (24) and (16) shows that determined by (16) resolution N_k is equal to information $I(V, \tilde{y}_1^k)$ in optimal estimates $\hat{V}_k(\tilde{y}_1^k)$ (or, that is the same, in observations $\tilde{y}_1^k$) about the input sample V. This value can be treated also as

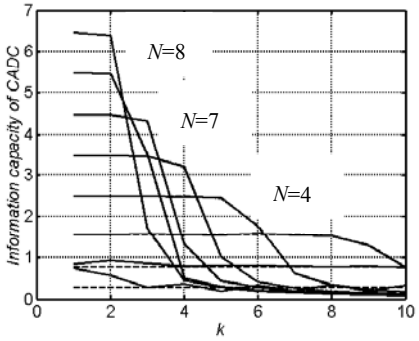

Fig. 2. Current information flow (capacity) of CADC as a function of k for different $\mathrm{ADC_{In}}$ (N_{ADC} =1 ÷ 8).

mean number of bits necessary for binary presentation of the values V with the accuracy $\pm\alpha\sqrt{P_k}$. This confirms once more an equivalence of the terms "resolution" and "ENOB" as the converter characteristics.

According to (24), additional information delivered by each processed observation $\widetilde{y}_k$, is equal to:

$$I(V;\widetilde{y}_k \mid \widetilde{y}_1^{k-1}) =$$

$$I(V,\widetilde{y}_1^{k}) - I(V,\widetilde{y}_1^{k-1}) = I[V,\hat{V}_k)] - I[V,\hat{V}_{k-1})] =$$

$$\frac{1}{2}\log_2\left(\frac{P_{k-1}}{P_k}\right) = N_k - N_{k-1}.. \qquad (25)$$

This value determines the current flow of information through CADC, or its capacity in gaussian case. It presents, simultaneously, the increment of CADC resolution (ENOB) in successive cycles of approximation.

If the gains C_k are increased according to (7), information flow through CADC reaches, for each k, maximum value:

$$R_k = \max I(V,\widetilde{y}_k \mid \widetilde{y}_1^{k-1}) =$$

$$= \frac{1}{2}\log_2(1+Q^2) - \frac{1}{2}\log_2\left(1+Q^2\frac{\sigma_v^2}{\sigma_v^2+P_{k-1}}\right) \qquad (26)$$

Dependencies R_k on k for CADC with different $\mathrm{ADC_{In}}$ are presented in Fig. 2.

3.1. Analysis of results

1. First term in (26) describes the information capacity of $\mathrm{ADC_{In}}$, which plays in CADC a role of data-transmission channel from the analog to digital part:

$$R_0 = \frac{1}{2}\log_2(1+Q^2) =$$

$$\frac{1}{2}\log_2\left(1+\frac{C_k^2E(e_k^2)}{\sigma_\xi^2}\right) = \frac{1}{2}\log_2\left(1+\frac{W_s}{\sigma_\xi^2}\right). \qquad (27)$$

Relationship (27) presents known Shannon's formula [12] for information capacity of stationary channels with additive white gaussian noise. Value $W_s = C_k^2E(e_k)^2$ is a power of useful signal at the $\mathrm{ADC_{In}}$ output.

In the ideal case of no input and feedback noise ($\sigma_v^2 = 0$; $P_k/\sigma_v^2 = \infty$), information capacity of CADC R_k takes maximal, constant value equal to information capacity of $\mathrm{ADC_{In}}$: $R_k = R_0$ at each cycle of conversion.

2. According to estimation and filtering theory [4,5], in gaussian case, the residuals $e_k = V - \hat{V}_{k-1} + v_k$ formed using optimal estimates (4), are zero-mean, mutually independent random values. This and dependence $\widetilde{y}_k = C_k e_k + \xi_k$ (valid due to the fitting condition) observations $\widetilde{y}_1^k = \{\widetilde{y}_1,...,\widetilde{y}_k\}$ at the $\mathrm{ADC_{In}}$ output are white gaussian noise with the monotonically diminishing variance $E(\widetilde{y}_k^2) = \sigma_\xi^2 + C_k^2(\sigma_v^2 + P_{k-1})$, and information in the observed realization $\widetilde{y}_1^k$ has the value:

$$H(\widetilde{y}_1^k) = \sum_{i=1}^{k}\log_2\{2\pi e[\sigma_\xi^2 + C_k^2(\sigma_v^2 + P_{k-1})]\} \qquad (28)$$

Setting C_k to maximal admissible values (7) makes the observations $\widetilde{y}_1^k$ the stationary white process with maximal achievable variance $E(\widetilde{y}_k^2) = \sigma_\xi^2(1+Q^2)$ (for the greater C_k a probability μ of CADC overloading takes unacceptably large values). As result, signal-to-noise ratio at the $\mathrm{ADC_{In}}$ output and entropy reach maximum value, and

$$H(\widetilde{y}_1^k) = \frac{k}{2}\log_2\{2\pi e\sigma_\xi^2(1+\mathrm{Q}^2)\} \qquad (29)$$

The conditional entropy $H(\widetilde{y}_1^k \mid y_1^k)$ has the value:

$$H(\widetilde{y}_1^k \mid y_1^k) = \frac{k}{2}\log_2\{2\pi e\sigma_\xi^2\} \qquad (30)$$

Using (29), (30), one can calculate the value $I(\widetilde{y}_k, y_k) = H(\widetilde{y}_k) - H(\widetilde{y}_k \mid y_k)$ which is equal to maximal information R_0 delivered to processor by each sample $\widetilde{y}_k$, that is equal to the capacity of $\mathrm{ADC_{In}}$.

This result is identical to the known claim of information theory: to transmit maximal information, signal should have the form of the stationary white gaussian noise [12]. In this case, a number of samples $\widetilde{y}_k$ necessary to deliver some quantity of information about V to the processor is minimal. That means, this information can be obtained in a minimal number of conversion cycles.

3. If CADC is fitted with input signal according to (3), then a probability of overloading and rough errors appearance is not greater of μ for each k=1,2,…, and conversion errors P_k reach minimal values. This and said above means that optimally fitted and controlled according to (7) unit "subtracting block + amplifier" realizes, in the analog way, the same functions as the optimal coding blocks in data-transmitting systems employing channels with Gaussian noise.

In this case, the input samples converted according to algorithm (4)-(7) under fulfilled condition (3) reach, for each k, minimal, MSE P_k and information flow equal to capacity of CADC under guaranteed probability of rough errors appearance not greater of μ .

3. PRACTICAL DESIGN AND APPLICATION

To apply the analytical results of previous sections to CADC design, nominal values of following parameters of the analog part should be determined or given:

- input range $[-V_{\max}, V_{\max}]$ of CADC;
- permissible probability of saturation μ ;
- resolution N_{ADC}, of the internal $\mathrm{ADC_{In}}$
- input range of D of the internal $\mathrm{ADC_{In}}$;
- variance σ_v^2 of the summary noise ν_k ;

The input range $[-V_{\max}, V_{\max}]$ of each CADC is determined by existing standard (there is assumed V_0 =0). According to fitting condition (3), saturation of converter will not exceed given μ , if maximal variance σ_0^2 of the input signal is not greater than $\sigma_0^2 = (V_{\max}/\alpha)^2$. This value should be taken as the nominal parameter of algorithm (4)-(7). Parameter D does not influence on MSE and can be chosen depending on convenience of amplifier realization and gains C_k setting.

In turn, parameter α is determined by the accepted level of saturation probability μ . Dependence $\mu = 1 - 2\Phi(\alpha)$ is very sensitive. Small enlargement of α cause fast μ diminution. For instance, setting α =3 ("three sigma" input range) gives $\mu = 0.0013$; for α =4, $\mu \sim 10^{-5}$; for α =5, $\mu \sim 10^{-7}$; for α =7, $\mu \sim 10^{-12}$, etc. Therefore, if one has doubts that the variance of real signal may exceed the value σ_0^2 , it is enough to diminish σ_0^2 for α^{-1} percents (i.e. to take α +1) to decrease a saturation probability till more than order. This will diminish, simultaneously, SNR_{out} Q^2 and a speed of conversion. However, due to logarithmic dependence on values Q, increment of n^* value (12) and narrowing of CADC band-pass will be not significant.

One should remember that according to (10) Q can be increased by application of $\mathrm{ADC_{In}}$ with greater N_{ADC}. Final choice of nominal value α and N_{ADC} requires a complex consideration of requirements to CADC. Nominal value of σ_v^2 noise is determined, to the large extent, by the noise of feedback DAC. Choice of DAC resolution is conditioned by needed final accuracy of CADC and possible additional requirements to the cost, stability, etc.

Being chosen and introduced into (4)-(7) nominal parameters may differ from real parameters of the input signal and analog part, as well as may depend on real distribution of signal values.

One can evaluate deviations of MSE P_k from nominal values (6), (9) due to the differences between the nominal σ_0^2 and real $\overline{\sigma}_0^2$ variances. Calculations show that, in this case, conditioned MSE of estimates $\overline{P}_k(V^{(m)}) = E[(\hat{V}_k - V^{(m)})^2 \mid V^{(m)}]$ has the same form for each sample $V^{(m)}$:

$$\overline{P}_k\,(V^{(m)}) = P_k + P_k^2 P_0^{-2}[\,(V^{(m)})^2 - \sigma_0^2] \qquad (31)$$

and averaged over all $V^{(m)}$ "real" MSE $\overline{P}_k\,(V^{(m)})$ is equal to:

$$\overline{P}_k\,(V^{(m)}) = P_k + P_k^2 P_0^{-2}[\,\overline{\sigma}_0^2 - \sigma_0^2] \qquad (32)$$

This means that the signals with variances $\overline{\sigma}_0^2 < \sigma_0^2$ will be converted initially with MSE always less than nominal. For greater k, "real" and nominal MSE differ quickly disappears as a value of $(1+Q^2)^{-2}$ order. Discrepancies between σ_v^2 and $\overline{\sigma}_v^2$ variances influence in similar way, but much weaker.

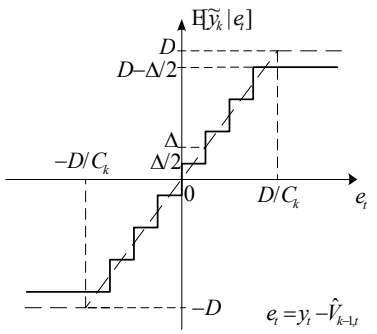

Fig. 3. Static input-output characteristic of analog unit "subtracting block -amplifier- internal converter"

Thus, accurate application of CADC to real signals conversion needs only to check the requirement: the input signal variance should be less than nominal value σ_0^2 .

Formula (31) is valid for each sample independently from the form of distribution of input signal values. This means it can be used for a numerical analysis of changes in MSE both in the case of non-gaussian and deterministic input signals including sin-waves.

3 RESULTS OF SIMULATION ANALYSIS

As it was shown in [9,10], mathematical modeling enables performance of fast and reliable analysis of CADC work and evaluating its performance depending on input signals, parameters of analog part and software, as well as on additional conditions and limitations. Important advantage of mathematical modeling is a possibility to obtain the exact solutions in domains where analytical investigation gives no results.

The modeling bench was built using real step-wise model of the CADC analog part as in Fig. 3. Data processing part is modeled by algorithm (4)-(7). The input signals was modeled as a sequence of random normally distributed samples $\{V^{(1)},...,V^{(M)}\}$, m=1,…,M , each of the length n enabling realization of k =1,...,n cycles of conversion. Empirical MSE (EMSE) $\hat{P}_k$ of estimates and resolution $\hat{N}_k$ were calculated according to formulas:

$$\hat{P}_k = \frac{1}{M}\sum_{m=1}^{M}\left[V^{(m)} - \hat{V}_k^{(m)}\right]^2; \quad \hat{N}_k = \frac{1}{2}\log_2\left(\frac{\sigma_0^2}{\hat{P}_k}\right) \qquad (33)$$

where $\hat{V}_k^{(m)}$ are estimates of the m-th sample; $P_0 = \sigma_0^2$ is the nominal prior value of MSE.

In the first series of experiments, the main attention was paid to analysis of influence of the differences between the parameters of real signals and analog elements of CADC, and their expected values used as the nominal parameters of algorithm (4)-(7) computing the estimates.

In Fig. 4, there is shown a dependence of MSE of conversion on the errors in analog gains $\overline{C}_k$ setting. The plot corresponds to $\mathrm{ADC_{In}}$ with N_{ADC}= 3. Very important for applications is a wide zone of insensitivity of the fastest MSE diminution to deviations of $\overline{C}_k$ from C_k .

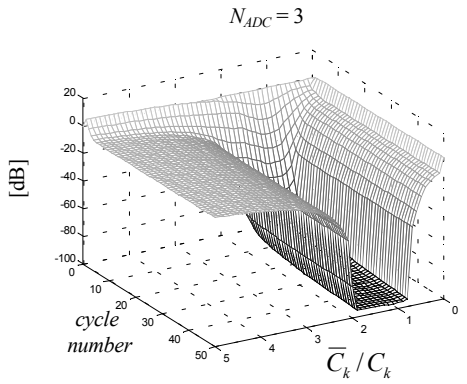

Fig. 4. Dependence of MSE of conversion on the errors in analog gains $\overline{C}_k$ setting (C_k is nominal gain value (7)).

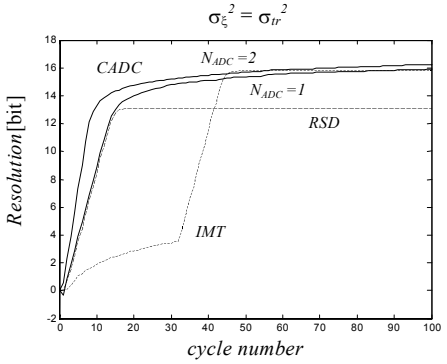

Fig. 2: Dependencies of CADC, RSD and IMT ADC resolution on the number of conversion cycles.

This zone is wider for CADC with one-two bits internal converters, and quickly narrows with a growth of N_{ADC}

Simulation analysis of MSE dependence on quantization noise power evaluation σ_ξ^2 has shown that performance of CADC with low-bit ADC_{In} reaches maximum, if nominal value σ_ξ^2 is taken about two times less than $\Delta^2/12$.

Resolution of low-bit CADC was compared with resolution of known RSD and IMT converters [2,3]. The results of simulations are shown in Fig. 5 for the case of σ_ξ^2 evaluation as $\sigma_\xi^2 = 0.45\ \Delta^2/12$. The plots show that CADC with 1-bit ADC_{In} (comparator) reaches the resolution of the same order as two-comparator converter RSD.

4 CONCLUSIONS

The results of investigation show a possibility to increase significantly the efficiency of CADC by transition to codes computing using model-based signal processing algorithms. The presented approach enables complex optimization and design of CADC software and hardware that ensures close to theoretically achievable, highest increment of resolution at each cycle of conversion.

The performed simulations confirm the numerical and qualitative concordance of theoretical and measured results. Moreover, developed simulation tools enable efficient, fast and exact analysis of effects defying to theoretical analysis.

Most efficient way of proposed CADC implementation seems to be their direct integration with microprocessor or computer, and direct calculation of estimates using their computing resources.

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