What's New in the Latest QorIQ 28nm 64-bit Processors including T1, T2, T4 Families?

EUF-NET-T1279

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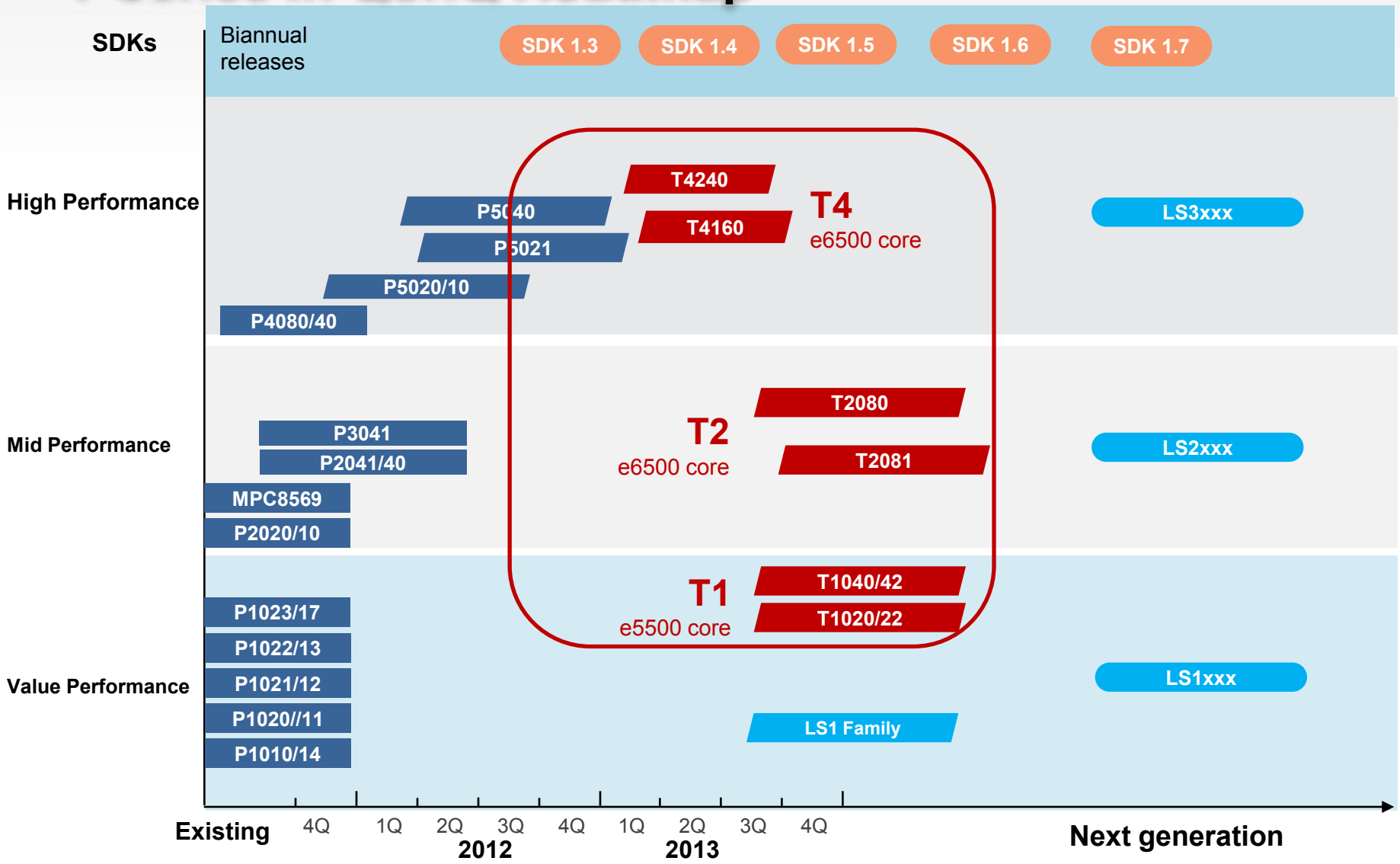
Agenda

- Intro – 28 nm QorIQ portfolio and quick comparison
- T2/T4 key core level features
  - threading /clustering
  - AltiVec
  - MMU HW Tablewalk
- T1 integrated Layer2 Switch
- T1/T2/T4 DPAA (Data-Path) enhancements
- Power Management

T Series in QorIQ Roadmap



Production | Execution | Planning | Proposal

Production

Sample

freescale™

Networking Processors Markets and Applications

Service Provider

Core routers

RNC

Edge routers

Central office / broadband access

Enterprise/Data Center

Multiservice routers

WLAN access points

Ethernet switches

Security / UTM appliances

Industrial & Aerospace

Factory & building automation

Machine to machine communications

Power protection

Medical imaging & networks

Aerospace communications, radar, sonar

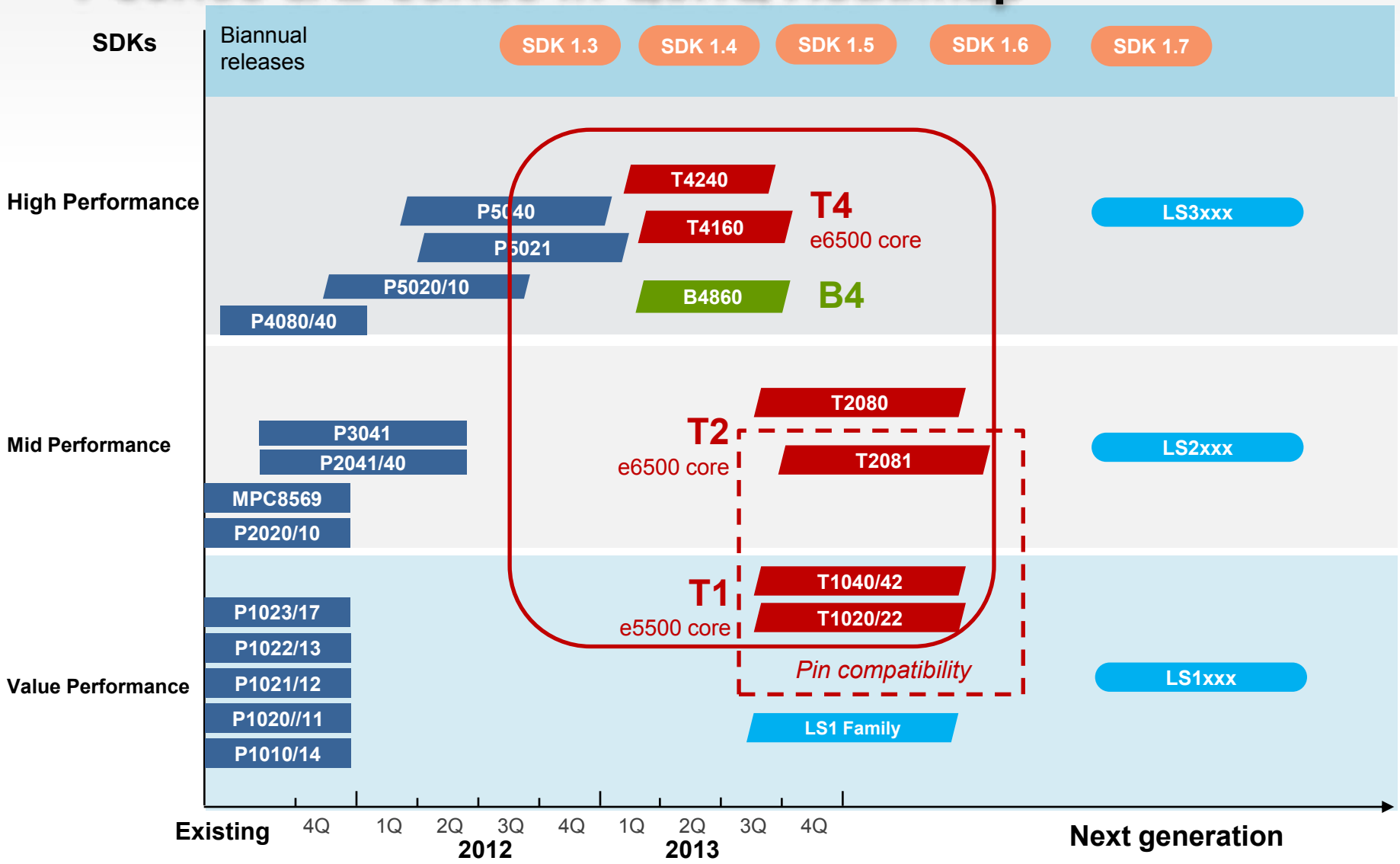
SOHO / Consumer

Home media distribution

Residential gateways

Small form-factor control systems

T-series & B-series in QorIQ Roadmap



Production | Execution | Planning | Proposal

Production

Sample

Complete Femto to Macro Product Portfolio

B4860 Macro SoC

- Very high throughputs
- Thousands of users
- Multi sector
- Multi-standard and multi-mode
- Full compliance to 3GPP Rel. 10
- New advanced cores and acceleration technologies
- Ready for cloud and HetNet deployments

BSC9132 Pico SoC

- 32 to 100 users (LTE (FDD, TDD), WCDMA) and multi-mode
- 2 MPU + 2 DSP + wireless accelerators

BSC9131 Femto SoC

- 8 to 16 users (LTE (FDD, TDD), WCDMA, CDMAx) and multi-mode
- 1 MPU + 1 DSP + wireless accelerators

T Series at a Glance- Comparison

	T1	T2	T4/B4
Cores	2 to 4 cores **e5500** 32b/64b up to 1.4 GHz	**e6500** 32b/64b **Dual-thread** up to 1.8 GHz	**e6500** 32b/64b **Dual-thread** up to 1.8 GHz
Altivec	–	✓	✓
MMU / HW Tablewalk	–	✓	✓
DDR	DDR3L/DDR4	DDR3/DDR3L	DDR3/DDR3L
Integrated Layer2 Switch	✓	–	–
DPAA	Enhanced	Enhanced	Enhanced
Power Mgmt	✓	Enhanced	Enhanced

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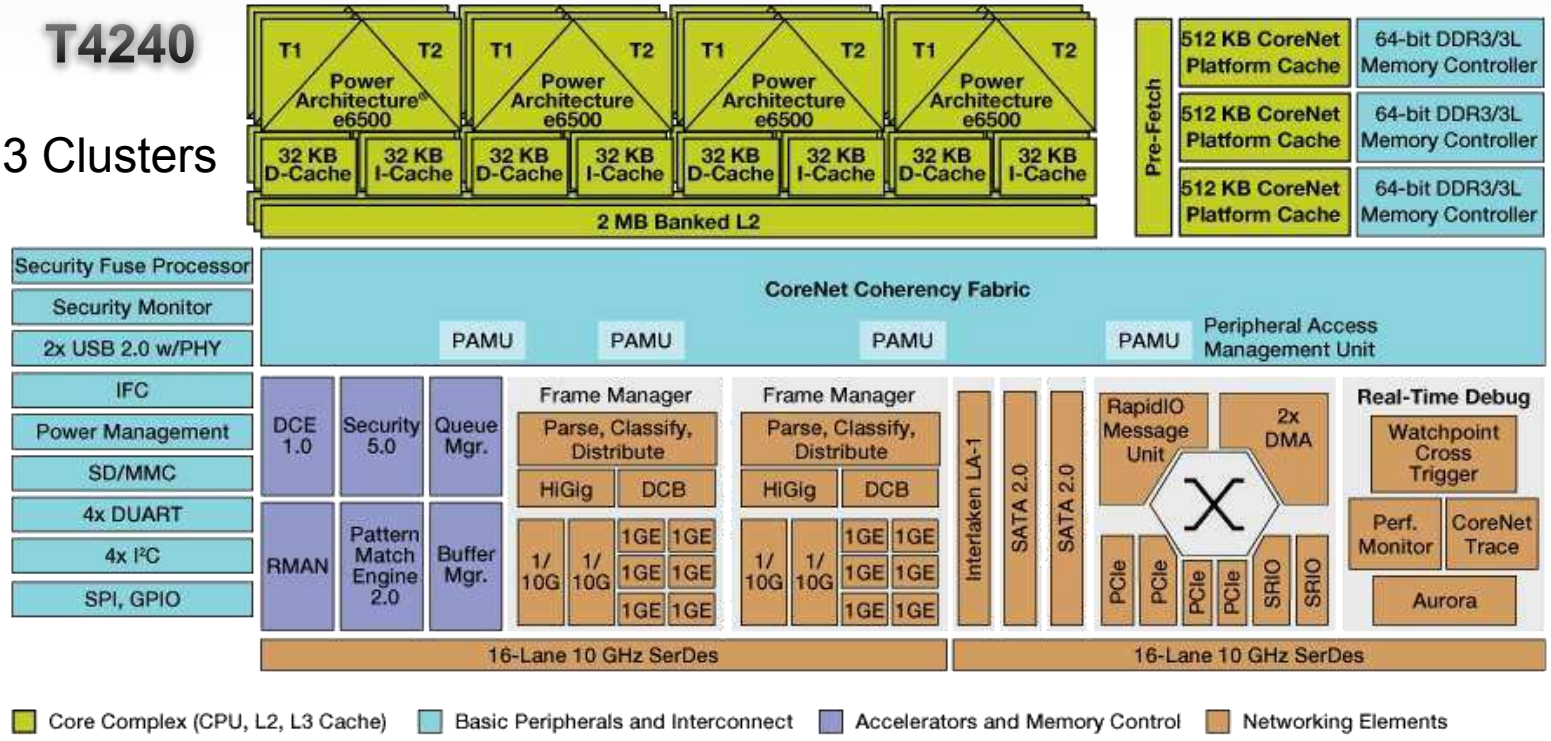
QorIQ Multicore T-series 28 nm – T4/T2

T4240

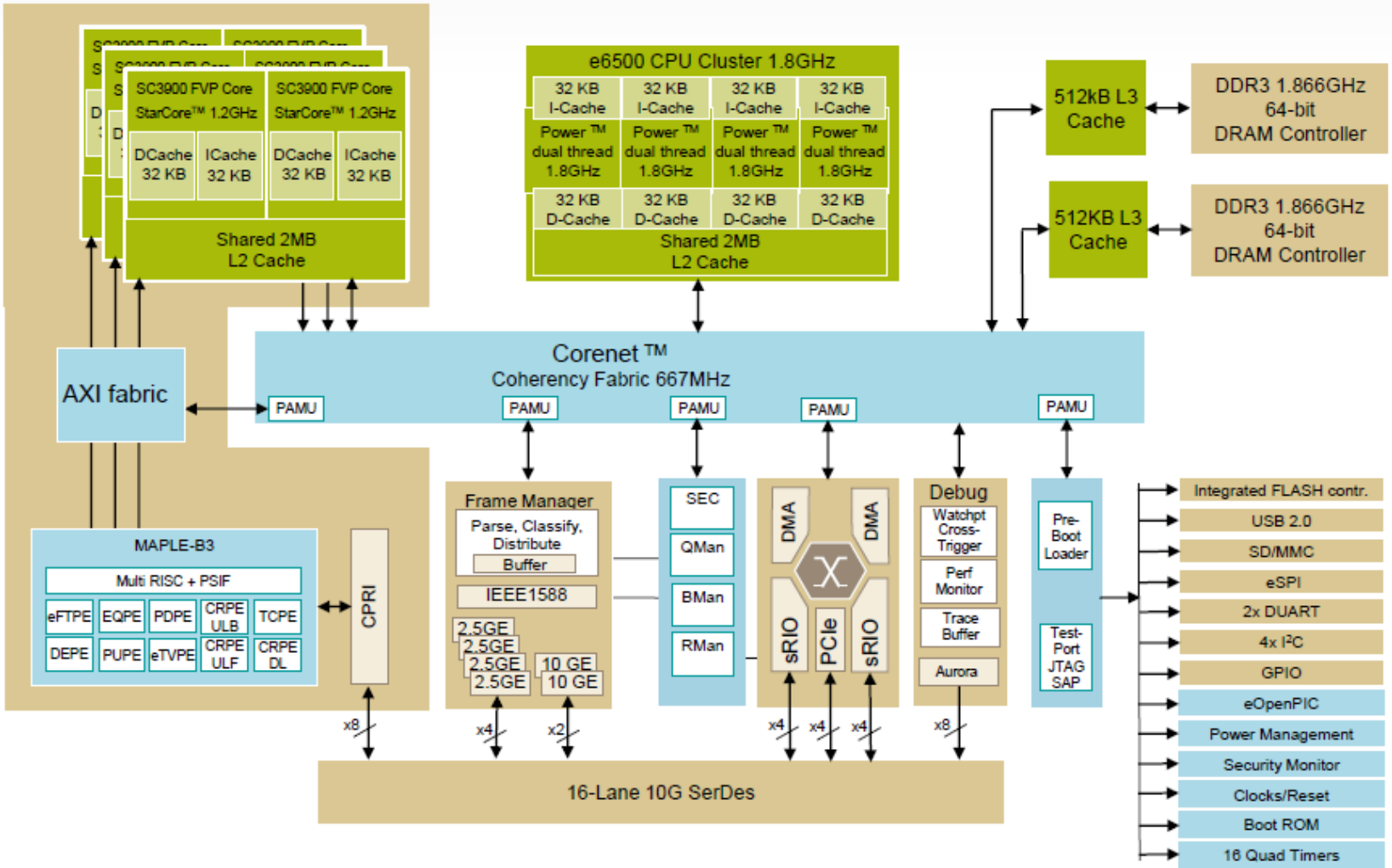
3 Clusters



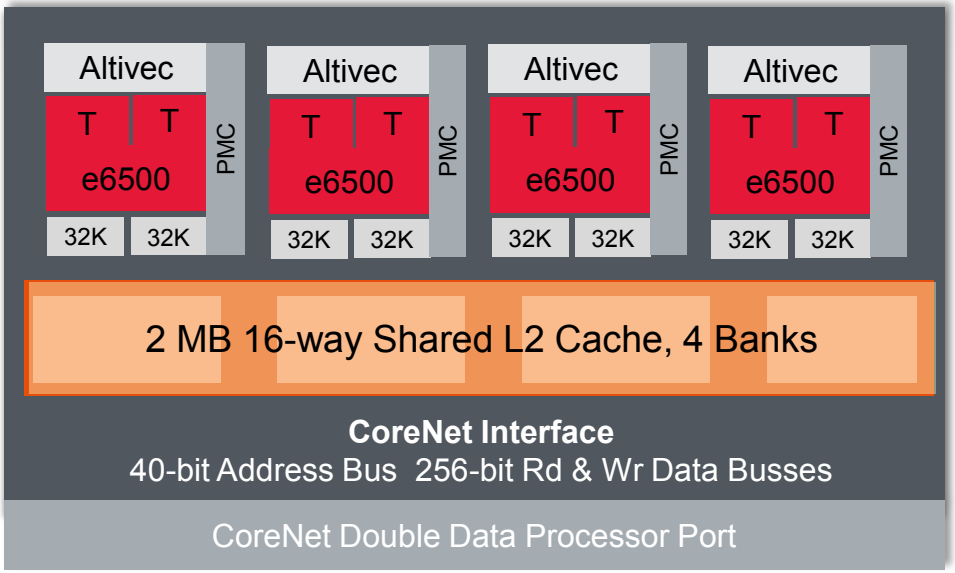
T4240: three cluster **12xcore**/24xthread e6500 32/64b w/ Altivec , **three** DDR controllers
T4160: two clusters **8xcore**/16xthread e6500 32/64b w/ Altivec , **two DDR** controllers
T2080/2081: one cluster **4xcore**/8xthread e6500 32/64b w/ Altivec , **one DDR** controllers

*** T2081 pin-compatible with T1**

QorIQ Qonverge B4860/B4420



e6500 Core Cluster



64-bit Power Architecture®

Up to 2.0 GHz operation

Dual thread per core
SMT – Simultaneous Multi-Threading, provides effective parallel execution

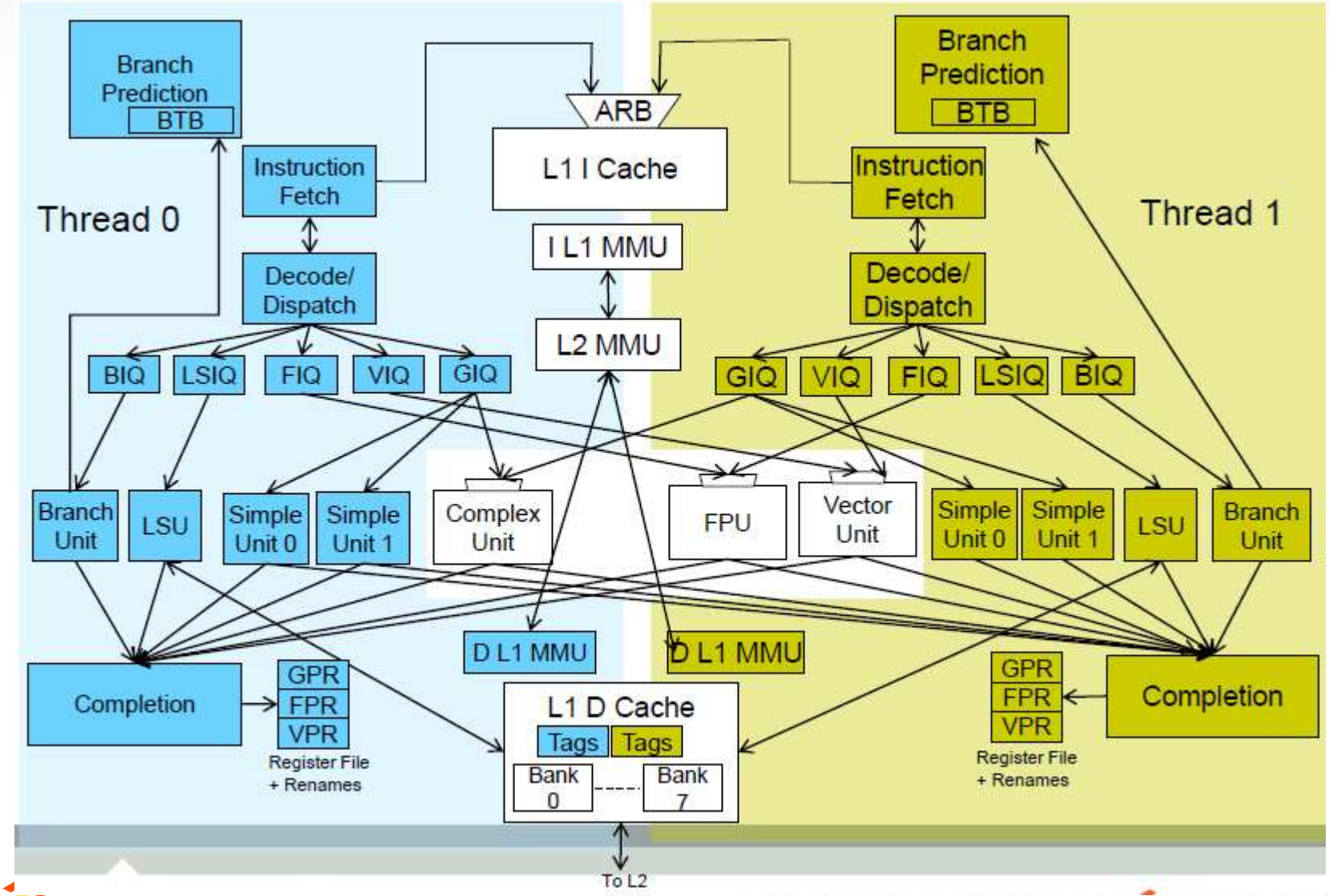
L2 in cluster of 4 cores
- 2 MB 16-way, 4 banks
- Supports L2 memory sharing and allocation to core or thread

AltiVec SIMD unit (128b)
- 8,16,32-bit signed/unsigned integer
- 32-bit floating-point
  - 192 GFLOP
- 8,16,32-bit Boolean

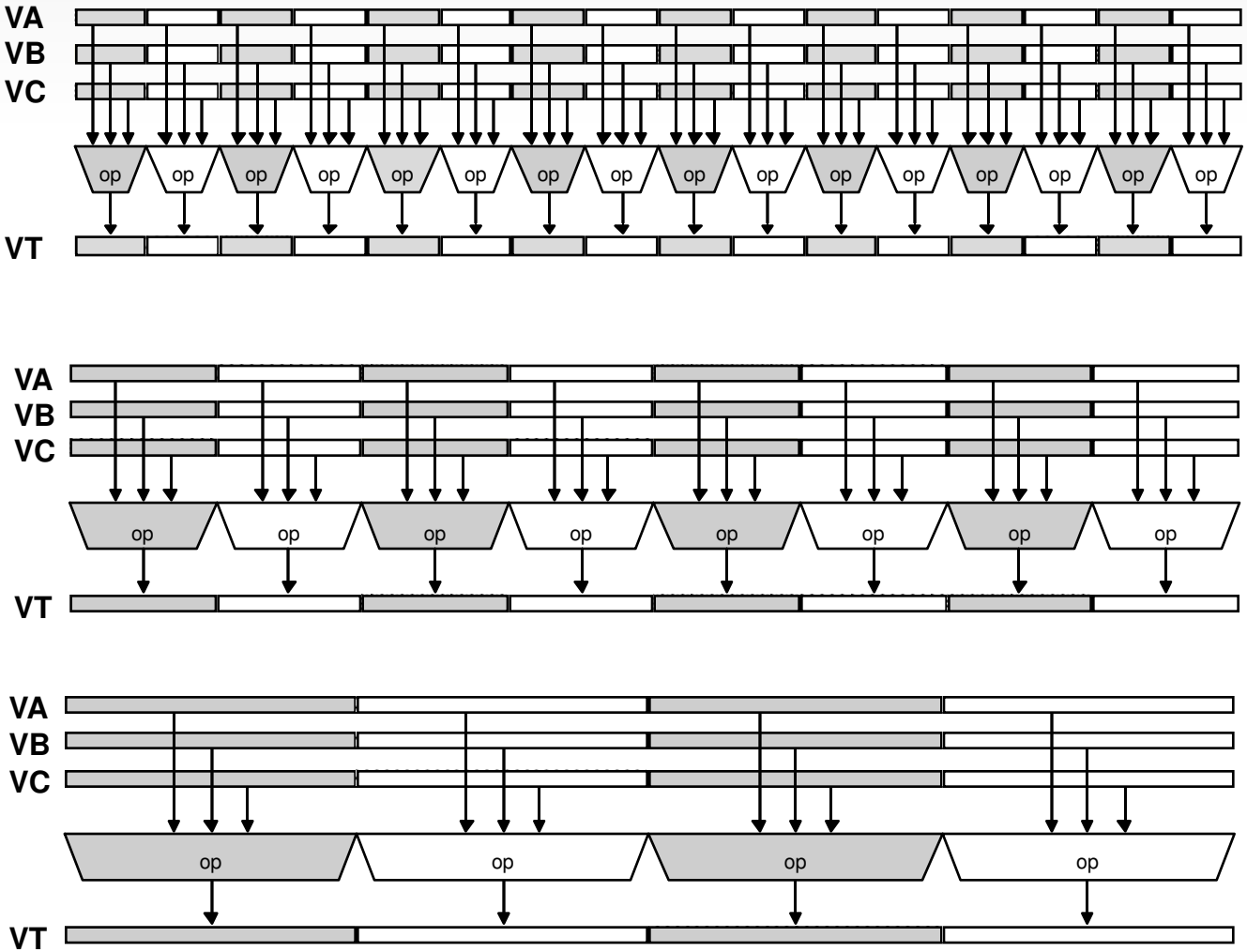
MMU
- 64-entry TLB variable Pages (4KB to 1TB)
- 1024-entry 4K Pages
- HW Tablewalk and LRAT

Power management enhancements (Clock & power gating)

e6500 core SMT dual-thread implementation



AltiVec - SIMD Intra-element Instructions



SIMD principle:

- one **single** instruction performs the **same operation 4 or 8 or 16 times** on operands in 128-bit registers
- **8-bit, 16-bit, 32-bit operands** can be integers, boolean or floating-point reals

AltiVec in QorIQ T-Serie

AltiVec Basic features:

- 32 registers, each 128-bit wide
- Vector packs:
  - 16 8-bit
  - 8 16-bit
  - 4 32-bit integers
  - 4 32-bit single-precision floating-point data
- 156 Instructions
- Four fully pipelined independent execution units:
  - VPU (Permute, Byte manipulation)
  - VSIU (Simple Integer)
  - VCIU (Complex Integer)
  - VFPU (Floating-Point- SP)
- Up to 2x vector instructions per cycle to ANY vector unit

e6500 enhancements over e600:

- Move from GPR to VR
- Absolute differences operation
- Extended support for misaligned vectors, handling head and tail of vectors

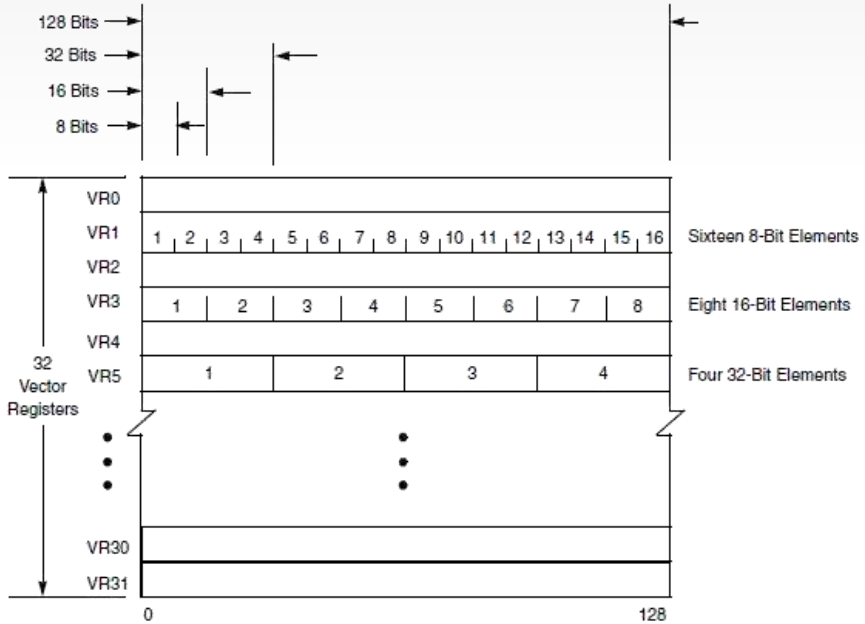


Figure 2-3. Vector Registers (VRs)

FP Performance:

- e6500 core: **14.4** GFLOPS with AltiVec FPU
- T4240/1.8GHz: **172.8** GFLOPS total SoC
- T2080/1.8GHz: **57.6** GFLOPS total SoC

(Frequ x 4 FP MAC per 128b instr. x 2 FP op. per MAC)

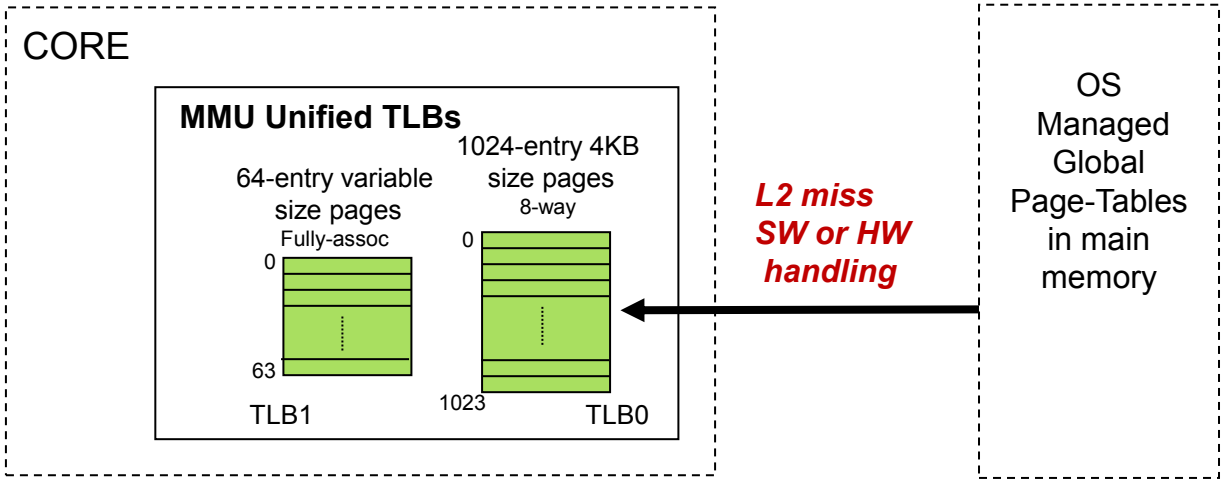
AltiVec – References and SW enablement

Available from www.freescale.com:

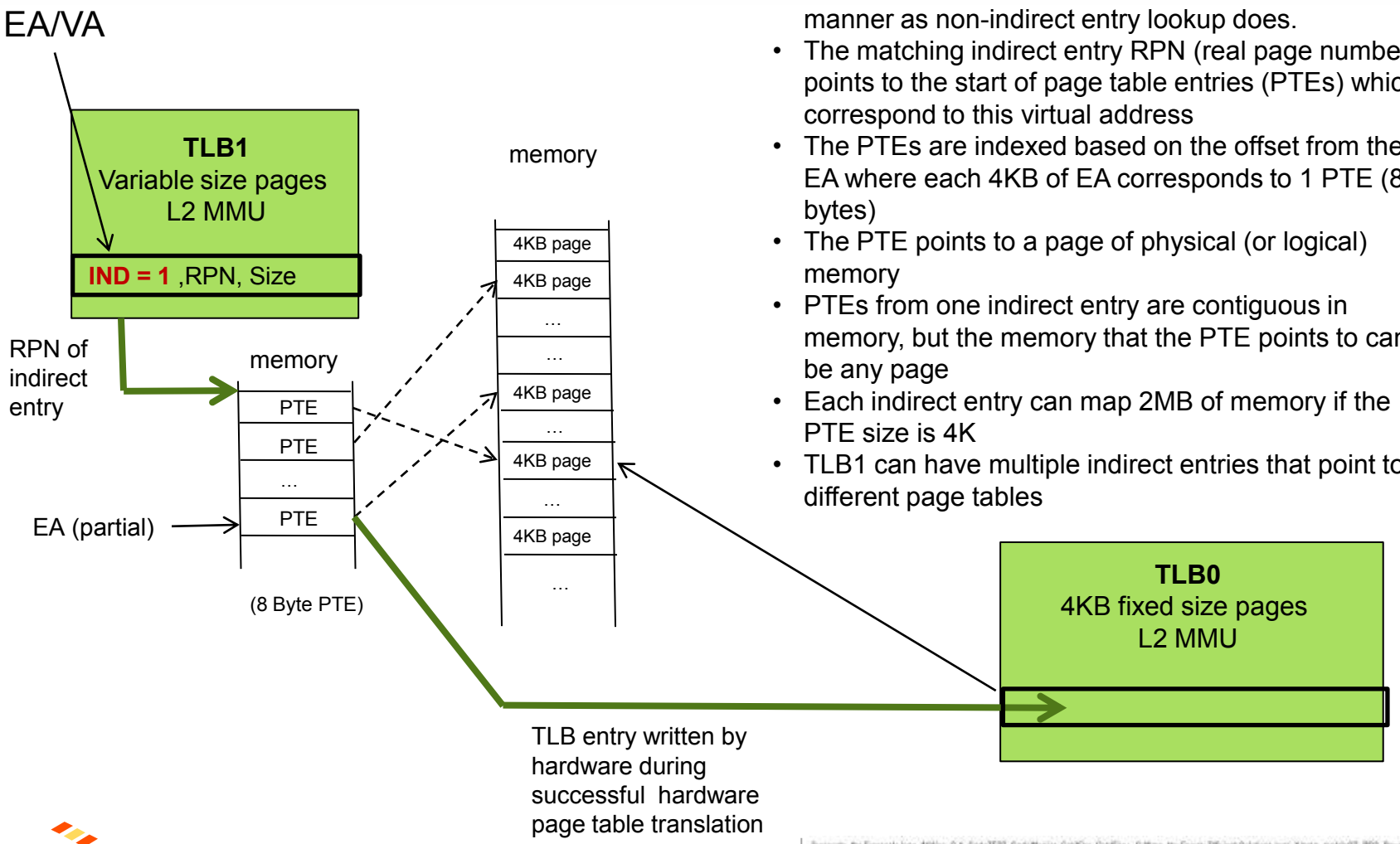
- AltiVec™ Technology Programming Environments Manual
  (Ref. guide for assembler programmers)
- AltiVec Technology Programming Interface Manual
  (Ref. guide for high-level programmers)
- Altivec enabled libc library (LIBMOTOVEC.ZIP)
  (memcpy, memmove, memcmp, memchr, bcopy, bzero
  strlen, strcmp, strcpy, strncpy, checksum)
- Altivec code samples
  (FIR, FFT, math subroutines, pixel conversion …)
- Mentor® Embedded Performance Library for Freescale's AltiVec

e6500 MMU - Hardware Tablewalk

- e6500 can perform hardware tablewalks when translations miss in the MMU
  - The e6500 hardware tablewalk is Linux friendly (it is not like the PowerPC classic hardware tablewalk, not a reversed hashed page table)
  - The definition comes from Power ISA 2.06
  - It defines a page table structure and PTE (page table entry) in-memory format which is compatible with what native Linux uses.



Page Table Translation



- The indirect entry that matches the virtual address is looked up in TLB1
- the address range defined by the EPN field and TSIZE (page size) field describe the range of addresses that the indirect entry maps. All other virtual address identifiers are used in the same manner as non-indirect entry lookup does.
- The matching indirect entry RPN (real page number) points to the start of page table entries (PTEs) which correspond to this virtual address
- The PTEs are indexed based on the offset from the EA where each 4KB of EA corresponds to 1 PTE (8 bytes)
- The PTE points to a page of physical (or logical) memory
- PTEs from one indirect entry are contiguous in memory, but the memory that the PTE points to can be any page
- Each indirect entry can map 2MB of memory if the PTE size is 4K
- TLB1 can have multiple indirect entries that point to different page tables

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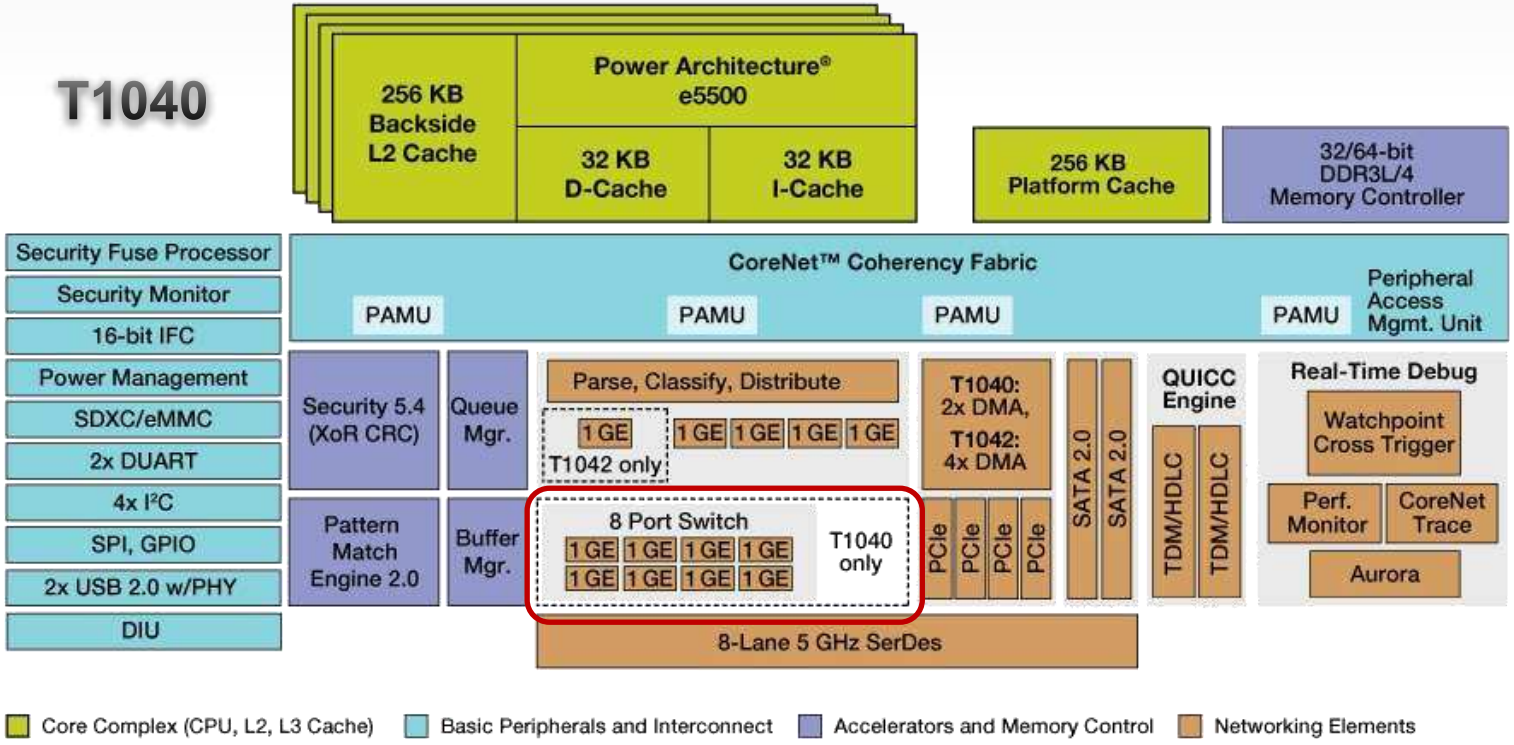
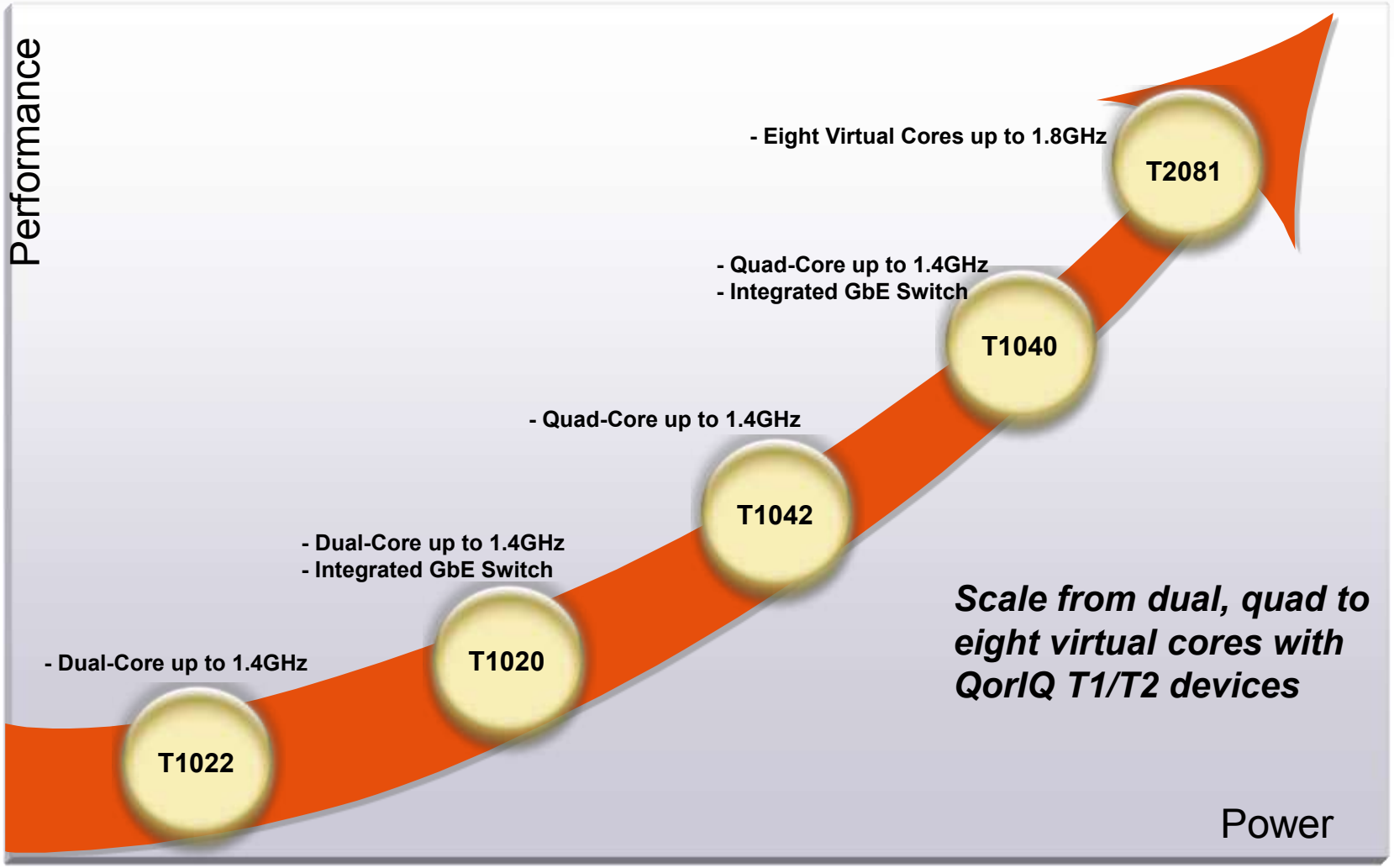
QorIQ Multicore T-series 28 nm - T1



T1040 / T1042 / T1020 / T1022:

- two or four e5500 32/64b cores with private L1/L2 caches
- with or without 8-port L2-Switch

T1/T2 - one of the Industry's Most Scalable, Pin-Compatible Communications Processor Family



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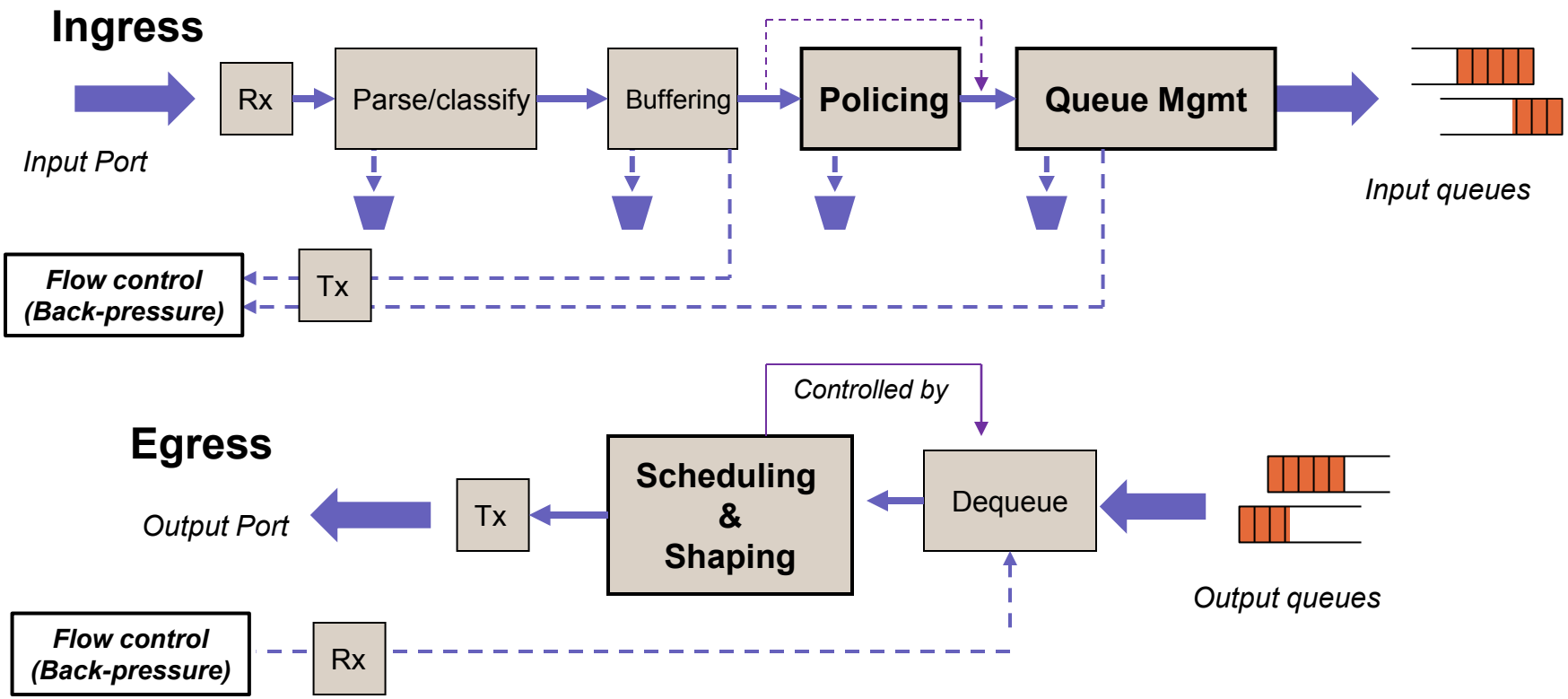
QorIQ P-series to T-series Main DPAA Enhancements

- **FMan**
  - Virtual Storage Profiles: Buffer allocation based on classification (per-flow buffers virtualization)
  - Ingress Multicast support (frame replication)
  - more IP offload acceleration for Fragmentation & Reassembly, IP-Sec, header manipulation
  - support of enhanced Ethernet modes:
    - Data Center Bridging PFC & ETS
    - IEEE802.3az Energy Efficient Ethernet
    - IEEE802.3bf Time sync
- **QMan**
  - more SW-Portals (2x per Thread + 2) for User+kernel direct access
  - Egress hierarchical shaping/scheduling (CEETM)
  - ''Cascaded Power Mgmt'' support (load-aware)
- **RMan (new Vs P4080) T2/T4**
  - SRIO & DPAA direct interaction (classification & queueing)
- **SEC 5.0**
  - more performance, more algorithms & protocols
- **DCE (new Vs P4/P3/P5) T2/T4**
  - Data Compression Engine

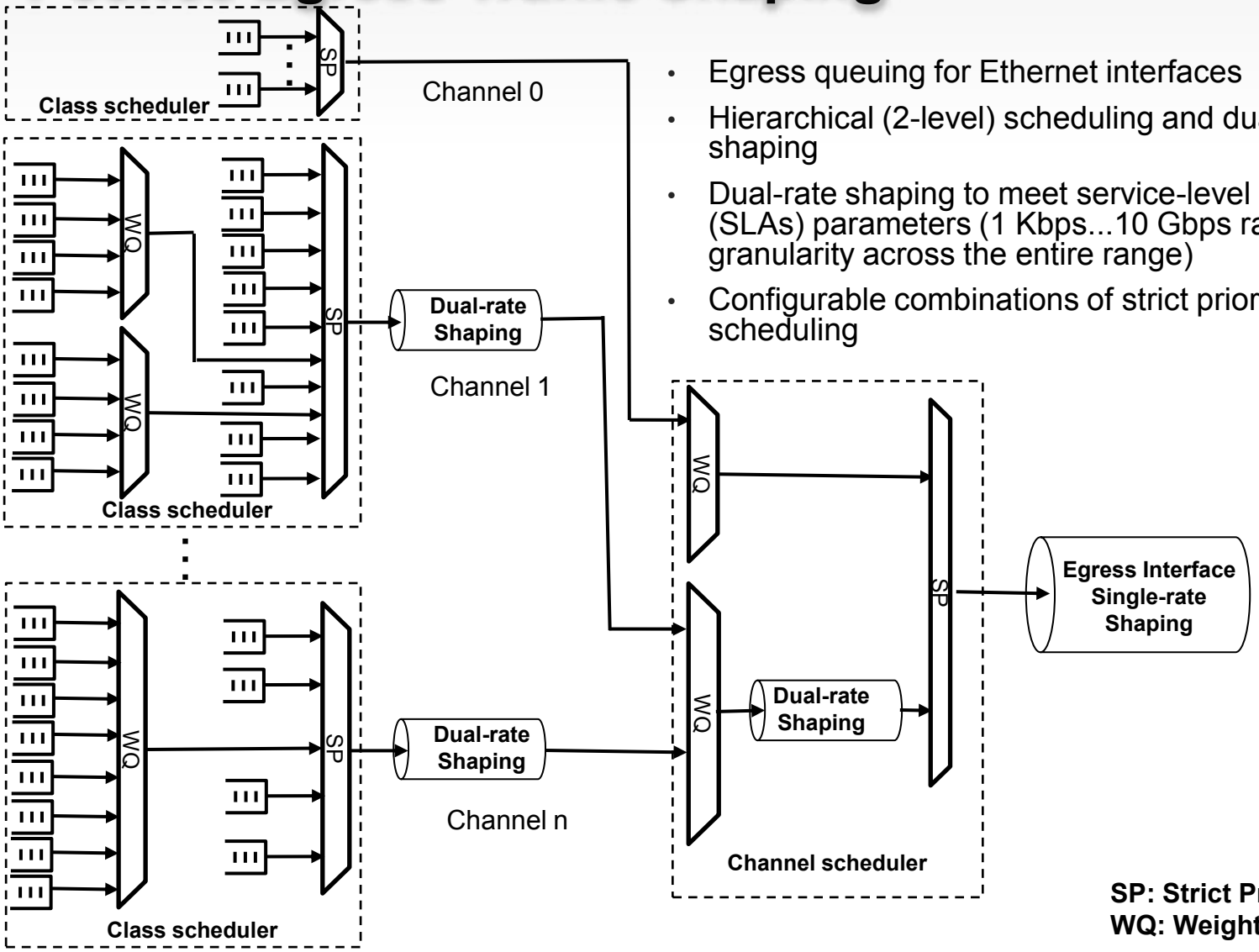
Traffic Management

TM purposes

- ✓ Control traffic against network usage policies/rules
- ✓ Manage congestion situations
- ✓ Provide QoS



T-series Egress Traffic Shaping



- Egress queuing for Ethernet interfaces
- Hierarchical (2-level) scheduling and dual-rate shaping
- Dual-rate shaping to meet service-level agreements (SLAs) parameters (1 Kbps...10 Gbps range, 1 Kbps granularity across the entire range)
- Configurable combinations of strict priority and fair scheduling

SP: Strict Priority
WQ: Weighted Queuing

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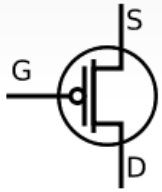
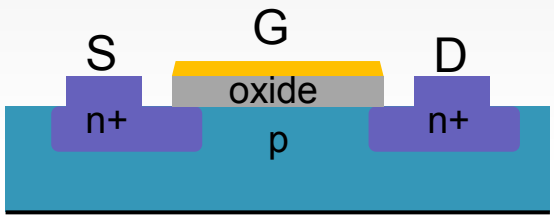
Power Consumption - Background

- Power = Dynamic + Static





$$\text{Power} = \underbrace{\text{Capacitance} \times \text{Frequency} \times \text{Voltage}^2}_{\text{Dynamic}} + \underbrace{\text{Current}_C \times \text{Voltage}}_{\text{Static}}$$

- Dynamic power is related to the activity performed and mainly due to:
  - Charging/discharging capacitor load
  - Dynamic hazards – switching glitches
  - Short-circuit currents

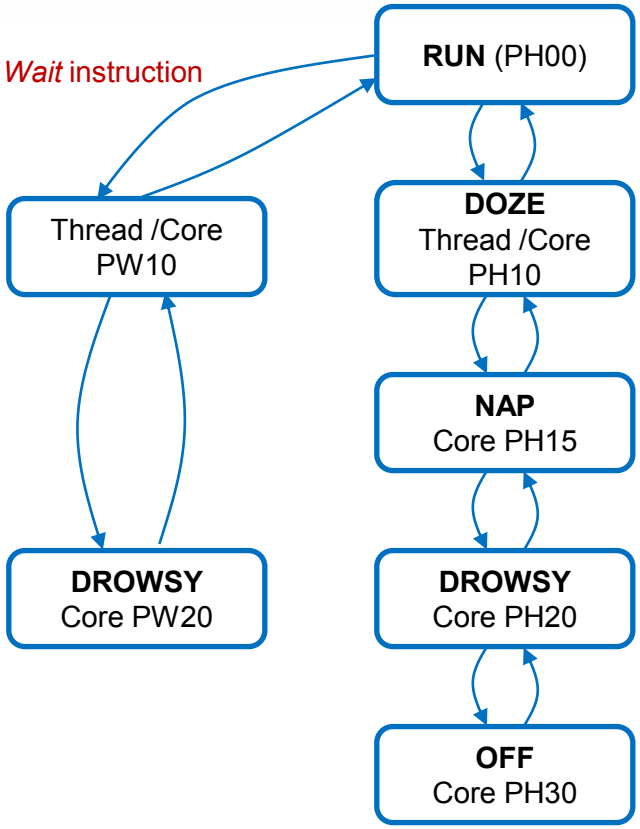
  Can be reduced thru **frequency adaption** and **clock gating**
- Static power is not activity related and mainly due to:
  - Drain leakage
  - Junction leakage
  - Gate leakage

  Can be reduced thru voltage adaption and **power gating**

T-series Power Management Features

- All T-series support:
  - Disabling of unused IPs (providing complete clock gating)
  - Core clock frequency adaption controlled by SW (thru several configurable PLLs and division factors)
  - Usual PowerPC reduced power states (Doze/Nap/Sleep)
  - Internal thermal sensor
- In addition in T2 and T4:
  - Addition of **SRPG (State Retention Power Gating)** technology to reduce Static Power in addition to Dynamic (applies to single core, cluster, Altivec levels)

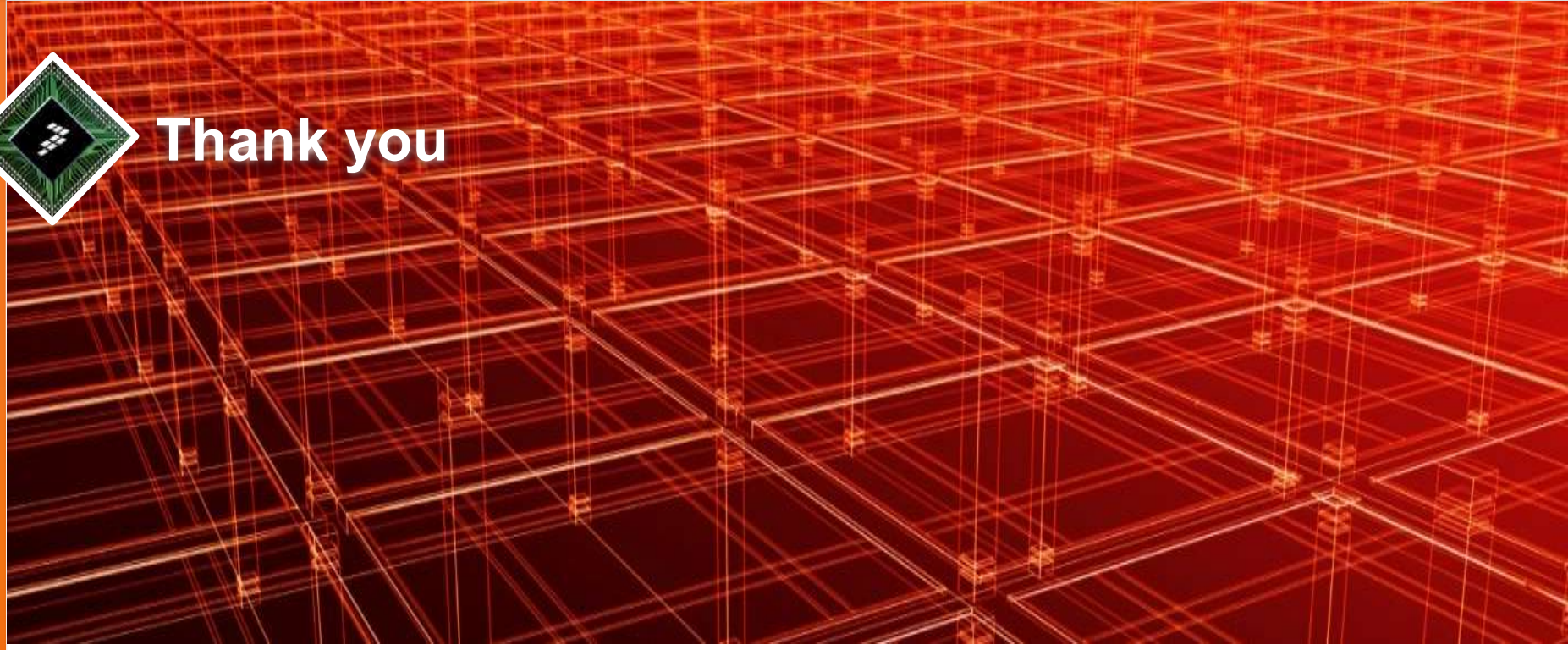
e6500 Core Power States



. Thread suspends instructions
. Clocks kept on
. Core enters PH10 when both threads have signaled entering PH10

. Both threads must be in PH10
. Clocks stopped except TimeBase
. Core state retained
. No snoop on L1, caches must be flushed
. Resumable

. Power Gated w/ state retained
. State and resume similar to NAP



Thank you

… Questions ?

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