Design Note:

HFDN-21.0

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Loop Bandwidth Calculator for the MAX3670

maxim integrated™

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1 Instructions

A Microsoft® Excel spreadsheet has been designed to aid in the setup of the loop bandwidth for the MAX3670 Reference Clock Generator. In order for the MAX3670 to operate properly, the external and internal components that determine the loop bandwidth need to be set up correctly. The spreadsheet calculates the component values needed for proper operation, as shown in Figure 1. To simplify the spreadsheet (shown in Figure 2) the input parameters are indicated in **RED**, and the output parameters are indicated in **BLACK**. The calculator (spreadsheet) can be downloaded at:

http://pdfserv.maxim-ic.com/arpdf/AppAttachments/1hfdn210.zip

The Loop Bandwidth Setup section below gives an overview of the implemented calculations. For more detail refer to the application note HFDN-13.0 Loop-Filter Configuration for the MAX3670 Low-Jitter PLL Reference Clock Generator, and the MAX3670 Data Sheet located at www.maxim-ic.com.

2 Loop Bandwidth Setup

The transfer function of the MAX3670 includes calculations for a zero frequency (f_{ZERO}), the 3dB point (K), and higher order poles (f_{HOP}). The 3dB point of the loop bandwidth is approximated by:

$$K = \frac{K_{PD} R_1 K_{VCO}}{2\pi(N_1 \cdot N_2)}$$

For stability, a zero frequency is added to the loop in the form of a resistor R_1 in series with a capacitor C_1. To minimize peaking the frequency should be placed 100 times lower than K. The location of the zero is approximated as:

$$f_{zero} = \frac{1}{2\pi R_1 C_1}$$

For proper transfer roll off, higher order pole frequencies must be set. To ensure that the overall loop phase-margin is not decreased and jitter peaking is not induced, the f_{HOP} should be placed at approximately 4 times the loop bandwidth (K). The higher order poles are generally implemented with a lowpass filter consisting of R_3 and C_3 directly on the VCO tuning port (VC), which produces a pole at:

$$f_{HOP} = \frac{1}{2\pi R_3 C_3}$$

It may be necessary to provide filtering via a compensation capacitor C_2 when using large values of R_1 and N_1 x N_2 to prevent clipping in the op amp. With C_2 a pole can be produced at:

$$f_{HOP} = \frac{1}{2\pi(20k\Omega)(C_2)}.$$

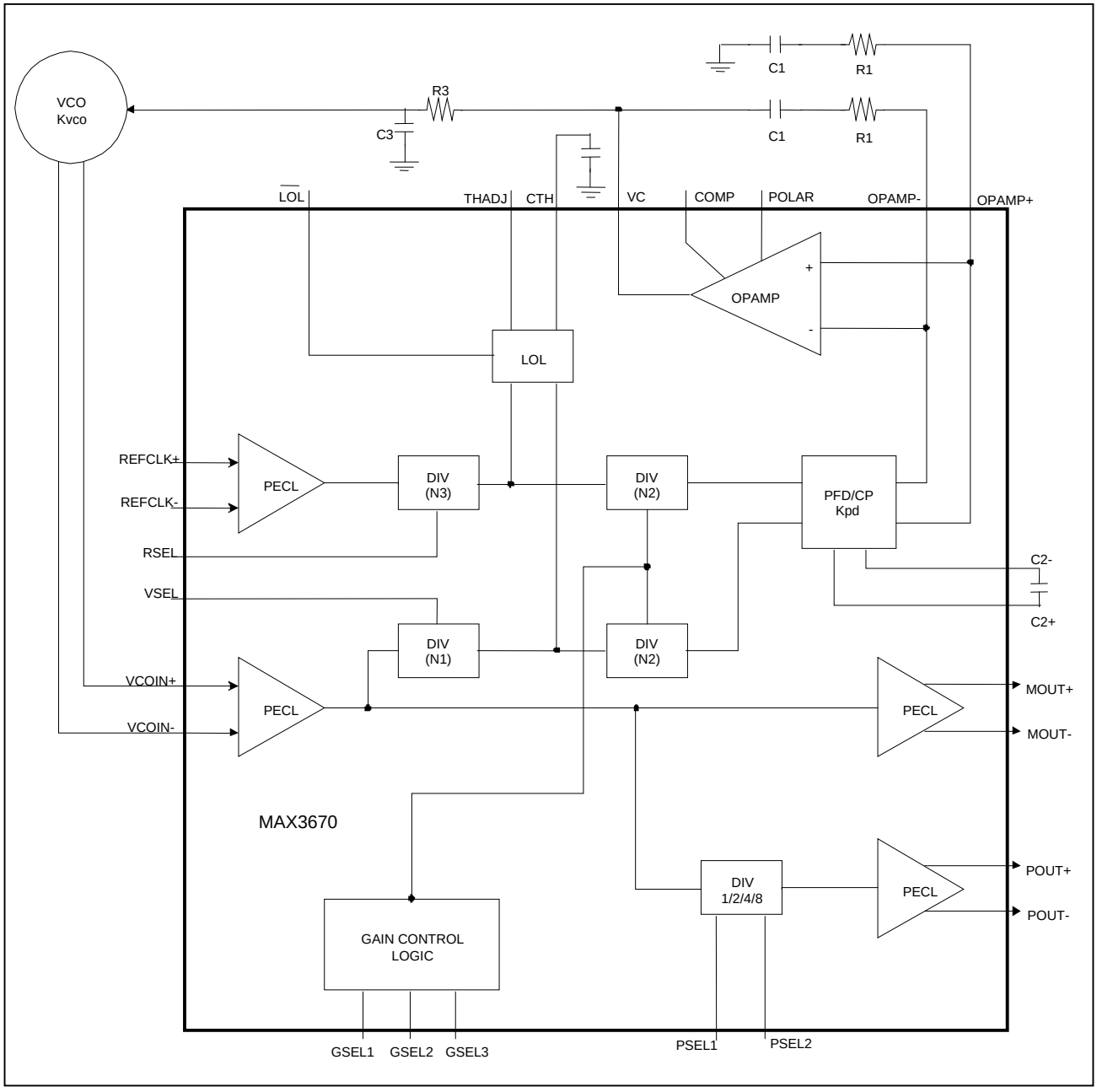

Figure 1. Functional Diagram

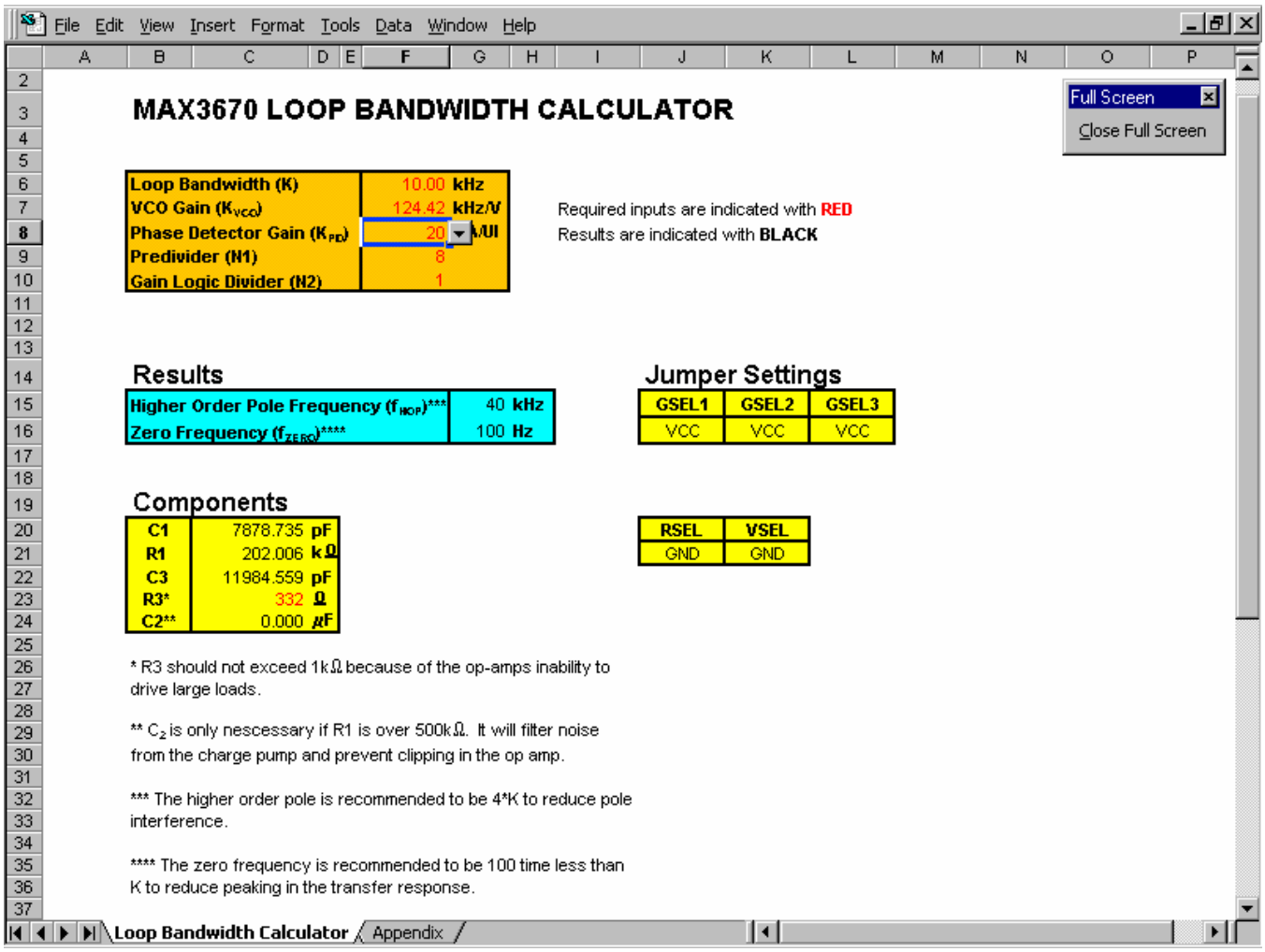

Figure 2. Excel Spreadsheet