AN-6005

Synchronous buck MOSFET loss calculations with Excel model

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Abstract

The synchronous buck circuit is in widespread use to provide "point of use" high current, low voltage power for CPU's, chipsets, peripherals etc. Typically used to convert from a 12V or 5V "bulk" supply, they provide outputs as low as 0.7V for low voltage CPUs made in sub-micron technologies.

The majority of the power lost in the conversion process is due to losses in the power MOSFET switches. The profiles of loss for the High-Side and Low-Side MOSFET are quite different.

These low output voltage converters have low duty cycles, concentrating the majority of the conduction loss in the low-side MOSFET.

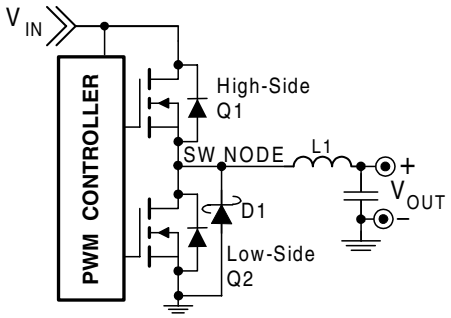


Figure 1. Synchronous Buck output stage

For the examples in the following discussion, we will be analyzing losses for the following synchronous buck converter:

System Parameters		
V_{IN}	12	V
V_{OUT}	1.5	V
I_{OUT}	15	A
F_{SW}	300	kHz

Table 1. Example Synchronous Buck

A spreadsheet to aid in the estimation of synchronous buck losses is available on Fairchild's web site at : https://www.fairchildsemi.com/design/design-tools/switching-loss-calculation-tool/
Operation of the spreadsheet is described in the Appendix at the end of this document.

High-Side Losses:

The power loss in any MOSFET is the combination of the switching losses and the MOSFET's conduction losses.

$$P_{MOSFET} = P_{SW} + P_{COND} \quad (1)$$

Q1 (Figure 1) bears the brunt of the switching losses, since it swings the full input voltage with full current through it. In low duty cycle converters (for example: $12V_{IN}$ to $1.8V_{OUT}$) switching losses tend to dominate.

High-Side Conduction Losses:

Calculating high-side conduction loss is straightforward as the conduction losses are just the I^2R losses in the MOSFET times the MOSFET's duty cycle:

$$P_{COND} = I_{OUT}^2 \bullet R_{DS(ON)} \bullet \frac{V_{OUT}}{V_{IN}} \quad (2)$$

where $R_{DS(ON)}$ is @ the maximum operating MOSFET junction temperature ($T_{J(MAX)}$).

The maximum operating junction temperature is equation can be calculated by using an iterative technique. Since

$R_{DS(ON)}$ rises with T_J and

T_J rises with P_D (dissipated power) and

P_D is largely being determined by $I^2 \times R_{DS(ON)}$.

The spreadsheet calculator iterates the die temperature and accounts for the MOSFET's positive $R_{DS(ON)}$ temperature coefficient. Iteration continues in the "DieTemp" custom function until the die temperature has stabilized to within 0.01°C.

High-Side Switching Losses:

The switching time is broken up into 5 periods (t1-t5) as illustrated in Figure 3. The top drawing in Figure 3 shows the voltage across the MOSFET and the current through it. The bottom timing graph represents V_{GS} as a function of time. The shape of this graph is identical to the shape of the Q_G curve contained in MOSFET datasheets, which assumes the gate is being driven with a constant current. The Q_G

notations indicate which QG is being charged during the corresponding time period.

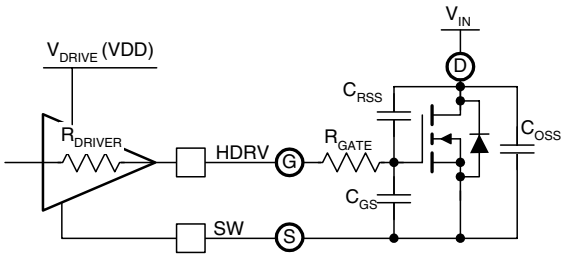
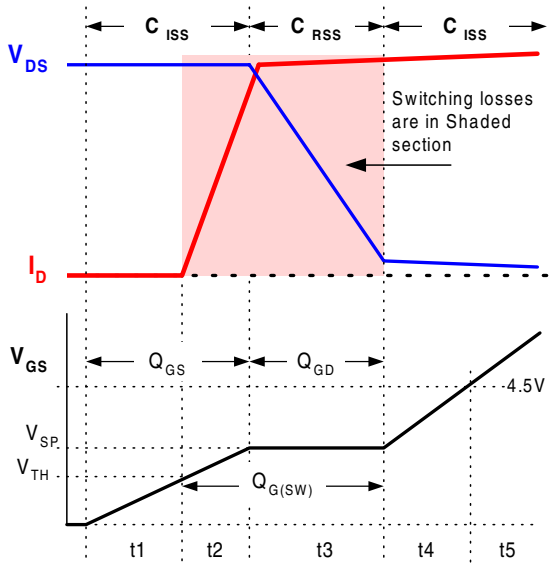


Figure 2. Drive Equivalent Circuit



$C_{ISS} = C_{GS} + C_{RSS}$

Figure 3. High-Side Switching losses and Q_G

The switching interval begins when the high-side MOSFET driver turns on and begins to supply current to Q1's gate to charge its input capacitance. There are no switching losses until V_{GS} reaches the MOSFET's V_{TH}. therefore $P_{t1} = 0$.

When V_{GS} reaches V_{TH}, the input capacitance (C_{ISS}) is being charged and I_D (the MOSFET's drain current) is rising linearly until it reaches the current in L1 (I_L) which is presumed to be I_{OUT}. During this period (t2) the MOSFET is sustaining the entire input voltage across it, therefore, the energy in the MOSFET during t2 is:

$$E_{t2} = t2 \bullet \left(\frac{V_{IN} \bullet I_{OUT}}{2} \right) \quad (3)$$

Now, we enter t3. At this point, I_{OUT} is flowing through Q1, and the V_{DS} begins to fall. Now, all of the gate current will be going to recharge C_{GD}. C_{GD} is similar to the "Miller" capacitance of bipolar transistors, so t3 could be thought of as "Miller time". During this time the current is constant (at I_{OUT}) and the voltage is falling fairly linearly from V_{IN} to 0, therefore:

$$E_{t3} = t3 \bullet \left(\frac{V_{IN} \bullet I_{OUT}}{2} \right) \quad (4)$$

During t4 and t5, the MOSFET is just fully enhancing the channel to obtain its rated $R_{DS(ON)}$ at a rated V_{GS}. The losses during this time are very small compared to t2 and t3, when the MOSFET is simultaneously sustaining voltage and conducting current, so we can safely ignore them in the analysis.

The switching loss for any given edge is just the power that occurs in each switching interval, multipied by the duty cycle of the switching interval:

$$P_{SW} = \left(\frac{V_{IN} \bullet I_{OUT}}{2} \right) (t2 + t3)(F_{SW}) \quad (5)$$

Now, all we need to determine are t2 and t3. Each period is determined by how long it takes the gate driver to deliver all of the charge required to move through that time period:

$$t_x = \frac{Q_{G(x)}}{I_{DRIVER}} \quad (6)$$

Most of the switching interval is spent in t3, which occurs at a voltage we refer to as "V_{SP}", or the "switching point" voltage. While this is not specifically specified in most MOSFET datasheets, it can be read from the Gate Charge graph, or approximated using the following equation:

$$V_{SP} \approx V_{TH} + \frac{I_{OUT}}{G_M} \quad (7)$$

where G_M is the MOSFET's transconductance, and V_{TH} is its typical gate threshold voltage.

With V_{SP} known, the gate current can be determined by Ohm's law on the circuit in Figure 2:

$$I_{DRIVER(L-H)} = \frac{V_{DD} - V_{SP}}{R_{DRIVER(PULL-UP)} + R_{GATE}} \quad (8A)$$

$$I_{DRIVER(H-L)} = \frac{V_{SP}}{R_{DRIVER(PULL-DOWN)} + R_{GATE}} \quad (8B)$$

The rising time (L-H) and falling times (H-L) are treated separately, since I_{DRIVER} can be different for each edge.

The V_{GS} excursion during t2 is from V_{TH} to V_{SP}. Approximating this as V_{SP} simplifies the calculation considerably and introduces no significant error. This approximation also allows us to use the $Q_{G(SW)}$ term to represent the gate charge for a MOSFET to move through the switching interval. A few

MOSFET manufacturers specify $Q_{G(SW)}$ on their data sheets. For those that don't, it can be approximated by:

$$Q_{G(SW)} \approx Q_{GD} + \frac{Q_{GS}}{2} \quad (9)$$

so the switching times therefore are:

$$t_{S(L-H)} = \frac{Q_{G(SW)}}{I_{DRIVER(L-H)}} \quad (10A)$$

$$t_{S(H-L)} = \frac{Q_{G(SW)}}{I_{DRIVER(H-L)}} \quad (10B)$$

The switching loss discussion above can be summarized as:

$$P_{SW} = \left(\frac{V_{IN} \times I_{OUT}}{2}\right)(F_{SW})\left(t_{S(L-H)} + t_{S(H-L)}\right) \quad (10C)$$

There are several additional losses that are typically much smaller than the aforementioned losses. Although their proportional impact on efficiency is low, they can be significant because of where the dissipation occurs (for example, driver dissipation). They are listed in order of importance:

1. The power to charge the gate:

$$P_{GATE} = Q_G \times V_{DD} \times F_{SW} \quad (11A)$$

Note that P_{GATE} is the power from the VDD supply required to drive a MOSFET gate. It is independent of the driver's output resistance and includes both the rising and falling edges.

P_{GATE} is distributed between R_{DRIVER}, R_{GATE}, and $R_{DAMPING}$ propoprtional to their resistances. Dissipation in the driver for the rising edge is:

$$P_{DR(L-H)} = \frac{P_{GATE} \bullet R_{DRIVER(PULL-UP)}}{2(R_{TOTAL})} \quad (11B)$$

where

$$R_{TOTAL} = R_{DRIVER} + R_{GATE} + R_{DAMPING} \quad (11C)$$

Similarly, dissipation in the driver for the falling edge is:

$$P_{DR(H-L)} = \frac{P_{GATE} \bullet R_{DRIVER(PULL-DOWN)}}{2(R_{TOTAL})} \quad (11D)$$

For an output stage (Driver + MOSFET) with the following parameters:

P_{GATE}	500	mW
$R_{DRIVER\ (PULL-UP)}$	5	Ω
$R_{DRIVER\ (PULL-DOWN)}$	2	Ω
$R_{DAMPING}$	2	Ω
R_{GATE}	1.5	Ω

Driver dissipation calculates to :

$$P_{DR(H-L)} = \frac{500 * 5}{2(8.5)} = 147mW \quad (11E)$$

$$P_{DR(L-H)} = \frac{500 * 2}{2(5.5)} = 91mW \quad (11F)$$

$$P_{DRIVER} = P_{DR(H-L)} + P_{DR(L-H)} = 238mW \quad (11G)$$

2. The power to charge the MOSFET's output capacitance:

$$P_{COSS} \approx \frac{C_{oss} \bullet V_{IN}^2 \bullet F_{SW}}{2} \quad (11H)$$

where C_{OSS} is the MOSFETs output capacitance, (C_{DS} +C_{DG}).

3. If an external schottky is used across Q2, the Schottky's capacitance needs to be charged during the high-side MOSFET's turn-on:

$$P_{C(SCHOTTKY)} = \frac{C_{SCHOTTKY} \bullet V_{IN}^2 \bullet F_{SW}}{2} \quad (12A)$$

If a Schottky diode is not used:

4. Reverse recover power for Q2's body diode:

$$P_{QRR} = Q_{RR} \bullet V_{IN} \bullet F_{SW} \quad (12B)$$

where Q_{RR} is the body diode's reverse recovery charge. If the MOSFET contains an integrated body diode (like SyncFET™), the Q_{RR} figure in the datasheet is actually Q_{OSS}, or the charge required by the MOSFET's C_{OSS} . If a SyncFET™ is used, then set Q_{RR} to 0 in the companion spreadsheet.

Low-Side Losses

Low-side losses (P_{LS}) are also comprised of conduction losses and switching losses.

$$P_{LS} = P_{SW} + P_{COND} \quad (13)$$

Switching losses are negligible, since Q2 switches on and off with only a diode drop across it, however for completeness we will include the analysis.

Conduction losses for Q2 are given by:

$$P_{COND} = (1 - D) \times I_{OUT}^2 \times R_{DS(ON)} \quad (14)$$

where $R_{DS(ON)}$ is the $R_{DS(ON)}$ of the MOSFET at the anticipated operating junction temperature and $D = \frac{V_{OUT}}{V_{IN}}$ is the duty cycle for the converter.

The junction temperature (T_J) of the MOSFET can be calculated if the junction to ambient thermal resistance (θ_{JA}) and maximum ambient temperature are known.

$$T_J = T_A + (P_{LS} \bullet \theta_{JA}) \quad (15)$$

P_{COND} dominates P_{LS}. Since $R_{DS(ON)}$ determines P_{COND} , and is a function of T_J, either an iterative calculation can be used, or T_J can be assumed to be some maximum number determined by the design goals. The calculations in the accompanying spreadsheet use T_A and θ_{JA} iteratively to determine the low-side operating T_J at full current, assuming a MOSFET $R_{DS(ON)}$ temperature coefficient of 0.4%/°C, which is typical for the MOSFETs used in this application.

Low-side Switching Losses

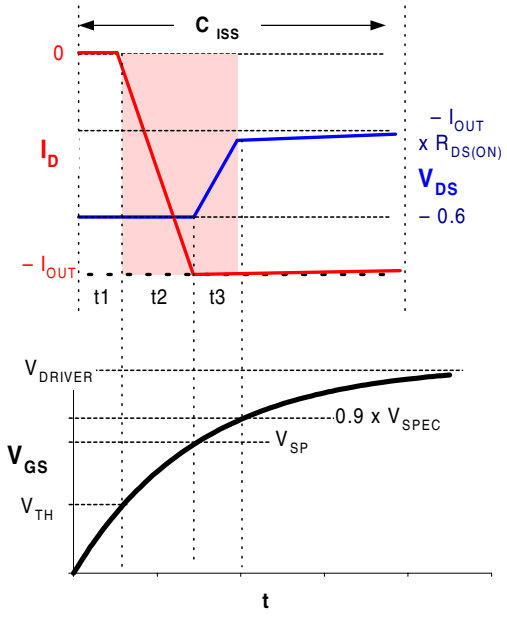


Figure 4. Low-Side turn-on switching loss waveforms

Low-side switching losses for each edge can be calculated in a similar fashion to high-side switching losses:

$$P_{SW(LS)} \approx \left(t2 \bullet V_F + t3 \bullet \frac{V_F + I_{OUT} \bullet 1.1 \bullet R_{DS(ON)}}{2} \right) I_{OUT} \bullet F_{sw} \quad (16)$$

but instead of V_{IN} as in eq. 3, we use V_F , the schottky diode drop (approximated as 0.6V) in the equation. Also, there is almost no Miller effect for the low-side MOSFET, since V_{DS} is increasing (becoming less negative) as we turn the device on, the gate driver is not having to supply charge to C_{GD}. The voltage collapse for Q2 is caused by the $R_{DS(ON)}$ going from $\frac{0.6}{I_{OUT}}$ @ $V_{GS} = V_{SP}$, to 90% of V_{SPEC}, the gate voltage for the highest specified $R_{DS(ON)}$. At 90% of V_{SPEC} the $R_{DS(ON)}$ is typically 110% of the specified $R_{DS(ON)}$.

The rising edge transition times for the low-side (t2 and t3 in Figure 4) can now be calculated from the RC equations.

$$t2_R = K_{2R}(R_{DRIVER} + R_{GATE})\,C_{ISS} \quad (17A)$$

where

$$K_{2R} = \ln\left(\frac{V_{DRIVE}}{V_{DRIVE} - V_{SP}}\right) - \ln\left(\frac{V_{DRIVE}}{V_{DRIVE} - V_{TH}}\right) \quad (17B)$$

$$t3_R = K_{3R}(R_{DRIVER} + R_{GATE})\,C_{ISS} \quad (17C)$$

where

$$K_{3R} = \ln\left(\frac{V_{DRIVE}}{V_{DRIVE} - 0.9V_{SPEC}}\right) - \ln\left(\frac{V_{DRIVE}}{V_{DRIVE} - V_{SP}}\right) \quad (17D)$$

and where C_{ISS} is the MOSFET's input capacitance ($C_{GS} + C_{GD}$) when V_{DS} is near 0V. If the MOSFET datasheet has no graph of capacitance vs. V_{DS}, use 1.25 times the typical C_{ISS} value, which is usually given with ½ of the rated V_{DS} across the MOSFET.

The turn-off losses are the same, but in reverse, so the switching waveforms are:

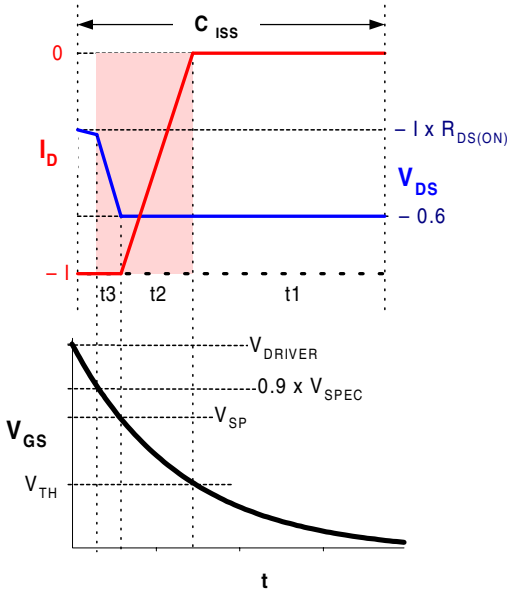


Figure 5. Low-Side turn-off switching loss waveforms

The falling edge transition times for the low-side (t3 and t2 in Figure 5) can now be calculated from the RC equations:

$$t3_F = K_{3F}(R_{DRIVER} + R_{GATE})\,C_{ISS} \quad (18A)$$

where

$$K3_F = \ln\left(\frac{0.9V_{SPEC}}{V_{SP}}\right) \quad (18B)$$

$$t2_F = K_{2F}(R_{DRIVER} + R_{GATE})C_{ISS} \quad (18C)$$

where

$$K2_F = \ln\left(\frac{V_{SP}}{V_{TH}}\right) \quad (18D)$$

Dead-Time (Diode Conduction) Losses

The dead-time is the amount of time that both MOSFETs are off. During this time the diode (body diode or parallel schottky diode) is in forward conduction. It's power loss is:

$$P_{DIODE} = t_{DEADTIME} \bullet F_{SW} \bullet V_F \bullet I_{OUT} \quad (19)$$

where $t_{DEADTIME} = t_{DEADTIME(R)} + t_{DEADTIME(F)}$, which are the deadtimes associated before the SW Node (Figure 1) rises, after Q2 turns off, and after SW Node falls, before Q2 turns on, respectively.

To determine $t_{DEADTIME}$, we need to consider how the driver controls the MOSFET gate drives. Most drivers use "adaptive dead-time circuits, which wait for the voltage of the opposite MOSFET to reach an "off" voltage before beginning to charge its own MOSFET. Most drivers add a fixed delay to prevent shoot-through, especially on the low to high transition.

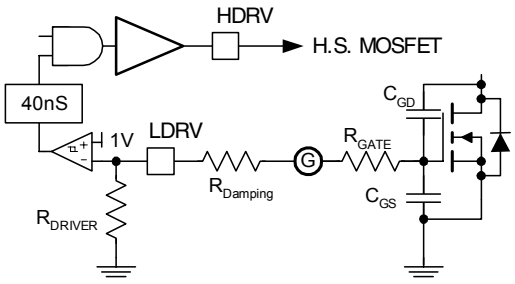


Figure 6. Typical Adaptive Gate drive (low-high transition)

For the $t_{DEADTIME(F)}$ the diode will be conducting the full load current from the time the switch node falls, until the Low-side MOSFET reaches threshold. This "deadtime" consists of 2 portions:

1. $t_{DELAY(F)}$: The driver's built in delay time from detection of $1V_{GS}$ at the high-side MOSFET gate until beginning of low-side MOSFET turn-on, plus
2. t_{TH} : the time for the driver to charge the low-side MOSFET's gate to reach threshold (V_{TH}).

t_{TH} can be approximated by:

$$t_{TH} \approx \frac{Q_{GS}}{2 \bullet I_{LDRV}} \quad (20)$$

This approximation holds, since prior to reaching threshold, the gate voltage is low enough that I_{LDRV} can be approximated with a constant current of

$$I_{LDRV} \approx \frac{V_{DRIVER} - \left(\frac{V_{TH}}{2}\right)}{R_{GATE} + R_{DRIVER}} \quad (21)$$

and typically $Q_{G(TH)} \approx \frac{Q_{GS}}{2}$.

The diode's total on-time on the falling edge is then:

$$t_{DEADTIME(F)} \approx t_{DELAY(F)} + \frac{Q_{GS}(R_{GATE} + R_{DRIVER})}{\left(V_{DRIVER} - \frac{V_{TH}}{2}\right)} \quad (22)$$

On the rising edge, $t_{DELAY(R)}$ is usually much longer to allow the low-side MOSFET's gate to discharge completely. This is necessary since charge is coupled into the low-side gate during the rising edge of the SW node. The peak of the resultant voltage "spike" at the low-side gate is the sum of the amplitude of the injected spike and the voltage the gate has discharged to when the SW node begins to rise. Sufficient delay is necessary to avoid having the resultant peak rise significantly above the low-side's V_{TH} , turning on both MOSFETs, and inducing "shoot-through" losses.

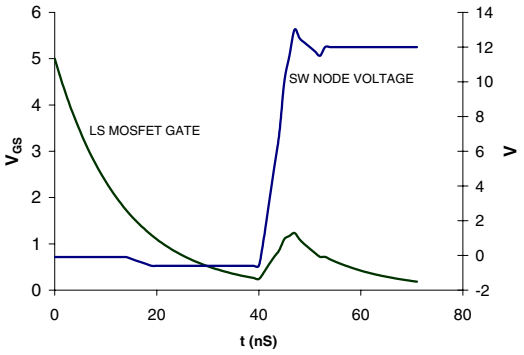


Figure 7. Coupled voltage spike on Low-side MOSFET gate from SW node rising edge

The other component of deadtime on the rising edge is the time it takes for the high-side MOSFET's gate to charge to V_{SP}. This is typically less than 10% of $t_{DELAY(R)}$ so we will ignore it and set:

$$t_{DEADTIME(R)} \approx t_{DELAY(R)} \quad (23)$$

Summary of results

A spreadsheet which contains MOSFET parameters is used to compute the losses for our example circuit (Table 1) using a 5V gate drive with 6Ω pull-up and 2Ω pull-down strength.

	High-Side	Low-Side		
MOSFET	FDD6644	FDB6676	Total	
Switching Loss	1.09	0.31	**1.40**	W
Conduction Loss	0.21	1.15	**1.36**	W
Other Losses			**0.26**	W
Total Losses	**1.30**	**1.46**	**3.02**	W
Output Power			**22.5**	W
Efficiency			**88%**	

Table 2. Results for 15A example (Table 1)

It's instructive to review the results in order to observe a few key points:

- Switching losses for the low-side MOSFET are only 15% of low-side MOSFET's total losses.
- Unless the switching frequency is very high (above 1 Mhz.), the loss contribution due to diode conduction (deadtime loss) is minimal.
- High-side losses are dominated by switching losses since the duty cycle is low.

Appendix: Using the efficiency and loss calculation spreadsheet tool

The spreadsheet is avaiable at the following :

https://www.fairchildsemi.com/design/design-tools/switching-loss-calculation-tool/

The spreadsheet implements the loss calculations described in this app note. To see the sheet in action press the "Run" button on the "EfficiencySummary" sheet.

The controller/driver database models several Fairchild products driver products. A listing of these is found in the ControllerDriver tab.

These detailed instructions can also be found in the " General Instructions" tab of the spreadsheet:

Notes:	Be sure to turn off Macro Protection in Excel to allow the custom functions and macros in this sheet to run. For Excel 2000, this is done through "Tools|Macro|Security". Set the level to "low". In Excel 97, you can do this through "Tools|Options. In the "General" tab, the "Macro Virus Protection" box should **not** be checked.
DieTemp function	RDS(ON) is a function of die temperature, and the die temperature is a function of Power Dissipation which is in turn dependent on RDS(ON). To solve for dissipation or die temperature, the conduction loss calculations in this spreadsheet use an iterative calculation method to arrive at the die temperature and dissipation.

Tabs	Function / Description
Definitions	Provides guidance on what MOSFET parametric data to enter in the "MOSFETDatabase" tab. This sheet is a hotlink destination from some of the column headings in the MOSFETDatabase table.
EfficiencyChart	Plots efficiency data from the table in EfficiencySummary tab.
LossChart	Plots power loss data from the table in EfficiencySummary tab.
ControllerDriver	Database for the IC Controllers. Fairchild's portable PWM controllers are featured in this database. Any controller can be added by using the "Add" button and filling in the appropriate fields.
MOSFETDatabase	Database for the MOSFETs. Many popular Fairchild MOSFETs are featured in this database. Any MOSFET can be added by using the "Add" button and filling in the appropriate fields.
EfficiencySummary	The main sheet where the system requirements and MOSFET choices can be entered, and the data is stored for graphing. To run the graphing routine, push the "RUN" button at the top of the sheet.
Output	The calculations contained in the "Synchronous buck MOSFET loss calculations" app note are programmed into this sheet. The EfficiencySummary macro uses this sheet as its calculator. If a particular operating point needs to be examined in more detail, then use this sheet, and enter the parameters by hand. Be sure to save a copy of this workbook before overwriting formulas in "Output" tab.

Cells are color coded as follows:	
	Indicates user input parameters
	Indicates calculated values that can be overwritten with selected values if desired. These fields default to the calculated value directly above them.
	These fields are written into, or contain formulae that were input on the "EfficiencySummary" sheet.

Macro Security Note:

Switching Loss Calculation Design Tool excel file uses macros extensively. For the spreadsheet to operate properly, check the "Always trust macros from this source" box if a security warning appears, then click the "Enable Macros" button..

This is only required the first time you run a Fairchild spreadsheet tool with macros.