3 November 1994

PRELIMINARY
MODULE DEVELOPMENT
SPECIFICATION

FOR THE

PROCESSING ELEMENT MODULE

CONTRACT NO.

CDRL SEQUENCE NO.

Prepared for:

RASSP Project
USA

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Initiated by: _____ Date _____

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1 SCOPE

This Module Specification was developed in conjuction with Benchmark 1 of the RASSP program.

1.1 Identification

This specification establishes the performance, design, development, and test requirements for the Processor Element Module of the SAR Signal Processor Configuration Item.

1.2 Configuration Item Overview

The Processor Element Module is a programmable digital signal processing module. It has a RACEway interface to support data transfer and a VME interface for control functions. The primary purpose of the Processor Element Module is to provide a platform for the Data Processing firmware element.

2 APPLICABLE DOCUMENTS

2.1 Government Documents

The following documents of the exact issue shown form a part of this specification to the extent specified herein. In the event of conflict between the documents referenced herein and the contents of the specification, the contents of this specification shall be considered a superseding requirement.

2.1.1 Specifications

At this time the RASSP project is not constrained by any DoD Specifications.

None

2.1.2 Standards

At this time the RASSP project is not constrained by any DoD Standards.

None

2.1.3 Drawings

Not Applicable

None

2.1.4 Other Publications

Not Applicable

None

Copies of specifications, standards, drawings, and publications required by suppliers in connection with specified procurement functions should be obtained from the contracting agency or as directed by the contracting officer.

2.2 Non–Government Documents

The following documents of the exact issue shown form a part of this specification to the extent specified herein. In the event of conflict between the documents referenced herein and the contents of the specification, the contents of this specification shall be considered a superseding requirement.

2.2.1 Specifications

TBD

None

2.2.2 Standards

VITA 5–1994 Rev 1.3	RACEway Intelink – Data Link and Physical Layers	22 June 1994

2.2.3 Drawings

TBD

None

2.2.4 Other Publications

TBD

None

Technical society and technical association specification standards are generally available for reference from libraries. They are also distributed among technical groups and using Federal Agencies.

3 REQUIREMENTS

3.1 Definition

3.1.1 Interface Definition

3.1.1.1 VME Interface

The Data I/O Module shall use the a 32 bit VME bus for control and set–up. This interface shall conform to TBD standard.

3.1.1.2 RACEway Interface

The Processor Element module shall contain a Mercury RACEway interface for access to the processing elements. This interface shall be capable of being either a master or a slave device on the RACEway. This interface shall conform to RACEway Interlink – Data Link and Physical Layers (VITA 5–1994).

3.1.2 Proposed Implementation

The Processor Element Module currently has 4 different proposed implementations. The first 2 implementations a Commercial Off the Shelf (COTS) modules. One is the Mercury MCV6 module which is based on the i860 processor. The second is a Mercury board in development which is based on the ADSP–21060 SHARC processor. Originally a custom ADSP–21060 module was considered but it appeared that the COTS module would be available before development could be completed.

The 2 custom solutions are both based on the Sharp LH9124 digital signal processing chip. The first custom solution uses only one LH9124 chip per module where the second uses two LH9124 chips per module. The LH9124 is a block floating point digital signal processing chip which performs up to TBD MFLOPs.

3.1.3 Connector Definition

3.1.3.1 VME Interface Connector

The VME connector shall have the pin out as shown in Table 3.1.3.1–1.

Table 3.1.3.1–1 VME Connector Pin Out

TBD

3.1.3.2 RACEway Interface Connector

The RACEway Interface pin out shall conform to RACEway Interlink – Data Link and Physical Layers (VITA 5–1994).

3.2 Characteristics

3.2.1 Performance Characteristics

3.2.1.1 Memory

Each Processor Element Module shall contain TBD Mbyte of RAM for firmware executables and data.

Due to the different quantity of modules of the different proposed types, this specification will be varied with the final selected approach. The total memory required is for data is 96 Mbytes. Table 3.2.1.1–1 indicates the minimum ;number of each module type that would be required and the memory available or required per module.

Table 3.2.1.1–1 Processor Element Memory Requirements

Option	Number	Memory/module (Avail)	Total Available
i860	6	16M (32M)	192 Mbyte
ADSP–21060	3	32M (??)	TBD
1–LH9124	3	TBD M** (25M)	TBD
2–LH9124	3	TBD M** (25M)	TBD

** – Since the LH9124 uses block floating point instead of floating point, it requires less memory.

3.2.1.2 Processor

The Processor Element Module must be able to efficiently perform the following types of functions:

a) Complex Vector Multiplication – used to apply weightings
b) DFT/FFT butterflies
c) Indexed Addressing – required to perform a corner turn operations
d) FIR filtering

In addition, it is desirable but not essential that the Processor Element Module be able to perform typical general purpose functions which are typical of microprocessors. These will be used for report generation.

3.2.1.3 Diagnostic Firmware

At a minimum, comprehensive built–in diagnostic capabilities (e.g., power–up memory test) shall be provided with the Processor Element Module. At a minimum, fault isolation must be to the Processor Module level, and preferably beyond. For example, the Processor Element Module must provide firmware capable of verifying the correct operation of the CPU, memory, RACEway interface, and VME interface. The interfaces shall be validated to the level possible without the intervention of outside hardware.

3.2.1.4 Processing Accuracy

The Processing Element Module must perform all operations with IEEE 32 bit Floating Point precision.

Note: analysis is being performed at this time to permit the use of 24 bit Block Floating Point instead.

3.2.1.5 Processing Rate

A full complement of Processor Element Modules must provide a minimum of 740 MOPs. The following table indicates the processing rates associated with each of the option

Table 3.2.1.5–1 Processing Rates

Option	Number	MFLOPs	Total Available
i860	6	TBD	TBD
ADSP–21060	3	320	960
1–LH9124	3	TBD	TBD
2–LH9124	3	TBD	TBD

3.2.1.6 Module Control

The Processor Element Module shall provide memory which addressable from the VME bus to permit the transfer of control and processing information. A minimum of TBD kbytes of VME addressable memory is required for this purpose.

3.2.2 Physical Characteristics

3.2.2.1 Size

The Processor Element Module shall confrom to the VME 6U form factor.

3.2.2.2 Weight

The Processor Element Module shall weigh less than TBD ounces

3.2.2.3 Power

The Processor Element Module shall operate correctly with the following power.

Voltage	5 V +– TBD V
Power	TBD Watts

3.2.3 Reliability

TBD

3.2.4 Maintainability

TBD

3.2.5 Environmental Conditions

TBD

3.2.6 Transportability

TBD

3.3 Design and Construction

TBD

3.4 Documentation

TBD

3.5 Logistics

TBD

3.6 Precedence

In the event of a conflict between the documents referenced in this specification and this specification, the content of this specification shall be considered the superseding requirement.

4 QUALITY ASSURANCE PROVISIONS

4.1 General

4.1.1 Responsibility for Tests

4.1.2 Special Tests and Examinations

4.1.2.1 Subsystem Level Tests

4.1.2.2 Parts Selection Verification

4.2 Quality Performance Tests and Inspections

Quality Conformance Tests or Inspections shall comprise examinations and tests to reveal:

a. Workmanship Problems
b. Omissions and Productions Process Errors
c. Functional and Performance Problems
d. Deviations from Design Requirements
e. Hidden Material Defects

These test or inspections are performed incompliance with the requirements of the configuration item specification.

4.3 Verification Methods

Compliance with the requirements of the configuration item specification shall be verified using the methods indicates in the following verification test matrix table as defined below:

a) Inspection (I) – Physical examination of documentation and hardware to verify conformance to specified requirements. Inspection will check design documentation adequacy to applicable standards. Inspection includes verification by design review and evaluation of the engineering design.

b) Analysis (A) – Use of recognized techniques, including computer models, to interpret or explain equipment performance or test data. Analysis is used in lieu of or to supplement test data. This method also includes analysis to qualify by similarity. This method include review of applicable data on similar equipment and comparing the appropriate characteristics for validation.

c) Demonstration (D) – Verification by operation or adjustment of an item under specific conditions

without recording or data collection. Demonstration is used when quantitative measurement is not required for verification.

d) Test (T) – Collection of testing data using simulation, test equipment, and/or an operational environment. Data are subsequently used to evaluate quantitative product performance and effectiveness characteristics. Evaluation includes comparison of demonstrated characteristics with requirements and any required analysis of the collected data.

4.3.1 Verification Matrix

Requirements Paragraph Number	Requirement Name	Meth-od*	Level**
3.1.1.2	VME Interface	I	Mod
3.1.1.3	RACEway Interface	I	Mod
3.1.3.1	VME Interface Connector	I	Mod
3.1.3.2	RACEway Interface Connector	I	Mod
3.2.1.1	Memory	I	Mod
3.2.1.2	Processor	T	Mod
3.2.1.3	Diagnostic Firmware	T	Mod
3.2.1.4	Processing Accuracy	I	Mod
3.2.1.5	Processing Rate	T	Mod
3.2.1.6	Module Control	I	Mod
3.2.2.1	Size	I	Mod
3.2.2.2	Weight	I	Mod
3.2.2.3	Power	T	Mod

5 PREPARATION FOR DELIVERY

Not Applicable. This module is not an individually deliverable item.

6 NOTES

6.1 Acronyms and Abbreviations

7 UNRESOLVED ISSUES

7.1 Several Possible Solutions

Several alternatives have been identified associated with the Processor Element Module. Each of these alternatives is distinct and has slightly different requirements. This specification must be updated after the final decision is made.

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8 APPENDIX I Traceability Tables

Source Requirement Number	Source Requirement Title	This Specification Requirement Number	This Specification Requirement Title
3.2.1.2.1.a	SOW.a Accuracy	3.2.1.4	Processing Accuracy
3.2.1.2.6	SOW Latency	3.2.1.5	Processing Rate
3.2.2.1	SOW Power Supply	3.2.2.3	Power
3.2.2.2	SOW Size	3.2.2.1	Size
3.2.2.3	SOW Weight	3.2.2.2	Weight
3.2.4.3	SOW Maintenance and Testability	3.2.1.3	Diagnostic Firmware