2

Setup and Synthesis Flow

Learning Objectives

After completing this lab, you should be able to:

- Use the basic features of Design Analyzer
- Use the Designs, Symbol and Schematic Views of Design Analyzer, and select menu, and mouse functions
- Take a design through the basic synthesis steps
- Invoke On-Line Documentation and find `DC` commands in the manual

Lab Duration: 50 minutes

To Get You Started

Match the answers with the following questions.

Questions

1. Why use Design Analyzer instead of the shell interface?
2. What is SOLD?
3. Define synthesis as required for the purpose of this workshop?
4. What DC command performs translation?
5. What DC command performs logic optimization + mapping?
6. What is a DC script file?
7. What does “Synthesis is Path Based” mean?

Answers

A. To see the design’s symbol and schematic view. This is a good interface for debugging purposes or for users with less experience with Synopsys tools.

B. `compile`

C. A sequence of DC commands in a text file. For example, it may contain the constraints and attributes for a design you want to compile.

D. A database, which contains Synopsys manuals, application notes, and manual pages for every DC command plus SOLV-IT articles.

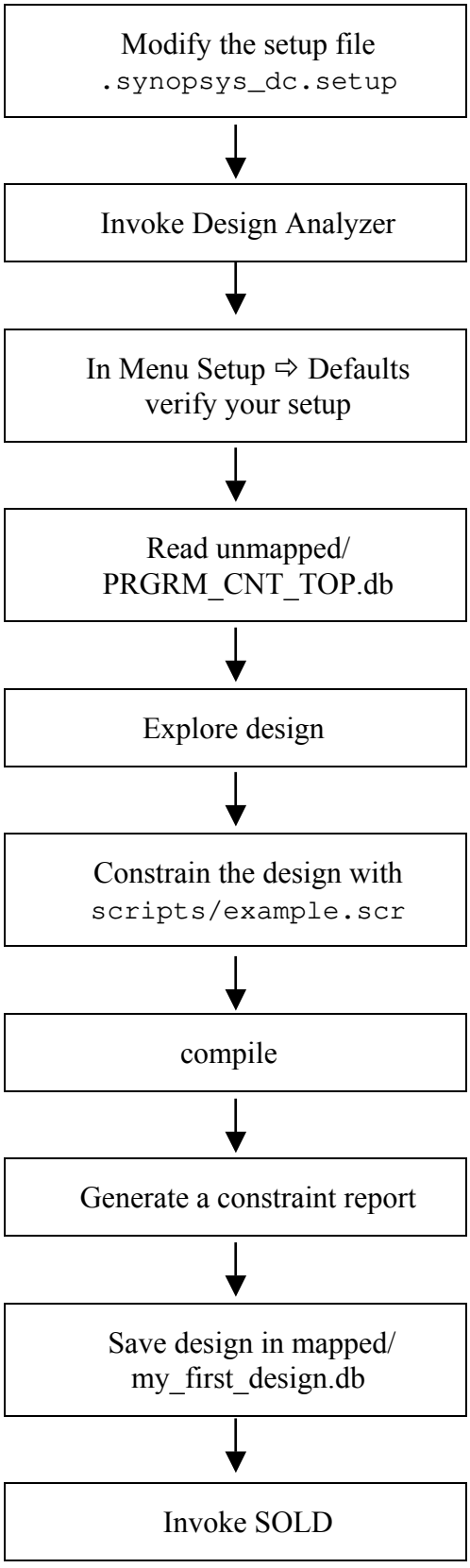
E. `read_vhdl` or `read_verilog`

F. translation + logic optimization + mapping

G. Design Compiler optimizes the timing paths in a design. It does NOT change the register architecture defined by the code.

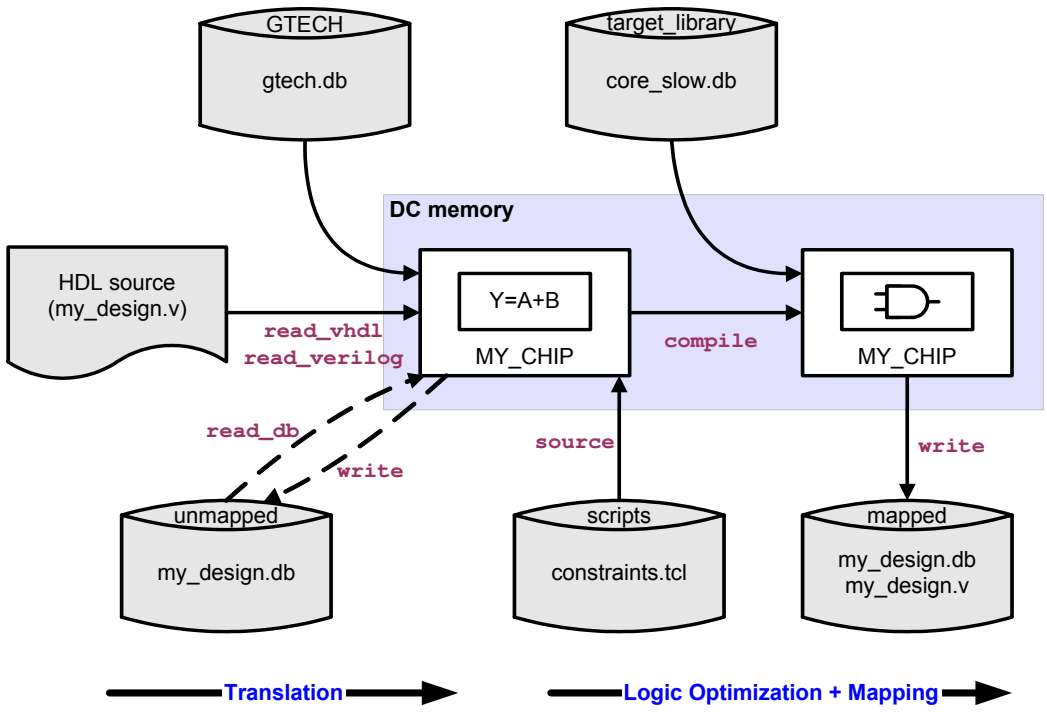
ANSWERS: 1A 2D 3F 4E 5B 6C 7G

Flow Diagram of Lab



Concepts

The following diagram illustrates the flow through Design Compiler:



To read RTL/HDL source code, you use the commands `read_verilog` or `read_vhdl`. The translation process transforms the code into a GTECH netlist (generic technology) using the `gtech.db` library.

After the translation is complete, the design can now be saved to disk in “db” format. The design is now ready to be constrained. This is done by sourcing a constraint file that includes all timing and environmental constraints (input/output delays, loads, transitions, etc).

After the design is constrained, the `compile` command can perform logic optimization, and map the design to the target technology using the library indicated by the `target_library` variable (in our case “core_slow.db”).

After synthesis is complete, the design (gate-level netlist) can be stored to disk using the `write` command. The output format can be a Synopsys binary db file, or a Verilog, VHDL or edif netlist.

Task 1. Create the .synopsys_dc.setup file

1. Make the `risc_design` directory your working directory.

```
UNIX> cd risc_design
```

2. Open the `.synopsys_dc.setup` file with a text editor.

3. **Add** the following lines at the beginning of the `.synopsys_dc.setup` file:

```
#
set target_library "core_slow.db"
set link_library "* core_slow.db"
set symbol_library "core.sdb"
```

The pound sign (#) at the beginning introduces a Tcl script that can be used for Design Analyzer, and dc_shell, as well as for dc_shell-t.

4. **Add** two aliases to the `.synopsys_dc.setup` file:

```
alias rt "report_timing"
alias h "history"
```

These commands are used quite often; creating aliases for them will make your job a little easier. Notice that there are other aliases already defined.

5. **Add** a custom menu item to the `.synopsys_dc.setup` file.

```
set view_script_submenu_items \
  {"Remove All Designs"  "remove_design -designs"}
```

In Design Analyzer, you will now have an option called **Remove All Designs** under the menu **Setup ⇨ Scripts**.

Remove all Designs will erase all designs from Design Analyzer memory (the DC command is `remove_design -designs`).

6. **Save** the `.synopsys_dc.setup` file, and **Quit** the editor.

Task 2. Invoke Design Analyzer

1. Invoke Design Analyzer from the `risc_design` directory.

```
UNIX> cd risc_design
```

or use the `pwd` command to verify you are in the `risc_design` directory.

```
UNIX> design_analyzer &
```

2. Open the Command Window by choosing menu **Setup ⇨ Command Window**.

It is always good practice to begin by opening a Command Window. The window displays all the executed commands, their results, and shows any error messages.

3. Choose menu **Setup ⇨ Defaults** and verify that the libraries are set up correctly.

If the libraries are not correct, ask an instructor for assistance.

Task 3. Read a Design into DC Memory

1. Choose menu **File ⇨ Read**. Double click on directory **`unmapped/`**, and then on `PRGRM_CNT_TOP.db`.

In Design Analyzer, there is now an icon for `PRGRM_CNT_TOP`, which is the top-level of a hierarchical design. There are also icons for the lower-level modules: `PRGRM_FSM`, `PRGRM_DECODE`, and `PRGRM_CNT`.

The** Designs View **does not display hierarchy - it simply displays an icon for each design in Design Compiler memory.

Task 4. Explore the Designs-, Symbol-, and Schematic-View

1. Explore the **Designs View** by observing all the blocks.

Look at the lower right corner to verify you are in the Designs View. Select `PRGRM_CNT_TOP` (single click via the left mouse button), and look at the lower left corner to verify the selection.

2. Go to the **Symbol View** by double clicking on `PRGRM_CNT_TOP` or clicking the down arrow on the left side of Design Analyzer.

If you do not see one (and only one) block, labeled **`PRGRM_CNT_TOP`**, you are in **Schematic View** instead of the **Symbol View**. If this happens, click the rectangular Symbol icon on the left side of Design Analyzer.

Look at the lower right corner of Design Analyzer to verify you are in Symbol View.

3. Go to the **Schematic View** by double clicking on `PRGRM_CNT_TOP` or clicking the AND symbol button on the left side of Design Analyzer.

The schematic of `PRGRM_CNT_TOP` contains instantiations of `PRGRM_FSM`, `PRGRM_DECODE` and `PRGRM_CNT`. This is the "block diagram" of `PRGRM_CNT_TOP`.

4. Explore `PRGRM_CNT_TOP` by visiting the **Symbol** and **Schematic Views** of `PRGRM_DECODE`, `PRGRM_FSM`, and `PRGRM_CNT`.

Because you have not compiled these designs yet, you will not see gates from the target technology library. You will see GTECH components. GTECH components are generic Boolean gates and registers that represent the functionality of a design.

Red boxes are DesignWare components. DesignWare will be discussed in lecture.

Task 5. Explore the Mouse Functions

1. **Click and hold** the **right mouse button** to see the available mouse functions.

2. Choose **Zoom (**while holding down the right mouse button). With the left mouse button, click and drag on the area you want to zoom into. Return to the **Full View** by using the appropriate mouse function.

3. Go to the Schematic View of `PRGRM_DECODE`.

   Note that the **Current Design** in the left corner of Design Analyzer shows `PRGRM_CNT_TOP` but the **Current Instance** shows `I_PRGRM_DECODE`.

4. To select multiple objects, experiment with using your **middle mouse button**. Use the left mouse button to select the first object, then the middle button to select additional objects. *Selected objects appear to be drawn with dashed lines or surrounded by a dashed box.*

Perform Basic Steps in Synthesis Flow

Recall that the steps are:

- Translate HDL code.

  This is normally done via `read_vhdl/read_verilog`. For this lab, `read_vhdl/verilog` has already been done, and the results were saved in the `unmapped/` directory.

  The translated design `unmapped/PRGRM_CNT_TOP.db` has been read into memory.

- Constrain the design
- `compile`
- Generate reports
- Save the resulting netlist

Task 6. Constrain PRGRM_CNT_TOP with a Script file

1. Go to the **Symbol View** for `PRGRM_CNT_TOP`.

You may also be in Schematic View, however, Symbol View gives you a good overview of your port names.

2. Choose menu **Setup ⇨ Execute Script**.

3. Double click on the *scripts* directory, and then `example.scr`.

This will execute a script file, which constrains the Program Counter design.

Task 7. Map the Program Counter to Vendor-Specific Gates

1. Choose menu Tools ⇨ Design Optimization.

2. Click `OK` to start the optimization and mapping process.

This executes the `compile` command. A Compile Log window appears showing the progress of `compile`. This table will be discussed later.

3. Cancel the Compile Log window when the compile is complete.

4. Explore the **Schematic View** of `PRGRM_DECODE`, `PRGRM_FSM` and `PRGRM_CNT`.

You will now see gates from the target technology library (`core_slow.db`).

Task 8. Generate a report to see if Design Compiler was able to meet the Timing Constraints

1. Go to the **Symbol View** of `PRGRM_CNT_TOP`.

2. In the Command Window, type `rc`

   The `rc` command is an alias that was specified in the `.synopsys_dc.setup` file. It executes the following command:

   ```
   report_constraint -all_violators
   ```

   A report will be generated, showing any data paths containing timing constraint violations.

   Record the following information:

   Max Delay: Largest Violation _____

3. Go back to the **Schematic View** of `PRGRM_CNT_TOP`.

4. Choose menu **Analysis ⇨ Highlight ⇨ Critical Path** (CTRL-T).

   The critical path, (the path with the largest violation), will be highlighted. Push into the hierarchy to see which gates are contained in this path.

   To undo the highlighting, select:

   Analysis ⇨ Highlight ⇨ Clear (CTRL-H).

Task 9. Save the Optimized Design

1. Go back to the Symbol View of `PRGRM_CNT_TOP`.

2. Choose menu **File ⇨ Save As.**

3. Double click on the ***mapped*** directory.

4. Verify that the Save **All Designs in Hierarchy** button is selected. This ensures that the entire design hierarchy, not just the top-level design, is saved.

5. Enter `my_first_design.db` in the File Name field.

6. Click **OK.**

   You just saved the gate-level netlist (the entire hierarchy) in 'db' format under the `mapped` directory. Verify the file was created from a UNIX window, using the '`ls -l`' command.

Task 10. Remove Designs from Design Compiler Memory

1. Choose menu **Setup ⇨ Scripts ⇨ Remove all Designs**. Verify that all the icons in Design Analyzer have been deleted.

   This menu executes the following command:

```
remove_design -design
```

   If the custom menu item did not work, ask your instructor to help you debug the problem.

   You could also use a graphical approach, by performing these steps:

   - **Select all** designs from the **Designs View** (use the left mouse button to draw a box around all the icons) you want to delete.
   - Choose menu **Edit ⇨ Delete**.

   This removes the selected designs from Design Analyzer memory.

2. In the Command Window, type **`h`.**

   This should show a history of all commands you have executed since you started Design Analyzer.

Task 11. Invoke On-Line Documentation

1. Choose menu **Help ⇨ On-Line** Documentation.

2. Select Synthesis Tools.

   This opens a new file in the Acrobat reader. From this file, you can access any manual for any Synopsys Synthesis Tool. Go directly to a manual by clicking on the appropriate title from the main window.

You may also invoke On-Line Documentation from a UNIX shell. Type:

```
acroread $SYNOPSYS/doc/online/top.pdf &
```

The $SYNOPSYS environment variable should point to the tool installation directory. If it does not, `ask` your instructor for help.

3. Use On-Line Documentation to find the variable that sets the file name to which a log of the commands executed in a DC shell or Design Analyzer session is written.

4. Look up a manual page on `view_command_log_file`. What is the difference between the contents of this file and that of the `command_log_file`?

5. Choose **File ⇨ Exit** (in the On-Line Docs window) when finished.

6. Choose **Help ⇨ Commands.**

Enter a command or variable for a manual page. Try `current_design`, or perhaps `compile`.

7. Click cancel when you are done.

Lab Review Questions

The answers can be found at the end of this lab.

Question 1. How do you select multiple objects in Design Analyzer?

.....

Question 2. What functions are available using your right mouse button?

.....

Question 3. Numerically order the following steps to show the basic synthesis flow:

A. Compile ..... _____
B. Read in the unmapped design ..... _____
C. Generate a constraint report ..... _____
D. Apply a constraint script file ..... _____
E. Save the mapped design ..... _____
F. Determine if constraints are met ..... _____
G. Set up library variables ..... _____

Question 4. How do you optimize and map a design with Design Analyzer?

.....

Question 5. Which Design Analyzer menu item saves a design?

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Question 6. What are the benefits of using synthesis in a design flow?

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Question 7. What is the difference between Design Analyzer and `dc_shell`?

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Question 8. Why should you create a `.synopsys_dc.setup` file?

.....

Question 9. How do you verify the library variables are set up correctly?

.....

Question 10. How do you "read" VHDL or Verilog code into Design Analyzer?

.....

Question 11. What are two optimization goals you can set on a design?

.....

Question 12. What is the function of the `target_library` variable?

.....

Answers / Solutions

Question 1. How do you select multiple objects in Design Analyzer?

Use the middle mouse button to select multiple objects, or use the left mouse button to draw a box around adjacent objects.

Question 2. What functions are available using your right mouse button?

Zoom (in conjunction with Full View) and Push to Reference (in conjunction with Pop to Instance).

Question 3. Numerically order the following steps to show the basic synthesis flow:

A. Compile	4
B. Read in the unmapped design	2
C. Generate a constraint report	5
D. Apply a constraint script file	3
E. Save the mapped design	7
F. Determine if constraints are met	6
G. Set up library variables	1

Question 4. How do you optimize and map a design with Design Analyzer?

Go to the Symbol or Schematic View of the design you wish to compile. Choose **Tools ⇨ Design Optimization.**

Question 5. Which Design Analyzer menu item saves a design?

Go to the Symbol View of the design you want to save. Choose **File ⇨ Save As**. Enter the file name. **Make sure that the Save All Designs in Hierarchy button is selected.**

Question 6. What are the benefits of using synthesis in a design flow?

Synthesis moves the designer to a higher level of abstraction. Synthesis can speed up the design process.

Question 7. What is the difference between Design Analyzer and `dc_shell`?

Design Analyzer is the GUI to the Synopsys synthesis tools. `dc_shell` or `dc_shell-t` is the command line interface.

Question 8. Why should you create a `.synopsys_dc.setup` file?

The `.synopsys_dc.setup` file is a script file, which is executed upon invocation of either Design Analyzer or `dc_shell-t`. It is a useful file for commands that are to be executed each time DC is invoked. For example, it is useful to initialize library variables in this file.

Question 9. How do you verify the library variables are set up correctly?

Choose menu **Setup ⇨ Defaults** in Design Analyzer.

Question 10. How do you "read" VHDL or Verilog code into Design Analyzer?

Choose menu **File ⇨ Read** in Design Analyzer.

Question 11. What are two optimization goals you can set on a design?

Timing and Area.

Question 12. What is the function of the `target_library` variable?

The `target_library` variable defines the technology library used during compile mapping phase.