Project Monitor Form

Project: CMS FED **Date:** Thursday 20-December-2001	**PMF number: 02** **Sheet:** 1 **of** 2

News and comment
Feasibility Study continues

Planning:
John has produced a draft of the Project Specification and the FED 9U prototype costings. He will pass both to Rob for approval before distributing them to the customer for the next customer meeting (provisionally on 11th January).

Front End Module:
No progress to report on Front-End Module overview. DO effort is occupied with migrating old CADENCE designs before year's end.

CERN has sent us the latest Opto-Receiver spec including a provisional pin out. We still have the opportunity (but only for a few weeks) to give feedback on our preferred pin out.

James is again experiencing problems with the preferred simulation tools (ie AWB tools compatible with PCB design flow). He has been unable to attach simulation models to his own generated symbols. He has consulted other users and experts but no one seems to have a fix for these problems yet.

Firmware:
Ed has started to use the Virtex II 40K development board. He has only been able to download designs using Rob's laptop. The provided test designs function, but the clock delay test design does not yet work

Other Issues:
A concern was raised regarding the assignment of staff effort currently being used on another project being put on the CMS project code.

Actions from the previous PMF

Action	Status	Who	Target date
Develop draft Project Spec	Done	JC	
Develop draft schedule	In progress	JC	xx-01-02
Pass schematic for Analogue part of Front End module to DO	Ongoing	JS/CD	17-12-01
Check Impact Memec if Cadence Xilinx footprints/symbols exist on Xilinx Web site	Ongoing	RH	17-12-01
Organise hand over meeting for Back End FPGA	Ongoing	RH	19-12-01
Organise a Board Level Design Meeting	Ongoing	RH	20-12-01

Test key aspect of Delay FPGA on development board in Lab	In progress	EF/RH	31-01-02

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Approve draft Project Spec & FED prototype costings before customer meeting.	RH	10-01-02
Develop draft schedule	JC	14-01-02
Produce procurement list for 9U Prototype	JC	14-01-02
Pass schematic for Analogue part of Front End module to DO	JS/CD	14-01-02
Check Impact Memec if Cadence Xilinx footprints/symbols exist on Xilinx Web site	RH	14-01-02
Organise hand over meeting for Back End FPGA	RH	14-01-02
Organise a Board Level Design Meeting	RH	14-01-02
Test key aspect of Delay FPGA on development board in Lab	EF/RH	31-01-02

Project Monitor Form- milestones

Project: CMS FED **Project Manager:** R. Halsall **Date:** Thursday 20-December-2001		**PMF number: 02** **Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**: 0.1**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30-07-01		26-09-01
2	Project Spec sign off	21-12-01	31-01-02	
3	Board Level Preliminary Review	14-01-02	14-01-02	
4	FE Analogue Channel Feasibility Review	31-01-02	31-01-02	
5	FE Module Feasibility Review	28-02-02	28-02-02	
7	Board Level Feasibility Review	04-03-02	04-03-02	
8	Delay FPGA Feasibility Review	31-01-02	31-01-02	
9	Front End FPGA Feasibility Review	31-01-02	31-01-02	
10	Back End FPGA Feasibility Review	31-01-02	31-01-02	
11	VME FPGA Feasibility Review	28-02-02	28-02-02	
12	Clock FPGA Feasibility Review	28-02-02	28-02-02	
13	Release Test Plan Document	22-02-02	22-02-02	