HOW TO BUILD AN SOI COMPACT MODEL WITHOUT VIOLATING THE LAWS OF PHYSICS

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ABSTRACT

An important application for partially depleted SOI is high performance microprocessors and other logic chips. In order to deliver market leading performance it is necessary for transistor design and circuit design to be done concurrently. The circuit design process requires a compact model that describes in detail the electrical characteristics of transistors that do not yet exist.

Our approach to building such models starts with an existing model that accurately describe a real physical transistor. This model is modified to match key parametric and performance targets for the new transistor. This paper describes a set of physical relationships that can be checked during construction of an SOI compact model to improve the accuracy of the model.

Keywords: Compact Model, SOI, Concurrent Design

INTRODUCTION

For circuit design to begin before transistor design is complete the modeling engineer must somehow estimate the characteristics of the transistors the will ultimately be used to build the circuit. [1] One approach is to use a finite element (TCAD) simulation of the intended transistors to create simulated transistor data. Our experience with this approach has been very unsatisfactory because of the difficulty in getting sufficiently consistent results across multiple transistor geometries especially in trying to estimate narrow channel effects.

Another approach is to use a compact model equation set which captures the necessary physics in sufficient detail to allow creation of models from the intended physical process parameters. The problem with this approach is that many of the important physical effects cannot be calculated from first principles.

A problem for both of these approaches is that a process that actually produces the desired transistors has not yet been found so not all of the inputs to either a TCAD simulation or a theoretically based compact model are available.

Several other sources of information are available to for completing the compact model. One is hardware and a model from a previous generation of transistors. Another is experimental hardware that has been built to explore the design space for the new transistors. There are probably working transistors with the correct oxide and silicon thickness but they are probably not the ones with the correct threshold voltage. A final source of information is the transistor design goals the device engineer is working toward. These might include ring oscillator delay, desired threshold voltage and maximum off current.

We drawn on all these sources of information to compile a list of transistor specifications or targets comprising the information listed in table I. We use the BSIMPD model formulation from UC Berkeley [2] which incorporates a great deal of physics in the model equations. This helps to ensure that the design targets are connected by physically reasonable curves. Finally we apply a series of test to both the transistors targets and the resulting models to detect unphysical effects before the model is released.

BODY CURRENT CHECKS

At many bias conditions the body voltage is determined primarily by the balance of reverse diode leakage across the drain to body junction and forward diode current across the source to body junction. It may be possible to fit diode currents to silicon even if FET characteristics are far from the desired targets. Otherwise diode currents can be estimated based anticipated doping and previous silicon.

A curve of body voltage vs. drain voltage without any gate or impact ionization current is a useful check on the consistency of the forward and reverse currents. For very low drain bias the body bias should be half the drain bias. ($V_{bs}=V_{ds}/2$) As the drain bias increases the body bias increase should slow as the body to source diode turns on and clamps the body voltage. Fig. 1 shows such curves for three different diode models plus a reference line of $V_{bs}=V_{ds}/2$. Diode 3 is not a physically reasonable diode because reverse current is stronger that forward current at low bias pushing the curve above the reference line. Diodes 1 and 2 are both possible. Diode 1 is dominated at low bias by diffusion current which has a steeper slope than recombination current which dominates diode 2 at low bias.

Turning on the gate tunneling current (without impact ionization) splits this curve into a family of curves. As shown in fig. 2 at high drain bias the reverse diode current dominates and the curves for all gate biases overlay. At lower drain bias the gate tunneling current is greater than

the reverse diode current and pulls the body potential up until diode forward current matches the tunneling current. Because the diode and tunneling currents are physically determined by different factors many such curves are possible. Noting at what drain and gate bias the tunneling and diode currents are comparable indicates whether or not these currents have the intended balance.

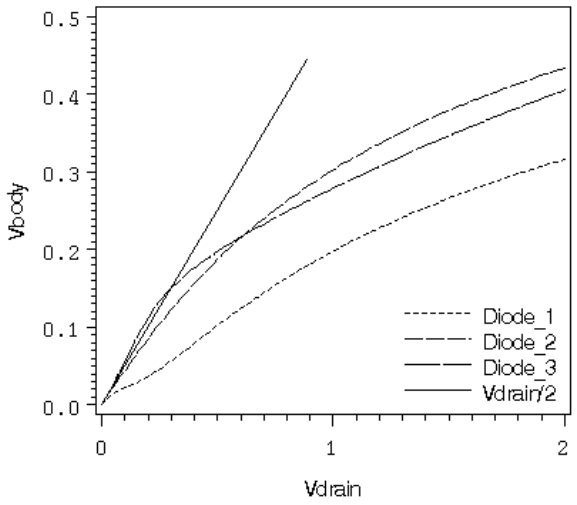

Fig.1 Body voltage resulting from diode currents only. Diode 1 is unphysical

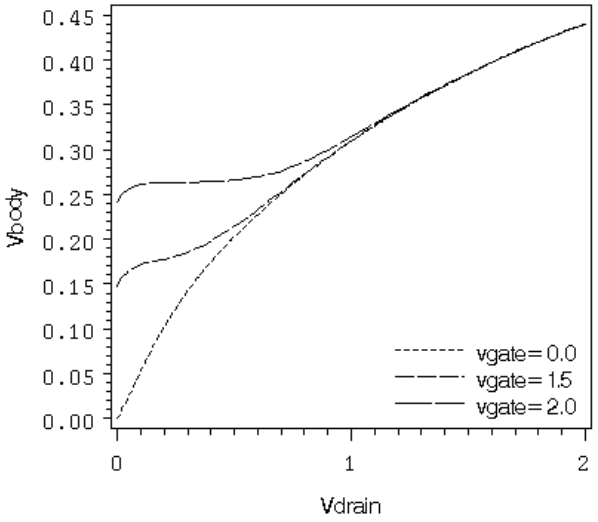

Fig. 2 Body voltage from balance of gate and diode currents

Fig. 3 shows the interaction of diode currents with impact ionization currents a various gate biases. The kink in body voltage seen here leads directly to the well known kink effect in the IdVd curves. The set of curves in fig 3 passes the sanity checks we apply here. First at low drain bias impact ionization is too small to effect the body voltage. Second at high drain bias the impact ionization dominates over drain to body diode leakage. And finally the largest impact ionization effect is with an intermediate gate bias, not with the highest gate bias which gives the largest drain current. Unlike diode and gate current impact ionization current changes greatly as drain current model is changed. For this reason these checks need to be made before, during and after drain current fitting.

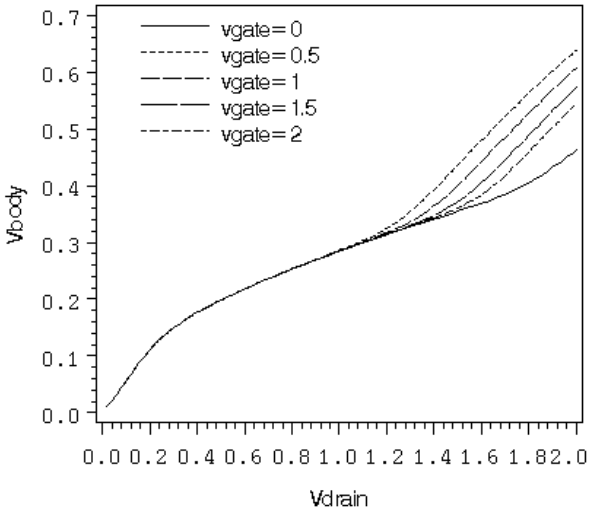

Fig 3. Body voltage from balance of impact ionization and diode currents

DRAIN CURRENT TARGET CHECKS

Table I shows a typical set transistor parameters for which targets are established to define the current-voltage characteristics as a function of length. Some of these parameters will be readily available because they have already been established by the device designer. Others will have to be estimated from early silicon and previous generation models, silicon or experience. Before attempting to build a model the targets are checked for physical consistency.

Ioff and Vt are connected by the sub threshold slope. Because we use a single point definition of Vt we can calculate sub threshold slope as:

$$S = \frac{V_t}{\log(I_{Vt}/I_{off})}$$

The minimum value for subthreshold slope (S) is approximately 60 mV/decade at 25C (ln(2)kT) for a bulk FET. In a floating body transistor S can be steeper than this because as Vgs increases, drain current and therefore impact ionization current increases. This causes the body to float up reducing Vt and increasing drain current. [3] In practice a partially depleted SOI MOSFET designed for high performance logic will have it's sub threshold slope

degraded by drain induced barrier lowering and capacitive coupling of the channel to the body. Targets that require a sub threshold slope steeper than about 70 mV/decade or shallower than 110 mV/decade are probably not realistic.

If both Ioff and Vt are specified at more than one channel length the indicated sub threshold slopes should be consistent. If Vt is nearly the same at both lengths then S should also be similar. If the shorter channel has significant roll off of Vt then it should also have a shallower slope because both effects are caused by increased control of the channel charge by the source and drain.

Similarly the subthreshold slope at various widths or temperatures should be consistent. Our experience with shallow trench isolated SOI is that subthreshold slope is nearly constant down to very narrow devices although Vt can change significantly.

The variation of on current from nominal to minimum length should also be checked for reasonable behavior. Classically saturated current is proportional to overdrive squared and inversely proportional to channel length. However this relation assumes that saturation starts when the pinch off occurs at the drain end of the channel which is controlled by channel charge and mobility. In deep sub-micron NFETs, both SOI and bulk, saturation is primarily due to velocity saturation and current is approximately proportional to overdrive to the first power. For PFETs the hole mobility is lower and the behavior is a mix of both. Using the linear relationship leads to the following expected ratio of Ion at L=nominal and L=minimum:

$$\frac{I_{ON}(L_{MIN})}{I_{ON}(L_{NOM})} = \frac{(V_{dd}-V_T(L_{MIN}))\cdot L_{NOM}}{(V_{dd}-V_T(L_{NOM}))\cdot L_{MIN}}$$

This is generally an upper limit for both NFETs and PFETs because heavy pocket implants and series resistance degrade device currents on shorter devices.

In the deep sub micron regime really narrow devices show some rather strange behavior due to lithographic effects, dopant redistribution with the isolation and mechanical stress. None the less it is useful to apply the same simple model to determine the ratio of the transistor gains between the narrow and wide devices:

$$\frac{\beta_{Narrow}}{\beta_{Wide}} = \frac{I_{Narrow}W_{Wide}(Vdd-V_{TWide})}{I_{Wide}W_{Narrow}(Vdd-V_{TNarrow})}$$

Ideally this ratio would be one. In practice a value less than 0.9 or greater than 1.1 suggests the narrow device targets may not be reasonable.

DRAIN CURRENT MODEL CHECKS

Once a model has been constructed that meets the transistor targets it is checked for various unphysical behaviors. A test for negative g_m, g_{mbs} and g_{ds} is performed at biases up to three times the normal operating voltage. It should be noted that very long channel MOSFETs with thin gate oxide can show negative g_m at low drain and high gate bias. This is due to gate tunneling current to the channel canceling a part of the channel current that would otherwise be measured at the drain.

Another physical effect seen in g_m measurements of SOI devices is shown in fig. 4. The second peak in g_m vs. Vgate (solid curve) is created when the current from the gate to the body becomes large enough to raise the body voltage (dashed curve) and reduce the threshold voltage.

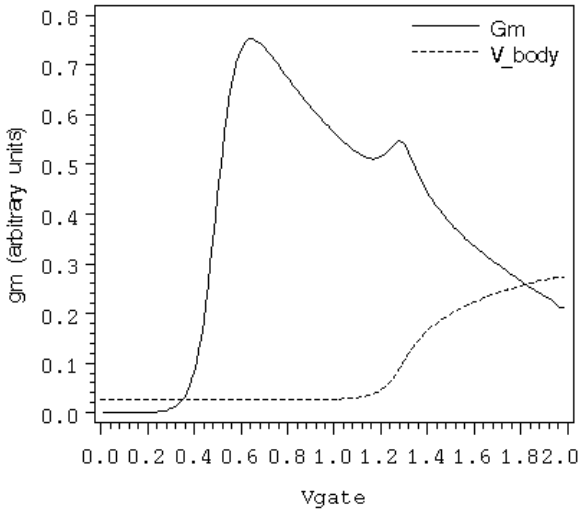

Fig. 4 The effect of gate current on transconductance

A second set of checks involves plotting drain current and threshold voltage against channel length, channel width and temperature. The currents used are Ion, Ioff and linear current and the threshold voltages Vds=.05 and Vds=Vdd. Fig. 5 is an example where the model was adjusted trying to achieve a Ion/W (dashed curve) flat with W; Ioff/W (solid curve) drop significantly lower at narrow W and Vt rolling up significantly at narrow W. We believe the these targets are physically reasonable; Vt is driven by dopant effects and Ioff follows from Vt. For Ion the Vt effect is countered by the change in mobility at narrow channels. [4] At minimum W the model matches the targets but the intermediate W region is not well behaved. To minimize such problems our fitting methodology tries to keep currents and threshold voltages monotonic with W during the fitting.

Fig. 6 shows Ion, Ioff and Vt vs. channel length. In this case the bumps in Vt and Ioff are physically real. The rise in Vt with channel length is due to strong pocket implants near the source and drain and the sudden drop at short channel is due to the normal short channel effect and drain induced barrier lowering. Because off current depends exponentially on Vt it shows a corresponding dip while on

current responds linearly to Vt but is more sensitive to L and therefore increases monotonically as length decreases.

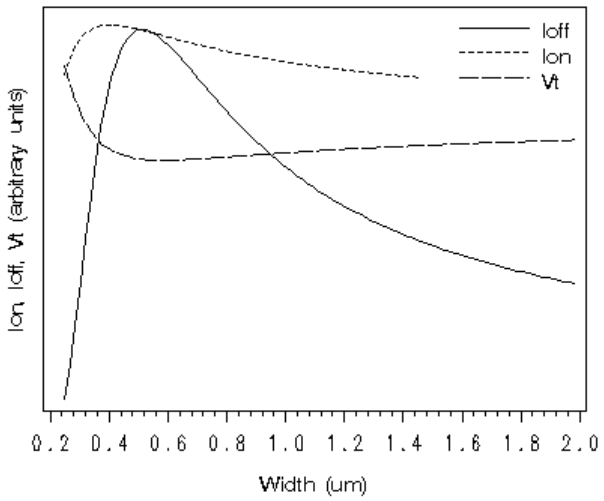

Fig. 5 Example of unphysical width scaling.

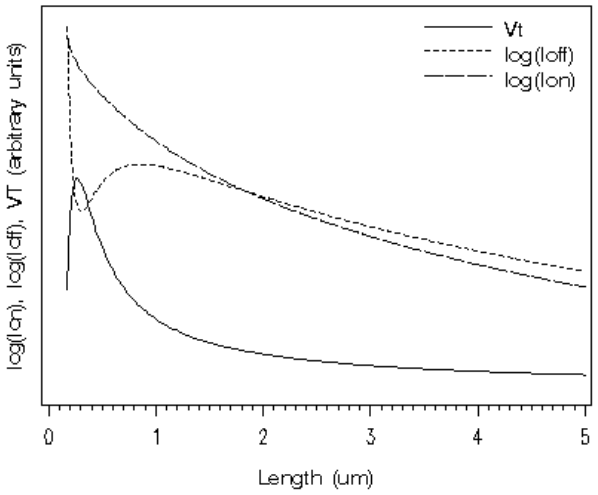

Fig. 6 Non momotonic Ioff vs. L is physically real.

CONCLUSION

We have presented our procedure for creating compact models of SOI MOSFETs for circuit design concurrent with transistor design. By describing the technology in terms of a set of transistor targets we are able compile a description using information from all the available source, preliminary silicon, previous generation silicon and requirements from the circuit designers. By applying physics based tests to both the targets and the resulting models we ensure the model is physically reasonable. This method allows circuit design to proceed with a high quality model for transistors which have not yet been produced.

Table 1: Transistor characteristics estimated for a model

General
Vdd -- Nominal operating voltage
Delta L
Delta L tolerance
Delta W
Tox - physical
Tox - electrical
Body Currents
Diode forward current
Diode reverse current
Peak Impact Ionization current (as a fraction of drain current)
Gate tunneling current - inversion
Gate tunneling current - accumulation
Threshold voltages
Linear and Saturated Vt L=long
Linear and Saturated Vt L=nominal
Linear and Saturated Vt L=minimum
Body Effect L=nominal
Temperature Sensitivity of Vt (mV/C)
Drain Currents
Ion L=nominal
Ion L=minimum
Ioff L=minimum
Linear current L=nominal
Linear current L=minimum
Switching current L=nominal
Temperature Sensitivity of Ion
Temperature Sensitivity of Linear Current
Temperature Sensitivity of Ioff
Width Effects (delta from W=wide to W=minimum
Linear Vt
Saturated Vt
Ion
Ioff

.REFERENCES

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[3] Preter, J., et.al., Proceedings of the 2001 International SOI Conference, P25-26, 2001

[4] Hook, T.J., IEEE Electron Device Lett. Vol.21, No.2 P85-7, 2000