IT-SoC Lab

Introduction to SOPC Builder

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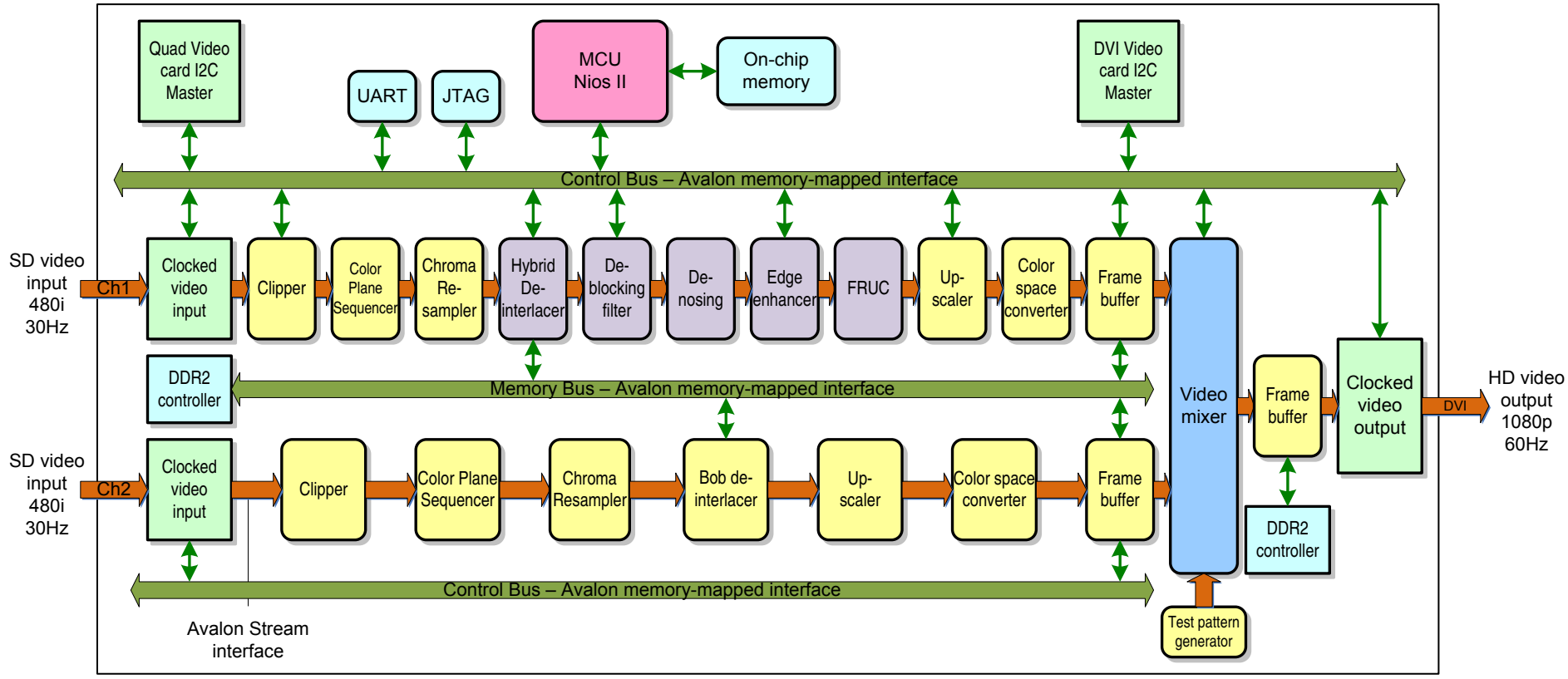
- **Class content**
  - SOPC VDP system block diagram
- **Required documents**
  - SOPC Builder User Guide (http://www.altera.com/literature/ug/ug_sopc_builder.pdf)
- **Class time**
  - 1 hours
- **Assignments**
  - 10 questions

Feature	Detail	Explain
Device	Cyclone III EP3C120	
Processor	Nios II	
Video processing	-Deblocking -Deinterlacing -Denoising -Scaling -Frame rate up-converting	Perform 5 video processing functions
Interface	-S-video input -DVI output	SD video input Full HD video output
Bus system	-Avalon-MM -Avalon-ST	Interface between components
Memory	-DDR2 SDRAM	To store video frames
Operating clock	134 MHz	For processing 1920x1080@59 video


Quad Video card I2C Master
UART
JTAG
MCU Nios II
On-chip memory
DVI Video card I2C Master
Control Bus – Avalon memory-mapped interface
SD video input 480i 30Hz
Ch1
Clocked video input
Clipper
Color Plane Sequencer
Chroma Re-sampler
Hybrid De-interlacer
De-blocking filter
De-nosing
Edge enhancer
FRUC
Up-scaler
Color space converter
Frame buffer
DDR2 controller
Memory Bus – Avalon memory-mapped interface
SD video input 480i 30Hz
Ch2
Clocked video input
Clipper
Color Plane Sequencer
Chroma Resampler
Bob de-interlacer
Up-scaler
Color space converter
Frame buffer
Video mixer
Frame buffer
DDR2 controller
Clocked video output
DVI
HD video output 1080p 60Hz
Control Bus – Avalon memory-mapped interface
Test pattern generator
Avalon Stream interface

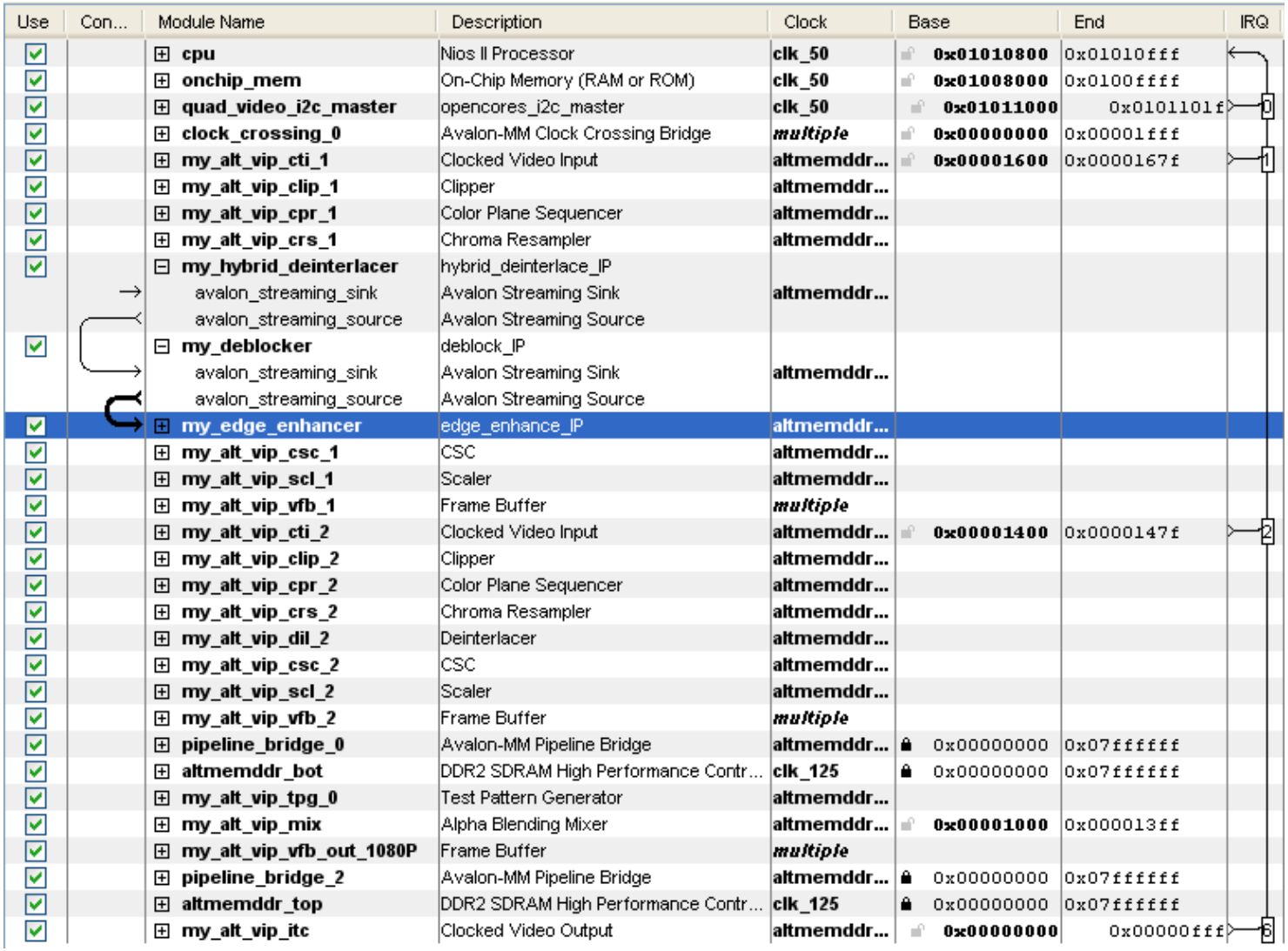
Part	Task	Timing (max. limitation)	Area (max. limitation)
Data processing channel 1	Clipper	7.4 ns (134MHz)	0.5 K logic cells
	Color plane sequencer	7.4 ns (134MHz)	0.5K logic cells
	Color resampling	7.4 ns (134MHz)	2 K logic cells
	Color converting	7.4 ns (134MHz)	1 K logic cells
	Hybrid deinterlacing	7.4 ns (134MHz)	15 K logic cells
	Deblocking	7.4 ns (134MHz)	20 K logic cells
	Scaling	7.4 ns (134MHz)	5 K logic cells
	Edge enhancing	7.4 ns (134MHz)	10 K logic cells
	Frame buffer	7.4 ns (134MHz)	3 K logic cells
Data processing channel 2	Clipper	7.4 ns (134MHz)	0.5 K logic cells
	Color plane sequencer	7.4 ns (134MHz)	0.5K logic cells
	Color resampling	7.4 ns (134MHz)	2 K logic cells
	Color converting	7.4 ns (134MHz)	1 K logic cells
	Bob Deinterlacing	7.4 ns (134MHz)	2 K logic cells
	Scaling	7.4 ns (134MHz)	5 K logic cells
	Frame buffer	7.4 ns (134MHz)	3 K logic cells

Interface and control	Test pattern generator	7.4 ns (134MHz)	0.2 K logic cells
	Mixer	7.4 ns (134MHz)	2 K logic cells
	Clock video input	7.4 ns (134MHz)	1 K logic cells
	Clock video output	7.4 ns (134MHz)	1 K logic cells
	Memory control	6 ns (166MHz)	5 K logic cells
	Quad video card control	20 ns (50MHz)	0.2 K logic cells
	DVI video card control	20 ns (50MHz)	0.2 K logic cells
	JTAG_UART control	20 ns (50MHz)	2 K logic cells
CPU	NIOS II	20 ns (50MHz)	3K logic cells
	Data master arbitrator	20 ns (50MHz)	0.2 K logic cells
	Instruction master arbitrator	20 ns (50MHz)	0.2 K logic cells
All system	Instruction master arbitrator	20 ns (50MHz)	86 K logic cells

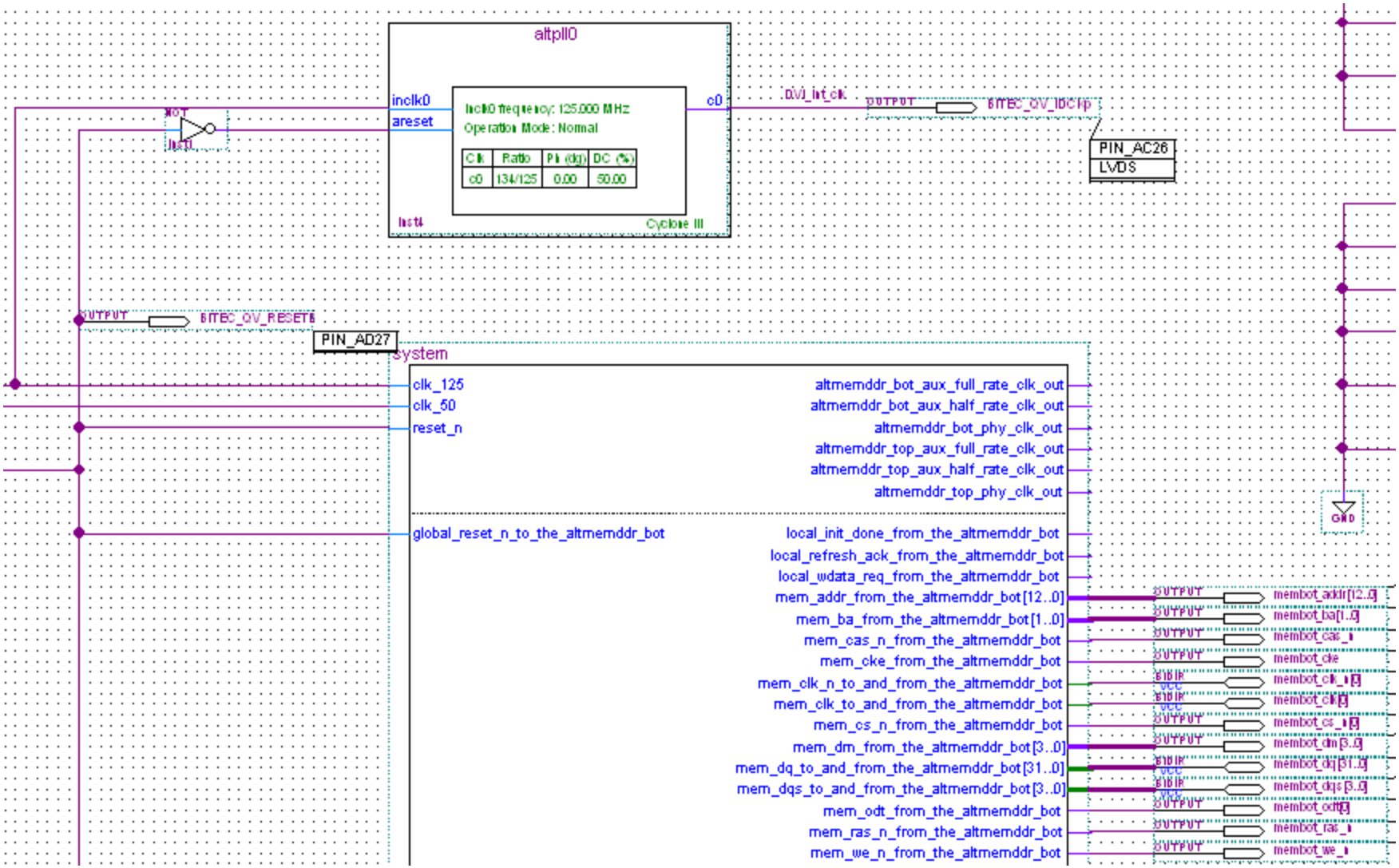
Global partitioning	Data processing part	Required performance
Data processing part	Color resampling	Strict real-time
	Color space converting	Strict real-time
	Clipper	Strict real-time
	Deblocking	Strict real-time
	Deinterlacing	Strict real-time
	Denoising	Strict real-time
	FRUC	Strict real-time
	Upscaling	Strict real-time
	Edge enhancing	Strict real-time
	Video mixer	Strict real-time
Application part	S-video card control	None strict real-time
	DVI card control	None strict real-time
	Video input control	None strict real-time
	Video output control	None strict real-time
	Video function control	None strict real-time
	Video channel control	None strict real-time
	Video resolution control	None strict real-time
	Frame buffer control	None strict real-time

Hardware partition	Software partition
Data processing: -Color resampling -Color space converting -Clipper -Deblocking -Denoising -Deinterlacing -FRUC -Upscaling -Edge enhancing -Video mixer Video interface: -Clocked video input -Clock video output -IO interface	-S-video card control -DVI card control -Video input control -Video output control -Video function control -Video channel control -Video resolution control -Frame buffer control

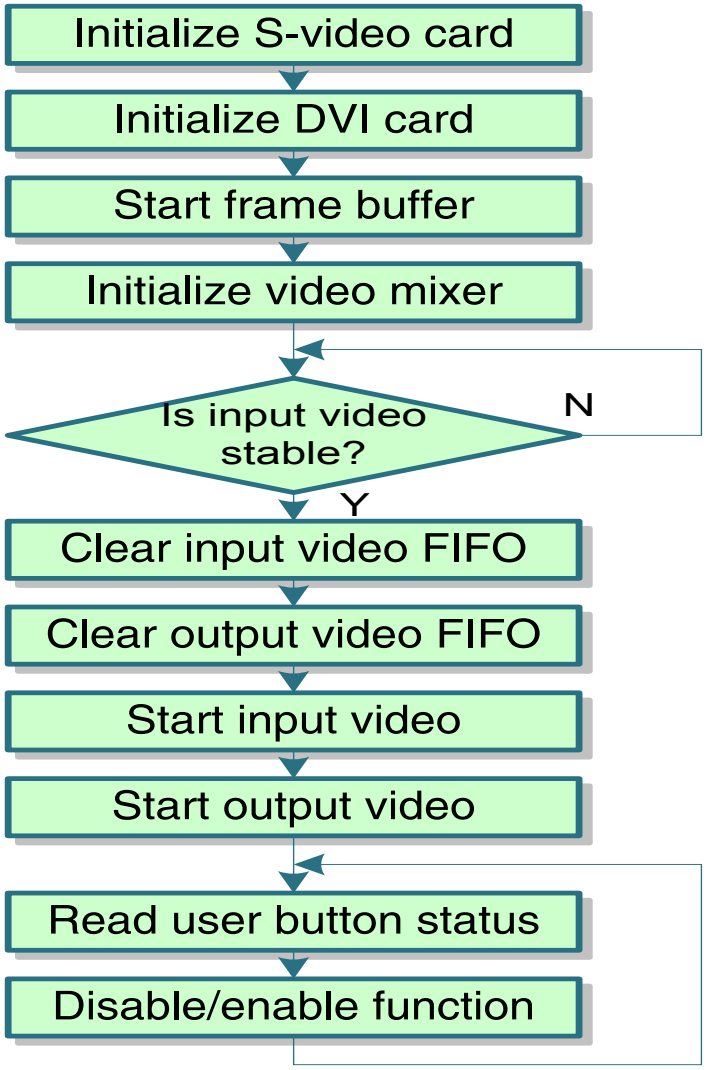
Group	Component name	Source
IO and memory controlling	Quad video I2C master	Bitec Ltd.
	DVI video I2C master	Bitec Ltd.
	Clocked video input controller	Altera library
	Clocked video output controller	Altera library
	DDR2 SDRAM controller	Altera library
Video processing	Clipper	Altera library
	Color plane sequencer	Altera library
	Chroma resampler	Altera library
	Color space converter	Altera library
	Frame buffer	Altera library
	Up-scaler	Altera library
	Video mixer	Altera library
	Deblocking filter	Designed in the project
	Hybrid deinterlacer	Designed in the project
	Denoiser	Designed in the project
	FRUC	Designed in the project
	Edge enhancer	Designed in the project

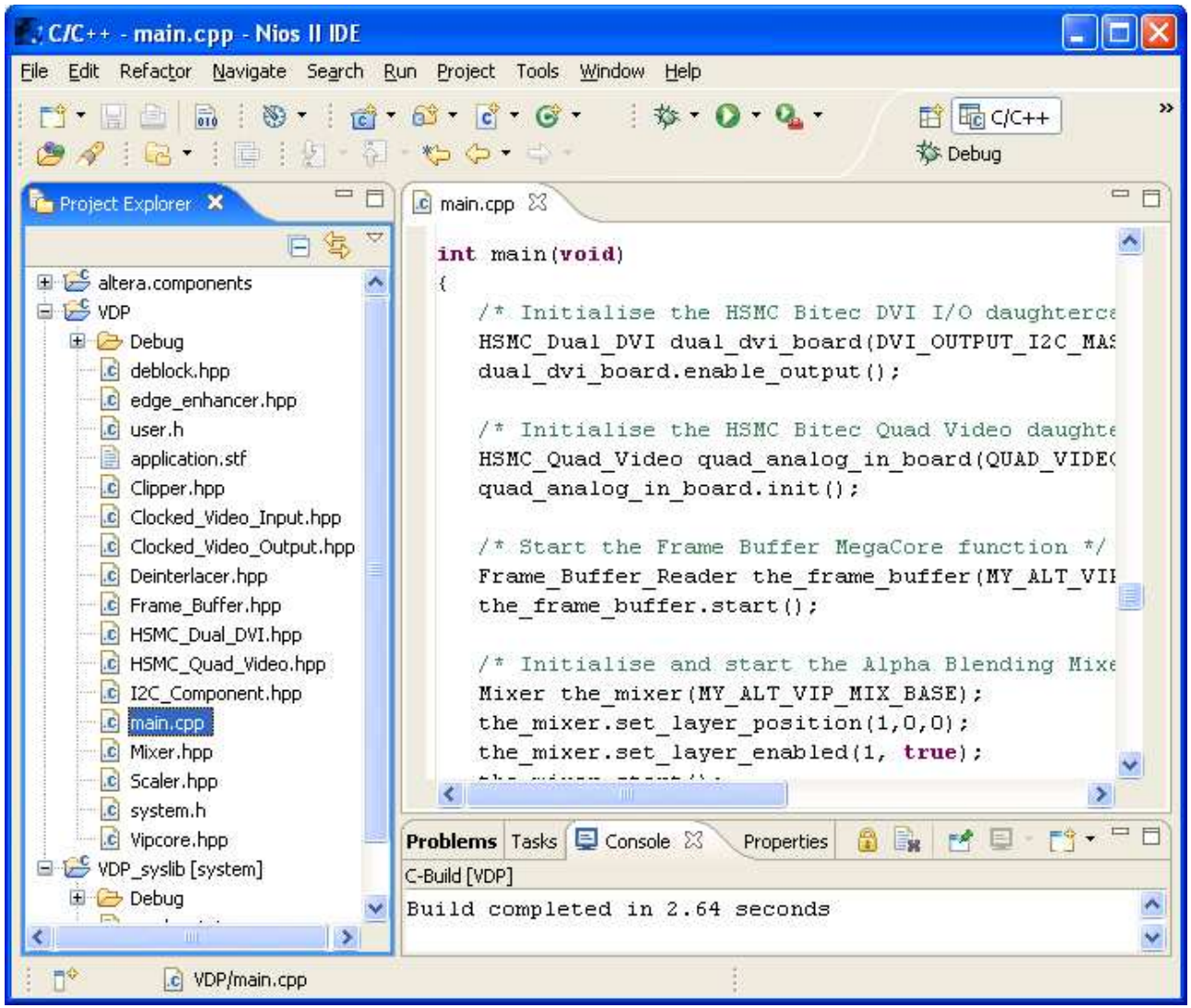


Use	Con...	Module Name	Description	Clock	Base	End	IRQ
☑		⊞ **cpu**	Nios II Processor	**clk_50**	**0x01010800**	0x01010fff	
☑		⊞ **onchip_mem**	On-Chip Memory (RAM or ROM)	**clk_50**	**0x01008000**	0x0100ffff	
☑		⊞ **quad_video_i2c_master**	opencores_i2c_master	**clk_50**	**0x01011000**	0x0101101f	0
☑		⊞ **clock_crossing_0**	Avalon-MM Clock Crossing Bridge	***multiple***	**0x00000000**	0x00001fff	
☑		⊞ **my_alt_vip_cti_1**	Clocked Video Input	**altmemddr...**	**0x00001600**	0x0000167f	1
☑		⊞ **my_alt_vip_clip_1**	Clipper	**altmemddr...**			
☑		⊞ **my_alt_vip_cpr_1**	Color Plane Sequencer	**altmemddr...**			
☑		⊞ **my_alt_vip_crs_1**	Chroma Resampler	**altmemddr...**			
☑		⊟ **my_hybrid_deinterlacer**	hybrid_deinterlace_IP				
	→	avalon_streaming_sink	Avalon Streaming Sink	**altmemddr...**			
	←	avalon_streaming_source	Avalon Streaming Source				
☑		⊟ **my_deblocker**	deblock_IP				
	→	avalon_streaming_sink	Avalon Streaming Sink	**altmemddr...**			
	←	avalon_streaming_source	Avalon Streaming Source				
☑	↩	⊞ **my_edge_enhancer**	edge_enhance_IP	**altmemddr...**			
☑		⊞ **my_alt_vip_csc_1**	CSC	**altmemddr...**			
☑		⊞ **my_alt_vip_scl_1**	Scaler	**altmemddr...**			
☑		⊞ **my_alt_vip_vfb_1**	Frame Buffer	***multiple***			
☑		⊞ **my_alt_vip_cti_2**	Clocked Video Input	**altmemddr...**	**0x00001400**	0x0000147f	2
☑		⊞ **my_alt_vip_clip_2**	Clipper	**altmemddr...**			
☑		⊞ **my_alt_vip_cpr_2**	Color Plane Sequencer	**altmemddr...**			
☑		⊞ **my_alt_vip_crs_2**	Chroma Resampler	**altmemddr...**			
☑		⊞ **my_alt_vip_dil_2**	Deinterlacer	**altmemddr...**			
☑		⊞ **my_alt_vip_csc_2**	CSC	**altmemddr...**			
☑		⊞ **my_alt_vip_scl_2**	Scaler	**altmemddr...**			
☑		⊞ **my_alt_vip_vfb_2**	Frame Buffer	***multiple***			
☑		⊞ **pipeline_bridge_0**	Avalon-MM Pipeline Bridge	**altmemddr...**	0x00000000	0x07ffffff	
☑		⊞ **altmemddr_bot**	DDR2 SDRAM High Performance Contr...	**clk_125**	0x00000000	0x07ffffff	
☑		⊞ **my_alt_vip_tpg_0**	Test Pattern Generator	**altmemddr...**			
☑		⊞ **my_alt_vip_mix**	Alpha Blending Mixer	**altmemddr...**	**0x00001000**	0x000013ff	
☑		⊞ **my_alt_vip_vfb_out_1080P**	Frame Buffer	***multiple***			
☑		⊞ **pipeline_bridge_2**	Avalon-MM Pipeline Bridge	**altmemddr...**	0x00000000	0x07ffffff	
☑		⊞ **altmemddr_top**	DDR2 SDRAM High Performance Contr...	**clk_125**	0x00000000	0x07ffffff	
☑		⊞ **my_alt_vip_itc**	Clocked Video Output	**altmemddr...**	**0x00000000**	0x00000fff	3


altpll0
inclk0
areset
c0
Inclk0 frequency: 125.000 MHz
Operation Mode: Normal
Clk | Ratio | Ph (dg) | DC (%)
c0 | 134/125 | 0.00 | 50.00
Cyclone III
NOT
DVI_int_clk
OUTPUT
81TEC_OV_IDCLK
PIN_AC26
LVDS
OUTPUT
81TEC_OV_RESETn
PIN_AD27
system
clk_125
clk_50
reset_n
global_reset_n_to_the_altmemddr_bot
altmemddr_bot_aux_full_rate_clk_out
altmemddr_bot_aux_half_rate_clk_out
altmemddr_bot_phy_clk_out
altmemddr_top_aux_full_rate_clk_out
altmemddr_top_aux_half_rate_clk_out
altmemddr_top_phy_clk_out
local_init_done_from_the_altmemddr_bot
local_refresh_ack_from_the_altmemddr_bot
local_wdata_req_from_the_altmemddr_bot
mem_addr_from_the_altmemddr_bot[12..0]
mem_ba_from_the_altmemddr_bot[1..0]
mem_cas_n_from_the_altmemddr_bot
mem_cke_from_the_altmemddr_bot
mem_clk_n_to_and_from_the_altmemddr_bot
mem_clk_to_and_from_the_altmemddr_bot
mem_cs_n_from_the_altmemddr_bot
mem_dm_from_the_altmemddr_bot[3..0]
mem_dq_to_and_from_the_altmemddr_bot[31..0]
mem_dqs_to_and_from_the_altmemddr_bot[3..0]
mem_odt_from_the_altmemddr_bot
mem_ras_n_from_the_altmemddr_bot
mem_we_n_from_the_altmemddr_bot
GND
membot_addr[12..0]
membot_ba[1..0]
membot_cas_n
membot_cke
membot_clk_n[0]
membot_clk[0]
membot_cs_n[0]
membot_dm[3..0]
membot_dq[31..0]
membot_dqs[3..0]
membot_odt[0]
membot_ras_n
membot_we_n

Module	File name	Source
Driver of S-video card	HSMC_Quad_video.hpp	Bitec Ltd.
Driver of DVI card	HSMC_Dual_DVI.hpp	Bitec Ltd.
Driver of clocked video input	Clocked_video_input.hpp	Altera library
Driver of clocked video output	Clocked_video_output.hpp	Altera library
Driver of PIO control	Pio_control.hpp	Altera library
Driver of scaler	Scaler.hpp	Altera library
Driver of mixer	Mixer.hpp	Altera library
Driver of frame buffer	Buffer.hpp	Altera library
Driver of deblocker	Deblocker.hpp	Designed in the project
Driver of deinterlacer	Deinterlacer.hpp	Designed in the project
Driver of edge enhancer	Edge_enhance.hpp	Designed in the project
System defined parameter	System.h	Auto-generated by SOPC
User defined parameters	User.h	Designed in the project
Main program	Main.cpp	Designed in the project


Initialize S-video card
Initialize DVI card
Start frame buffer
Initialize video mixer
Is input video stable?
N
Y
Clear input video FIFO
Clear output video FIFO
Start input video
Start output video
Read user button status
Disable/enable function


C/C++ - main.cpp - Nios II IDE
File Edit Refactor Navigate Search Run Project Tools Window Help
C/C++
Debug
Project Explorer
altera.components
VDP
Debug
deblock.hpp
edge_enhancer.hpp
user.h
application.stf
Clipper.hpp
Clocked_Video_Input.hpp
Clocked_Video_Output.hpp
Deinterlacer.hpp
Frame_Buffer.hpp
HSMC_Dual_DVI.hpp
HSMC_Quad_Video.hpp
I2C_Component.hpp
main.cpp
Mixer.hpp
Scaler.hpp
system.h
Vipcore.hpp
VDP_syslib [system]
Debug
main.cpp
int main(void)
{
/* Initialise the HSMC Bitec DVI I/O daughterca
HSMC_Dual_DVI dual_dvi_board(DVI_OUTPUT_I2C_MA
dual_dvi_board.enable_output();
/* Initialise the HSMC Bitec Quad Video daughte
HSMC_Quad_Video quad_analog_in_board(QUAD_VIDE
quad_analog_in_board.init();
/* Start the Frame Buffer MegaCore function */
Frame_Buffer_Reader the_frame_buffer(MY_ALT_VI
the_frame_buffer.start();
/* Initialise and start the Alpha Blending Mixe
Mixer the_mixer(MY_ALT_VIP_MIX_BASE);
the_mixer.set_layer_position(1,0,0);
the_mixer.set_layer_enabled(1, true);
Problems Tasks Console Properties
C-Build [VDP]
Build completed in 2.64 seconds
VDP/main.cpp

1. Download VDP.zip file from http://soc.chonnam.ac.kr/~tqvinh/VDP_lecture/Project/
2. Import IP cores into SOPC system
    1. Edge enhancing IP
    2. Deblocking IP
    3. Deinterlacing IP
    4. Denoise IP
3. Generate SOPC system, and compile the top block
4. Download .sof file to FPGA
5. Open Nios II IDE, and create new project
6. Add source files from IP folder
7. Compile and run the embedded software