Modeling Complex IO with IBIS 4.1

IBIS Summit
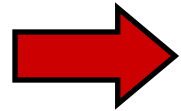
January 31, 2005

Donald Telian

Agenda

- History

- New Data

- Model Types

- Recommendations

Agenda

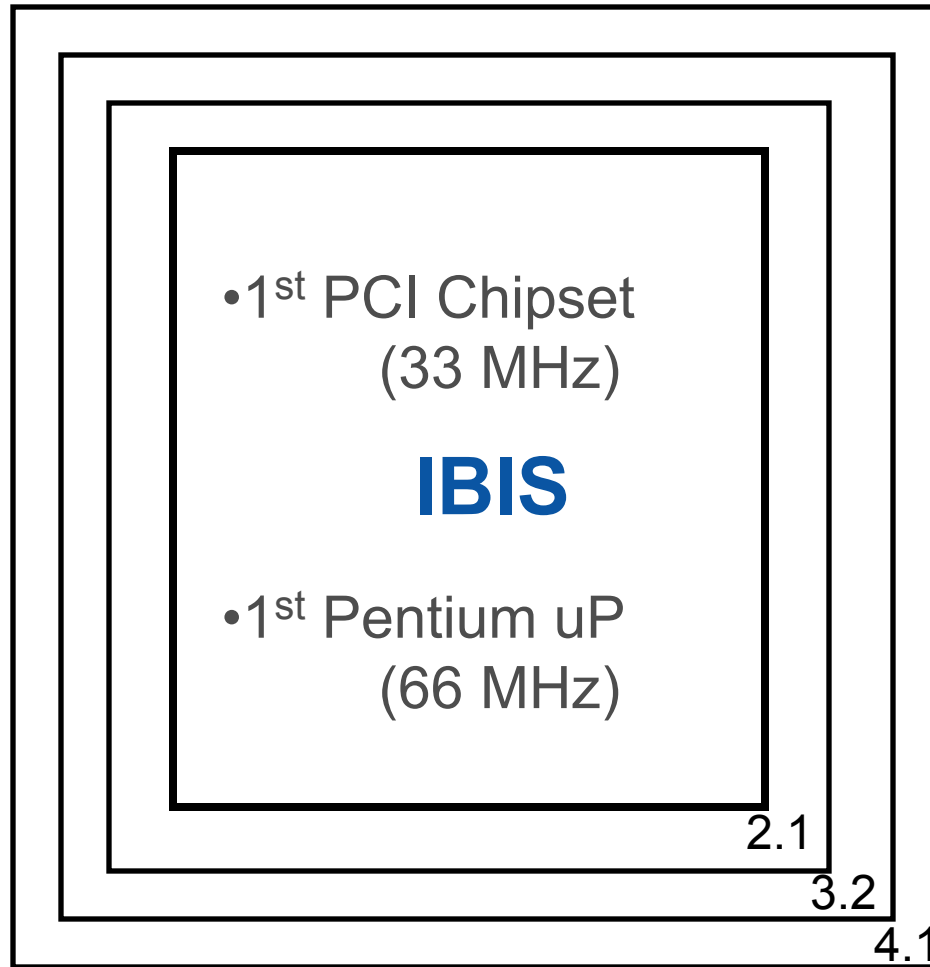- History

- New Data

- Model Types

- Recommendations

IBIS' First Words

In order to…

The Original "Box"

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•1st PCI Chipset
(33 MHz)

IBIS

•1st Pentium uP
(66 MHz)

…and the "Box" did grow

- 1st PCI Chipset
  (33 MHz)

IBIS

- 1st Pentium uP
  (66 MHz)

2.1

3.2

4.1

An increasing amount of Complex IO models are missing the box
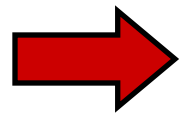
Our Mission

IBIS

Solve the issues to widen the box

*To do so, we'll need a
good understanding of
these Complex IO*

4.1

Agenda

- History

➡️ • New Data

  - Interviews with those working with Complex IO
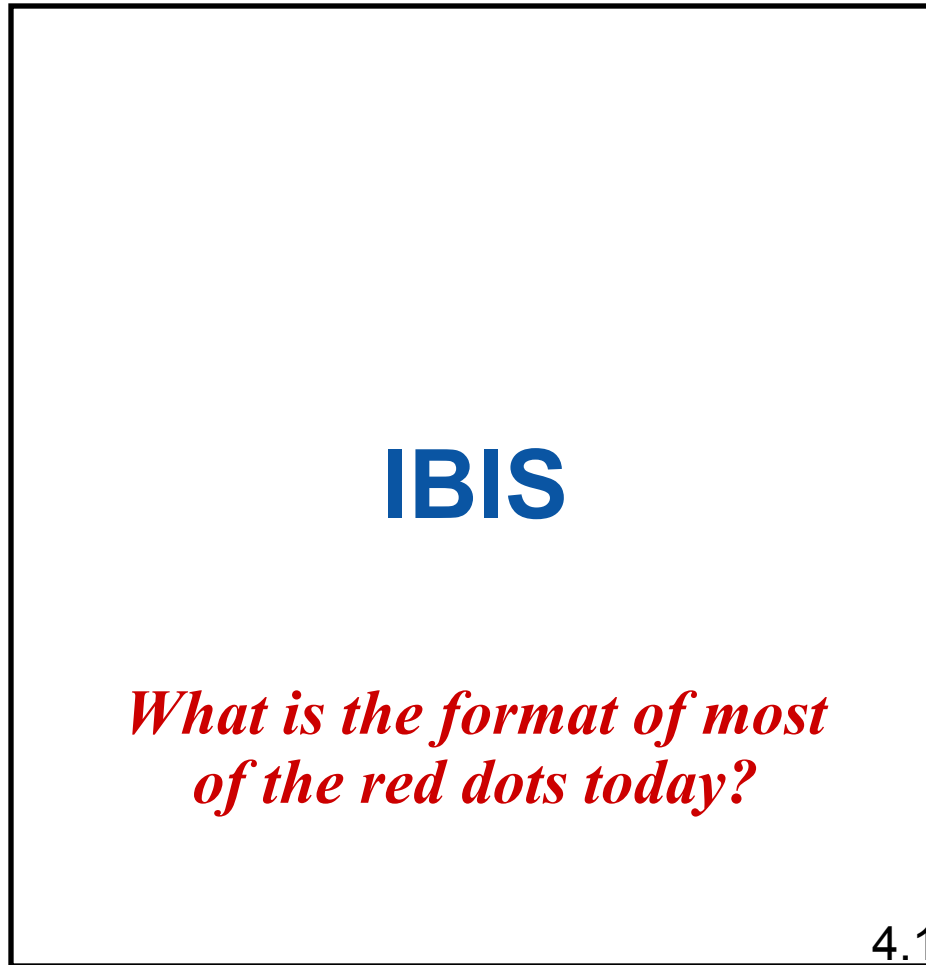
- Model Types

- Recommendations

11 Interviews During December 2004

cādence®

- All are involved with Complex IO

    - Majority were not CDS users

- Good re-introduction to the issues

- The issues are many

    - and the solutions weren't clear

- Will use this data to propose solutions

- Most want "industry standard solution"

    - but don't know how to get there
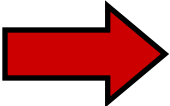
- So who will lead?

The Current Situation

IBIS

*What is the format of most
of the red dots today?*

4.1

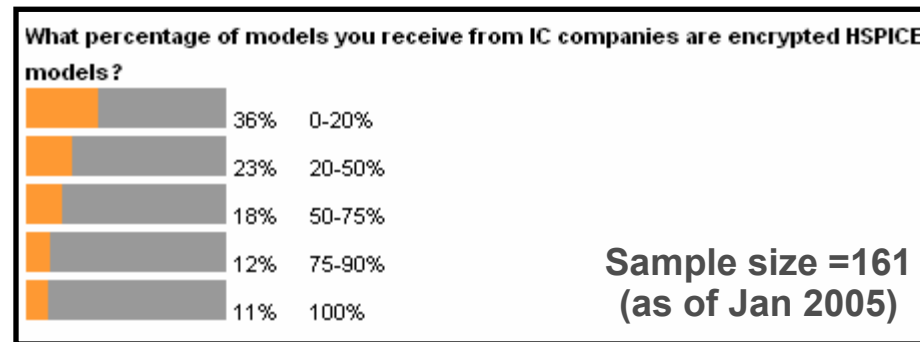# Agenda

- History

- New Data

➡ - Model Types – opportunity/issues with each

  – Hspice

  – AMS

  – SPICE

- Recommendations

High-Speed PCB Web Surveys

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- 64% say that more than 20% of the models they receive are Hspice

What percentage of models you receive from IC companies are encrypted HSPICE models?

%	Range
36%	0-20%
23%	20-50%
18%	50-75%
12%	75-90%
11%	100%

Sample size =161 (as of Jan 2005)

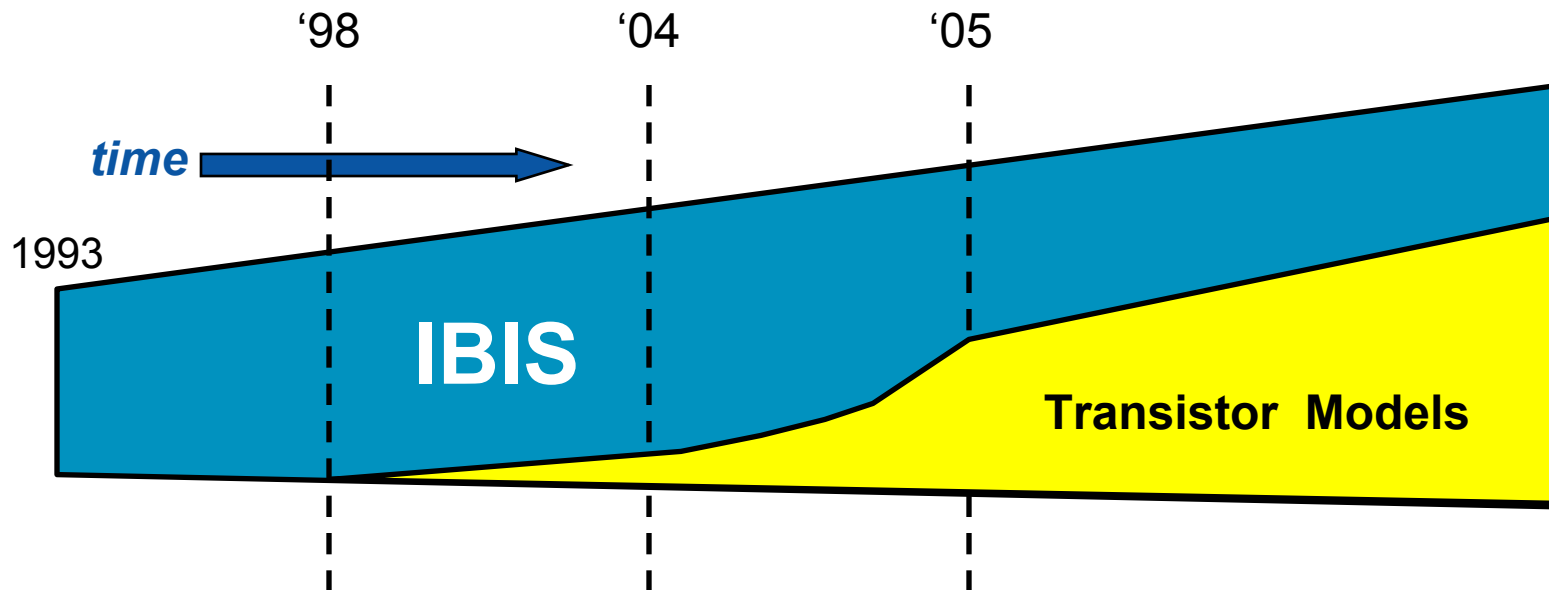http://www.pcbhighspeed.com/discuss/user/non-frames/surveyresults.asp?surveyid=62

- 69% say that this percentage increased in 2004 over 2003

Do you see the percentage of models in encrypted HSPICE increasing in 2004 compared to 2003?

%	
69%	Yes
31%	No

Sample size =432 (as of Jan 2005)

http://www.pcbhighspeed.com/discuss/user/non-frames/surveyresults.asp?surveyid=63

What has Happened

'98   '04   '05

time →

1993

IBIS

Transistor Models

- IBIS enjoyed 5 years as THE digital IO model format

- Higher frequencies brought new issues and more skeptics

- Gigabit serial links brought rapid transistor model increase in 2004

# Hspice Related Interview Questions

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- "Do you want to see [External Model] Hspice?"   - all "yes"
    - Half qualified this as a non-optimal short-term solution

This is actually already happening

- "Do you see Hspice as a long-term solution?"   - all "no"
    - Unanimous reason: "it's too slow"

- As such, also unanimous in need to return to behavioral

What Must Happen

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'98   '04   '05

IBIS

Behavioral

Transistor Models

I B I S
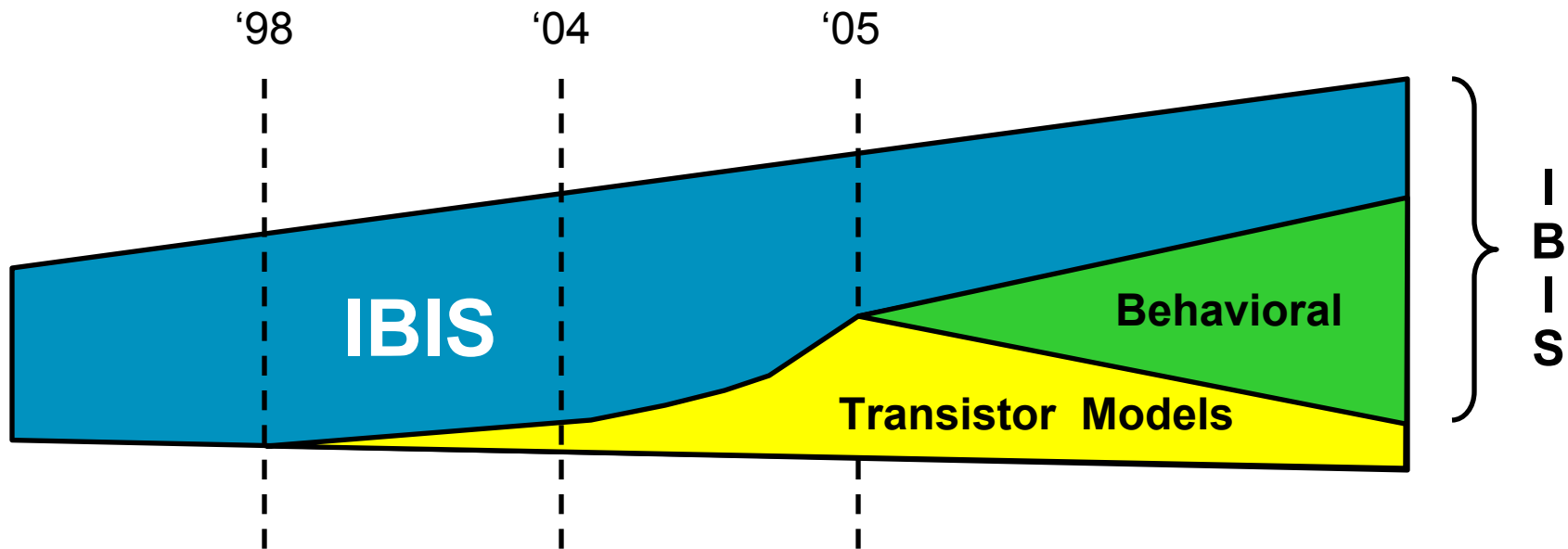
- Enable faster behavioral solutions

What behavioral options exist?

Features of Behavioral Solution

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1. Fast

2. Protects IP

3. Template based

4. Works in many tools

5. Have links to IC design

AMS Models – the Positives

- Most interviewed at this point are unfamiliar with AMS

  - When asked if they think AMS can be a good solution:

    3 said "yes", 3 were hopeful, and 4 were unsure, 1 said no

- The experts list the following positives

  - Standards with documented specs

  - Mathematical freedom

  - Conditionals

  - File IO

  - Flexible language
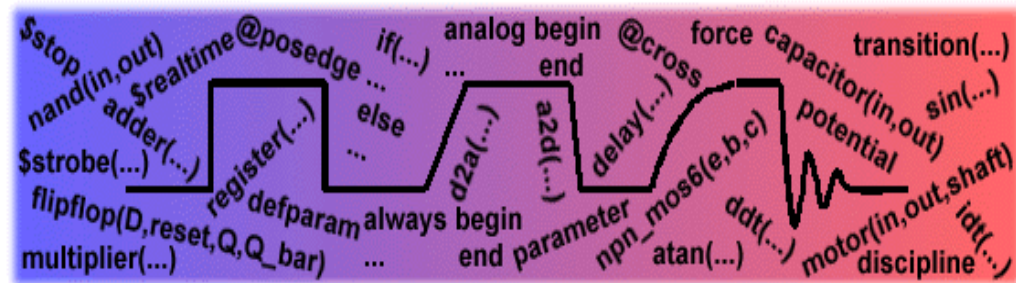
# AMS Models – Issues to Solve

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- Unfamiliar in SI world, learning curve exists

  - Must seed with templates / training

- Spec nuances/implementations (as with IBIS)

- Not naturally occurring in IO design

  - This is why transistor-level models get used

- IP protection

  - 3 would encrypt, 2 might, 4 are unsure, 2 would not

  - Has IBIS thought about this?
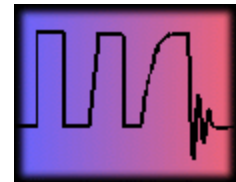
The 4.1 [External Model] SPICE Option

- IBIS 4.1 also specifies [External Model] SPICE

- For most, SPICE == Transistor Model

- BUT
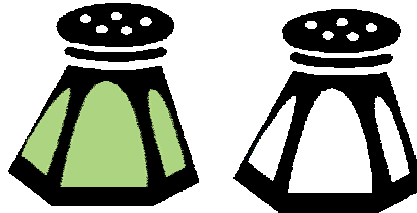
SPICE also == Behavioral Macromodeling

- When it was suggested, all liked the idea

  – many already doing it in some form

- Some history:

  this is the technique Arpad used to invent IBIS and release the first schematic

What Experience has Shown

- Cadence has always had SPICE macromodeling
  - And this has made IBIS keyword support quite simple
- Once we had a central IBIS 2.1 driver element

All later keywords have been macromodeled around it

- In other words, basic SPICE around a B drvr/element has handled everything IBIS has added for the last 10+ years
- What has slowed the industry down is that *additions have belonged to the committee*, and not the model maker

This option empowers the model maker to also add new features

Behavioral SPICE Solutions

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- 2.5 Gbps PCIe SerDes Chipset

  – http://www.cadence.com/company/newsroom/press_releases/pr.aspx?xml=090804_intel

- 1.5 Gbps S-ATA SerDes

  – http://www.designcon.com/conference/7-ta3.html

- Differential pass-thru receiver

  – http://www.eda.org/pub/ibis/summits/jan00/telian.zip

- Adjustable FPGA SerDes

  – http://www.altera.com/corporate/news_room/releases/releases_archive/2004/products/nr-cadence_design_kit.html

- Front-side bus driver, impedance control, SSN, & gate choke effect

  – http://www.cadence.com/company/newsroom/press_releases/11_16_98_SQ_Intel_Merced_Processor.doc

- Others under NDA, mostly higher speed SerDes

The technique has been used for many "beyond IBIS" Complex IO models

[External Model] SPICE Macromodeling   cadence®

- IBIS began with it

- Many tools and users have experience with it

- With template help, model makers are succeeding

- Academia is quite engaged in macromodeling research

  – http://domino.research.ibm.com/acas/w3www_acas.nsf/images/proposals_04.05/$FILE/madhavan.pdf

  – http://domino.research.ibm.com/acas/w3www_acas.nsf/images/projects_03.04/$FILE/canavero.pdf

  – http://www.spi.uni-hannover.de/2004/presentations/spi04_s08_p02_Stievano.pdf

  – http://www.ece.ncsu.edu/erl/html2/papers/paulf/2003/paulf_2003_10_varma.pdf   … etc.

> You are all invited to a CPMT TC-12 (EDP) meeting at which I will be presenting a proposed effort to generate concepts for a future I/O Macromodeling format, based on a collaborative effort involving Madhavan Swaminathan, Michael Steer, and Ambrish Varma. This meeting is held in conjunction with the EPEP meeting, that follows M-W of that week.
>
> **Our intent is to formulate a research program to define a new macromodel format that retains the key features of IBIS (ease of use, ease of simulation, generality) while improving its accuracy, e.g. in SSN simulations.**   Paul Franzon NCSU

How can the IBIS Committee better support this?

Agenda

- History

- New Data

- Model Types

➡ - Recommendations

Remove the Berkeley SPICE Barrier

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- IBIS ties itself to Berkeley SPICE 3F5
  - This was released/closed in 1993
  - No effort since then – yikes!
- No PCB SI tools use this
  - It is lower than the lowest common denominator
- Some have called for a SPICE 4
  - Larry Nagel presented on this in '04
  - This will not likely happen

- Positives
  - Equation-based sources with mathematical operators

1993

Berkeley ⟵
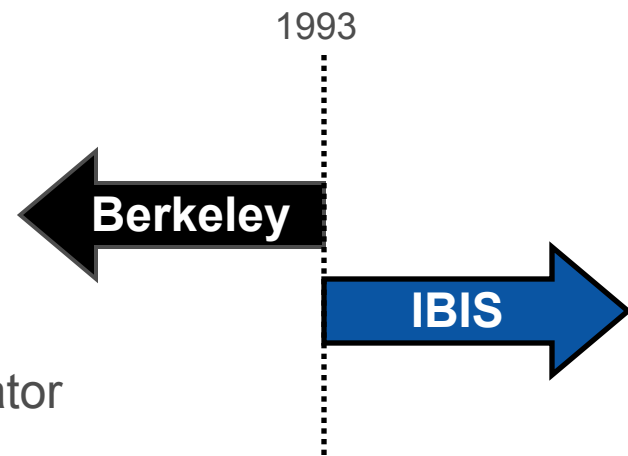
IBIS ⟶

Add to IBIS What's Missing (yet common in existing SPICEs)

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- Must
  - IBIS Driver
  - Table-based EFGH

- Should
  - Parameters (under [EM])

- Could
  - Time-controlled source

1. IBIS [EM]

2. SPICE IBIS
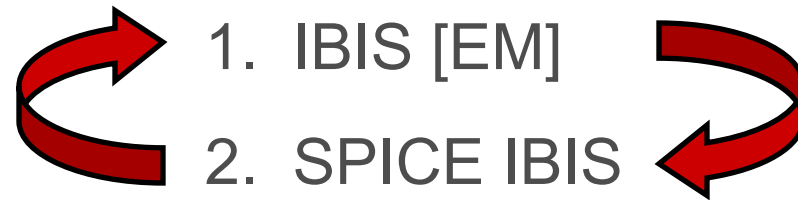
IBIS should pick a syntax for these items (any would do),
then all known complex models could be easily implemented

Create a 4.1 Complex IO Template Repository

- Adaptable Model Templates showcasing use of 4.1 languages

  – Fast path to a model for various Complex IO

- Cadence would offer numerous templates

  – gate-throttle, pass-thru Rx, multi-tap SerDes, Rx equalization, self-compensating drivers, DDR2, …

- No doubt others would too

- At the IBIS web-site?

- In order to…

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