Section 39. Power-Saving Features with Deep Sleep

HIGHLIGHTS

This section of the manual contains the following major topics:

39.1 INTRODUCTION

All PIC24F devices offer a number of built-in strategies for reducing power consumption. These can be particularly useful in applications, which are both power-constrained (such as battery operation), yet require periods of full-power operation for timing-sensitive routines (such as serial communications). This section discusses the four power-saving features implemented in hardware:

- Microcontroller Clock Manipulation
- Instruction-Based Power-Saving Modes (Sleep, Deep Sleep and Idle)
- Software Controlled Doze Mode
- Selective Peripheral Control

39.2 MICROCONTROLLER CLOCK MANIPULATION

In general, reducing the microcontroller clock speed for any application will result in a power saving that is roughly proportional to the clock frequency reduction. PIC24F devices allow for a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can switch between low-power operation from an internal RC oscillator, or high-speed and high-precision operation from a crystal oscillator, by simply changing the NOSC Configuration bits. In fact, users can choose between up to five different oscillators at any time, allowing a maximum amount of flexibility in configuring application speed, frequency precision and power consumption.

The process of changing the system clock during operation, as well as restrictions on clock changes, are discussed in more detail in the PIC24F Family Reference Manual **Section 6. "Oscillator"**.

Note:	Oscillator availability varies by device. Refer to the device data sheet to determine what oscillators are available.

39.3 INSTRUCTION-BASED POWER-SAVING MODES

PIC24F devices have three special power-saving modes that can be entered through the execution of a special PWRSAV instruction:

- Sleep Mode: The CPU, system clock source and any peripherals that operate on the system clock source are disabled. This is the lowest power mode for the device.
- Idle Mode: The CPU is disabled, but the system clock source continues to operate. Peripherals continue to operate, but can optionally be disabled.
- Deep Sleep Mode: The CPU, system clock source and all the peripherals except RTCC and DSWDT are disabled. This is the lowest power mode for the device. The power to RAM and Flash is also disabled.

The assembly syntax of the PWRSAV instruction is provided in Example 39-1.

Example 39-1: PWRSAV Assembly Syntax for Sleep Mode

```
//Put the device into Sleep mode
PWRSAV  #SLEEP_MODE;
```

Example 39-2: PWRSAV Assembly Syntax for Idle Mode

```
//Put the device into Idle mode
PWRSAV  #IDLE_MODE;
```

Example 39-3: PWRSAV Assembly Syntax for Deep Sleep Mode

```
//Put the device into Deep Sleep mode
BSET     DSCON DSEN
PWRSAV   #SLEEP_MODE;
```

Note: SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

The Sleep and Idle modes can be exited due to enabled interrupt, WDT time-out or a device Reset. The Deep Sleep mode can be exited due to INT0 interrupt, DSWDT time-out, RTCC interrupt or device Reset. When the device exits one of these three operating modes, it is said to 'wake-up'. The characteristics of the power-saving modes are described in the subsequent sections.

Note: Deep Sleep mode is not available on all PIC24F devices. Refer to the device data sheet to determine if Deep Sleep mode is supported.

39.3.1 Interrupts' Coincident with Power Save Instructions

Any interrupt that coincides with the execution of a PWRSAV instruction will be held off until entry into Sleep, Idle or Deep Sleep mode is completed. The device will then wake-up from Power-Managed mode.

39.3.2 Sleep Mode

The characteristics of Sleep mode are:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption will be optimum provided, no I/O pin is sourcing the current.
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode since the system clock source is disabled.
- The LPRC clock will continue to run in Sleep mode if the WDT is enabled.
- If the on-chip voltage regulator and Brown-out Reset (BOR) are enabled, its Brown-out Reset (BOR) circuit remains operational during Sleep mode.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some peripherals may continue to operate in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, or peripherals that use an external clock input. Any peripheral that operates from the system clock source will be disabled in Sleep mode.

The processor will exit, or 'wake-up', from Sleep on one of the following events:

- On any interrupt source that is individually enabled
- On any form of device Reset
- On a WDT time-out

39.3.2.1 CLOCK SELECTION ON WAKE-UP FROM SLEEP MODE

The processor will restart the same clock source that was active when Sleep mode was entered.

39.3.2.2 DELAY ON WAKE-UP FROM SLEEP MODE

The restart delay associated with waking up from Sleep mode for different oscillator modes is shown in Table 39-1.

Table 39-1: Delay Times for Exiting from Sleep Mode

Clock Source		Sleep Exit Delay	Oscillator Delay	Notes
EC		TVEG/TPM	—	**1**
ECPLL		TVEG/TPM	TLOCK	**1, 3**
XT, HS		TVEG/TPM	TOST	**1, 2**
XTPLL, HSPLL		TVEG/TPM	TOST + TLOCK	**1, 2, 3, 4**
SOSC	(Off during Sleep)	TVEG/TFLASH	TOST	**1, 2**
	(On during Sleep)	TVEG/TPM	—	**1**
FRC, FRCDIV		TVEG/TPM	TFRC	**1, 5**
LPRC	(Off during Sleep)	TVEG/TFLASH	TLPRC	**1, 5**
	(On during Sleep)	TVEG/TPM	—	**1**
FRCPLL		TVEG/TPM	TLOCK	**1, 3**

Note 1: TVREG = Start-up delay on devices with an on-chip regulator. The TVREG delay occurs when the regulator is disabled (VREGS = 0). TPM = Start-up delay on devices without an on-chip regulator. The TPM is an additional delay for program memory stabilization when powered down during Sleep (PMSLP = 0).

2: TOST = Oscillator Start-up Timer; a delay of 1024 oscillator periods before the oscillator clock is released to the system.

3: TLOCK = PLL lock time.

4: HSPLL mode exceeds PIC24F maximum operating frequency.

5: TFRC and TLPRC are RC oscillator start-up times.

Note:	Please refer to the **"Electrical Characteristics"** section of the product data sheet for detailed operating frequency and timing specification values.

39.3.2.3 WAKE-UP FROM SLEEP MODE WITH CRYSTAL OSCILLATOR OR PLL

If the system clock source is derived from a crystal oscillator and/or the PLL, the Oscillator Start-up Timer (OST) and/or PLL lock times must be applied before the system clock source is made available to the device. As an exception to this rule, no oscillator delays are necessary if the system clock source is the secondary oscillator and it was running while in Sleep mode.

39.3.2.4 SLOW OSCILLATOR START-UP

The OST and PLL lock times may not have expired when the power-up delays have expired.

To avoid this condition, one can enable Two-Speed Start-up by the device that will run on FRC until the clock source is stable. Once the clock source is stable, the device will switch to the selected clock source.

39.3.2.5 WAKE-UP FROM SLEEP ON INTERRUPT

User interrupt sources that are assigned to CPU Priority Level 0 cannot wake-up the CPU from Sleep mode because the interrupt source is effectively disabled. To use an interrupt as a wake-up source, the CPU priority level for the interrupt must be assigned to CPU Priority Level 1 or greater.

Any source of interrupt that is individually enabled, using its corresponding IE control bit in the IECx registers, can wake-up the processor from Sleep mode. When the device wakes from Sleep mode, one of two following actions may occur:

- If the assigned priority for the interrupt is less than or equal to the current CPU priority, the device will wake-up and continue code execution from the instruction following the `PWRSAV` instruction that initiated Sleep mode.
- If the assigned priority level for the interrupt source is greater than the current CPU priority, the device will wake-up and the CPU exception process will begin. Code execution will continue from the first instruction of the ISR.

The SLEEP status bit (RCON<3>) is set upon wake-up. For RCON register values, refer to **Section 7. "Reset"**.

39.3.2.6 WAKE-UP FROM SLEEP ON RESET

All sources of device Reset will wake-up the processor from Sleep mode. Any source of Reset (other than a POR) that wakes the processor will set the SLEEP status bit (RCON<3>) to indicate that the device was previously in Sleep mode.

On a Power-on Reset (POR), the SLEEP bit is cleared.

39.3.2.7 WAKE-UP FROM SLEEP ON WATCHDOG TIME-OUT

If the Watchdog Timer (WDT) is enabled and expires while the device is in Sleep mode, the processor will wake-up. The WDTO and SLEEP status bits (RCON<4:3>) are both set to indicate that the device resumed operation due to the WDT expiration. Note that this event does not reset the device. Operation continues from the instruction following the `PWRSAV` instruction that initiated Sleep mode.

39.3.3 Idle Mode

When the device enters Idle mode, the following events occur:

- The CPU will stop executing instructions.
- The WDT is automatically cleared.
- The system clock source will remain active and peripheral modules, by default, will continue to operate normally from the system clock source. Peripherals can optionally be shutdown in Idle mode using their 'Stop in Idle' control bit. (See peripheral descriptions for further details.)
- If the WDT or FSCM is enabled, the LPRC will also remain active.

The processor will wake-up from Idle mode on the following events:

- On any interrupt that is individually enabled.
- On any source of device Reset.
- On a WDT time-out.

Upon wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution begins immediately, starting with the instruction following the `PWRSAV` instruction, or the first instruction in the ISR.

39.3.3.1 WAKE-UP FROM IDLE ON INTERRUPT

User interrupt sources that are assigned to CPU Priority Level 0 cannot wake-up the CPU from Idle mode because the interrupt source is effectively disabled. To use an interrupt as a wake-up source, the CPU priority level for the interrupt must be assigned to CPU Priority Level 1 or greater.

Any source of interrupt that is individually enabled using the corresponding IE control bit in the IECx register, and exceeds the current CPU priority level, will be able to wake-up the processor from Idle mode. When the device wakes from Idle mode, one of two options may occur:

- If the assigned priority for the interrupt is less than or equal to the current CPU priority, the device will wake-up and continue code execution from the instruction following the `PWRSAV` instruction that initiated Idle mode.
- If the assigned priority level for the interrupt source is greater than the current CPU priority, the device will wake-up and the CPU exception process will begin. Code execution will continue from the first instruction of the ISR.

The IDLE status bit (RCON<2>) is set upon wake-up.

39.3.3.2 WAKE-UP FROM IDLE ON RESET

Any Reset, other than a POR, will wake-up the CPU from Idle mode. On any device Reset, except a POR, the IDLE status bit is set (RCON<2>) to indicate that the device was previously in Idle mode. In a POR, the IDLE bit is cleared.

39.3.3.3 WAKE-UP FROM IDLE ON WDT TIME-OUT

If the WDT is enabled, then the processor will wake-up from Idle mode on a WDT time-out and continue code execution with the instruction following the `PWRSAV` instruction that initiated Idle mode. Note that the WDT time-out does not reset the device in this case. The WDTO and IDLE status bits (RCON<4,2>) will both be set.

39.3.3.4 TIME DELAYS ON WAKE-UP FROM IDLE MODE

Unlike a wake-up from Sleep mode, there are no additional time delays associated with wake-up from Idle mode. The system clock is running during Idle mode, therefore, no start-up times are required at wake-up.

39.3.4 Deep Sleep Mode

Note:	Not all devices support Deep Sleep mode. Refer to the device data sheet to determine if this feature is present on the device.

Deep Sleep mode brings the device into its lowest power consumption state without requiring the use of external switches to remove power from the device. During Deep Sleep, the power to the core is removed, effectively disconnecting power to the core logic of the microcontroller.

Note:	In Deep Sleep mode, the device with an on-chip regulator powers down the microcontroller by turning off the on-chip VDDCORE voltage regulator, Deep Sleep capability is available only when operating with the internal regulator enabled.

On devices that support it, the Deep Sleep mode is entered by:

- Setting the DSEN bit (DSCON<15>)
- Executing the SLEEP instruction immediately after setting DSEN (no delay in between)

In order to minimize the possibility of inadvertently entering Deep Sleep, the DSEN bit is cleared in hardware after two instruction cycles have been set. Therefore, in order to enter Deep Sleep, the SLEEP instruction must be executed in the immediate instruction cycle after setting DSEN. If DSEN is not set when Sleep is executed, the device will enter conventional Sleep mode instead.

During Deep Sleep, the core logic circuitry of the microcontroller is powered down to reduce leakage current. Therefore, most peripherals and functions of the microcontroller become unavailable during Deep Sleep. Two data memory locations, DSGPR0 and DSGPR1, are preserved for context information after exit of Deep Sleep. However, a few specific peripherals and functions are powered directly from the VDD supply rail of the microcontroller, and therefore, can continue to function in Deep Sleep.

The device has a dedicated Deep Sleep Brown-out Reset (DSBOR) and Deep Sleep Watchdog Timer Reset (DSWDT) for monitoring voltage and time-out events in Deep Sleep mode. The DSBOR and DSWDT are independent of the standard BOR and WDT used with other power-managed modes (Run, Idle and Sleep).

Entering Deep Sleep mode clears the DSWAKE register. If enabled, the Real-Time Clock and Calendar (RTCC) continues to operate uninterrupted.

When a wake-up event occurs in Deep Sleep mode (by Reset, RTCC alarm, external interrupt (INT0) or DSWDT), the device will exit Deep Sleep mode and rearm a Power-on Reset (POR). When the device is released from Reset, code execution will resume at the device's Reset vector.

39.3.4.1 WAKE-UP DELAY

The Reset delay associated with wake-up from Deep Sleep in different oscillator modes is provided in Table 39-2.

Table 39-2: Delay Times for Exiting from Deep Sleep Mode

Clock Source		Deep Sleep Exit Delay	Oscillator Delay	Notes
EC		TDSWU	—	
ECPLL		TDSWU	TLOCK	**1, 3**
XT, HS		TDSWU	TOST	**1, 2**
XTPLL, HSPLL		TDSWU	TOST + TLOCK	**1, 2, 3, 4**
SOSC	(Off during Sleep)	TDSWU	TOST	**1, 2**
	(On during Sleep)	TDSWU	—	**1**
FRC, FRCDIV		TDSWU	TFRC	**1, 5**
LPRC	(Off during Sleep)	TDSWU	TLPRC	**1, 5**
	(On during Sleep)	TDSWU	—	**1**
FRCPLL		TDSWU	TFRC + TLOCK	**1, 3, 5**

Note 1: TDSWU = Deep Sleep wake-up delay.

2: TOST = Oscillator Start-up Timer; a delay of 1024 oscillator periods before the oscillator clock is released to the system.

3: TLOCK = PLL lock time.

4: HSPLL mode exceeds PIC24F maximum operating frequency.

5: TFRC and TLPRC are RC oscillator start-up times.

Note:	Refer to the **"Electrical Characteristics"** section of the product data sheet for maximum operating frequency, TDSWU, TFSCM, TLOCK and oscillator start-up specification values.

39.3.4.2 DEEP SLEEP WAKE-UP SOURCES

The device can be awakened from Deep Sleep mode by a $\overline{\text{MCLR}}$, POR, RTCC, INT0 I/O pin interrupt or DSWDT event. After waking, the device performs a POR. When the device is released from Reset, code execution will begin at the device's Reset vector.

The software can determine if the wake-up was caused from an exit from Deep Sleep mode by reading the DS bit (RCON<10>). If this bit is set, the POR was caused by a Deep Sleep exit. The DS bit must be manually cleared by the software.

The software can determine the wake-up event source by reading the DSWAKE register. These registers are cleared automatically when entering Deep Sleep mode, so software should read these registers after exiting Deep Sleep mode or before re-enabling this mode.

39.3.4.2.1 Clock Selection on Wake-up from Deep Sleep Mode

The processor will restart with the default oscillator source, selected with the FNOSC Configuration bits. On wake-up from Deep Sleep, a POR is generated internally, hence, the system resets to its POR state with exception of the RCON, DSCON and DSGPRx registers.

39.3.4.3 SAVING CONTEXT DATA WITH THE DSGPR0/DSGPR1 REGISTERS

As exiting Deep Sleep mode causes a POR, most Special Function Registers reset to their default POR values. In addition, because the core power is not supplied in Deep Sleep mode, information in data RAM may be lost when exiting this mode. Applications which require critical data to be saved prior to Deep Sleep may use the Deep Sleep General Purpose registers, DSGPR0 and DSGPR1, or data EEPROM (if available). Unlike other SFRs, the contents of these registers are preserved while the device is in Deep Sleep mode. After exiting Deep Sleep, software can restore the data by reading the registers and clearing the RELEASE bit (DSCON<0>).

39.3.4.4 I/O PINS DURING DEEP SLEEP

During Deep Sleep, the general purpose I/O pins will retain their previous states.

Pins that are configured as inputs (TRIS bit set) prior to entry into Deep Sleep will remain high-impedance during Deep Sleep.

Pins that are configured as outputs (TRIS bit clear) prior to entry into Deep Sleep will remain as output pins during Deep Sleep. While in this mode, they will drive the output level determined by their corresponding LAT bit at the time of entry into Deep Sleep.

Once the device wakes back up, all I/O pins will continue to maintain their previous states, even after the device has finished the POR sequence and is executing application code again. Pins configured as inputs during Deep Sleep will remain high-impedance, and pins configured as outputs will continue to drive their previous value. After waking up, the TRIS and LAT registers will be reset. If firmware modifies the TRIS and LAT values for the I/O pins, they will not immediately go to the newly configured states. Once the firmware clears the RELEASE bit (DSCON<0>), the I/O pins are “released”. This causes the I/O pins to take the states configured by their respective TRIS and LAT bit values.

If the Deep Sleep BOR (DSBOR) is enabled, and a DSBOR event occurs during Deep Sleep (or V_{DD} is hard cycled to V_{SS}), the I/O pins will be immediately released similar to clearing the RELEASE bit. All previous state information will be lost, including the general purpose DSGPR0 and DSGPR1 contents.

If a $\overline{MCLR}$ Reset event occurs during Deep Sleep, the I/O pins will also be released automatically, but in this case, the DSGPR0 and DSGPR1 contents will remain valid.

In case of $\overline{MCLR}$ Reset and all other Deep Sleep wake-up cases, application firmware needs to clear the RELEASE bit (DSCON<0>) in order to reconfigure the I/O pins.

39.3.4.5 DEEP SLEEP WATCHDOG TIMER (DSWDT)

Deep Sleep has its dedicated WDT (DSWDT) with a postscaler for time-outs of 2.1 ms to 25.7 days, configurable through the Configuration bits, DSWDTPS<3:0>.

DSWDT also has a configurable reference clock source for selecting the LPRC or SOSC. The reference clock source is configured through the DSWDTOSC Configuration bit.

DSWDT is enabled through the DSWDTEN bit. Entering Deep Sleep mode automatically clears the DSWDT.

Under certain circumstances, it is possible for the DSWDT clock source to be off when entering Deep Sleep mode. In this case, the clock source is turned on automatically (if DSWDT is enabled), without the need for software intervention. However, this can cause a delay in the start of the DSWDT counters. In order to avoid this delay, when using SOSC as a clock source, the application can activate SOSC prior to entering Deep Sleep mode.

39.3.4.6 DEEP SLEEP LOW-POWER BROWN-OUT RESET

The device has its dedicated BOR for Deep Sleep mode (DSBOR). It has a trip point range of 1.7V-2.3V nominal, and is enabled through the DSBOREN Configuration bit. When the device enters Deep Sleep mode and receives a DSBOR event, the device will not wake-up and will remain in Deep Sleep mode. When a valid wake-up event occurs and causes the device to exit Deep Sleep mode, software can determine if a DSBOR event occurred during Deep Sleep mode by reading the DSBOR (DSCON<1>) status bit.

39.3.4.7 RTCC PERIPHERAL AND DEEP SLEEP

The RTCC can operate uninterrupted during Deep Sleep mode. It can wake-up the device from Deep Sleep by configuring an alarm.

The RTCC clock source is configured with the RTCOSC Configuration bit. The available reference clock sources are the LPRC and SOSC. If the LPRC is used, the RTCC accuracy will directly depend on the LPRC tolerance.

39.3.4.8 TYPICAL DEEP SLEEP SEQUENCE

To review, these are the necessary steps involved in invoking and exiting Deep Sleep mode:

1. Device exits Reset and begins to execute its application code.
2. If DSWDT functionality is required, program the appropriate Configuration bit.
3. Select the appropriate clock(s) for the DSWDT and RTCC (optional).
4. Enable and configure the DSWDT (optional).
5. Enable and configure the RTCC (optional).
6. Write context data to the DSGPRx registers (optional).
7. Enable the INT0 interrupt (optional).
8. Set the DSEN bit in the DSCON register.
9. Enter Deep Sleep by issuing a `PWRSV #SLEEP_MODE` command.
10. Device exits Deep Sleep when a wake-up event occurs.
11. The DSEN bit is automatically cleared.
12. Read and clear the DS status bit in RCON, and the DSWAKE status bits.
13. Read the DSGPRx registers (optional).
14. Once all state related configurations are complete, clear the RELEASE bit.
15. Application resumes normal operation.

Register 39-1: RCON: Reset Control Register(1)

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0	R/W-0
TRAPR	IOPUWR	SBOREN	—	—	DPSLP	—	VREGS/PMSLP
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TRAPR:** Trap Reset Flag bit
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit
1 = An illegal opcode detection, an illegal address mode or uninitialized W register used as an Address Pointer caused a Reset
0 = An illegal opcode or uninitialized W Reset has not occurred

bit 13 **SBOREN:** Software Enable/Disable of BOR bit
1 = BOR is turned on in software
0 = BOR is turned off in software

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **DPSLP:** Deep Sleep Mode Flag bit
1 = Deep Sleep has occurred
0 = Deep Sleep has not occurred

bit 9 **Unimplemented:** Read as '0'

bit 8 **VREGS:** Voltage Regulator Standby Enable bit
1 = Regulator will be active during Sleep
0 = Regulator will go to Standby mode during Sleep

PMSLP: Program Memory Power During Sleep bit
1 = Program memory bias voltage remains powered during Sleep
0 = Program memory bias voltage is powered down during Sleep

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin bit
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset (Instruction) Flag bit
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed

bit 5 **SWDTEN:** Software Enable/Disable of WDT bit(2)
1 = WDT is enabled
0 = WDT is disabled

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

bit 3 **SLEEP:** Wake From Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up From Idle Flag bit
1 = Device has been in Idle mode
0 = Device has not been in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit
1 = A Brown-out Reset has occurred. Note that BOR is also set after a Power-on Reset.
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = A Power-up Reset has occurred
0 = A Power-up Reset has not occurred

Note 1: All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

Register 39-2: DSCON: Deep Sleep Control Register

R/W-0, HC	U-0	U-0	U-0	U-0	U-0	U-0	U-0
DSEN(1)	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HCS(2)	R/W-0, HS(2)
—	—	—	—	—	—	DSBOR	RELEASE
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HCS = Hardware Clearable/Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
HS = Hardware Settable bit			

bit 15 **DSEN:** Deep Sleep enable bit(1)
1 = Deep Sleep mode is entered on a SLEEP command
0 = Sleep mode is entered on a SLEEP command

bit 14-2 **Unimplemented:** Read as '0'

bit 1 **DSBOR:** Deep Sleep BOR Event Status bit(2)
1 = DSBOREN was enabled and VDD dropped below the DSBOR threshold during Deep Sleep(3)
0 = DSBOREN was disabled, or VDD did not drop below the DSBOR threshold during Deep Sleep

bit 0 **RELEASE:** I/O Pin State Release bit(2)
1 = Upon waking from Deep Sleep, the I/O pins maintain their previous states
0 = Release I/O pins and allow their respective TRIS and LAT bits to control their states

Note 1: In order to enter Deep Sleep, Sleep must be executed immediately after setting DSEN.
2: This is the value when VDD is initially applied.
3: Unlike all other events, a Deep Sleep BOR event will not cause a wake-up from Deep Sleep; this bit is present only as a status bit.

Register 39-3: DSWAKE: Deep Sleep Wake-up Source Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS
—	—	—	—	—	—	—	DSINT0
bit 15							bit 8

R/W-0, HS	U-0	U-0	R/W-0, HS	R/W-0	R/W-0, HS	U-0	R/W-0
DSFLT	—	—	DSWDT	DSRTC	DSMCLR	—	DSPOR(1)
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **DSINT0:** Interrupt-on-Change bit
1 = Interrupt-on-change was asserted during Deep Sleep
0 = Interrupt-on-change was not asserted during Deep Sleep

bit 7 **DSFLT:** Deep Sleep Fault Detected bit
1 = A Fault occurred during Deep Sleep, and some Deep Sleep configuration settings may have been corrupted
0 = No Fault was detected during Deep Sleep

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **DSWDT:** Deep Sleep Watchdog Timer Time-out bit
1 = The Deep Sleep Watchdog Timer timed out during Deep Sleep
0 = The Deep Sleep Watchdog Timer did not time out during Deep Sleep

bit 3 **DSRTC:** Real-Time Clock and Calendar Alarm bit
1 = The Real-Time Clock and Calendar triggered an alarm during Deep Sleep
0 = The Real-Time Clock and Calendar did not trigger an alarm during Deep Sleep

bit 2 **DSMCLR:** $\overline{\text{MCLR}}$ Event bit
1 = The $\overline{\text{MCLR}}$ pin was active and was asserted during Deep Sleep
0 = The $\overline{\text{MCLR}}$ pin was not active, or was active, but not asserted during Deep Sleep

bit 1 **Unimplemented:** Read as '0'

bit 0 **DSPOR:** Deep Sleep Fault Detected bit(1)
1 = The VDD supply POR circuit was active and a POR event was detected
0 = The VDD supply POR circuit was not active, or was active, but did not detect a POR event

Note 1: Unlike the other bits in this register, this bit can be set outside of Deep Sleep.

Register 39-4: DSGPR0: Deep Sleep Persistent General Purpose Register 0(1)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Deep Sleep Persistent General Purpose bits							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Deep Sleep Persistent General Purpose bits							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 Deep Sleep Persistent General Purpose bits
Contents are retained, even in Deep Sleep mode.

Note 1: All register bits are reset only in the case of a VDD POR event outside of Deep Sleep mode.

Register 39-5: DSGPR1: Deep Sleep Persistent General Purpose Register 1(1)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Deep Sleep Persistent General Purpose bits							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Deep Sleep Persistent General Purpose bits							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 Deep Sleep Persistent General Purpose bits
Contents are retained, even in Deep Sleep mode.

Note 1: All register bits are reset only in the case of a VDD POR event outside of Deep Sleep mode.

39.3.5 Doze Mode

Changing clock speed and invoking one of the instruction-based Power-Saving modes are effective strategies for reducing power consumption. There may be circumstances, however, where this is not practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed may introduce communication errors, while using a Power-Saving mode may stop communications completely.

Doze mode provides an alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the Special Function Registers (SFRs) while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default. For CLKDIV register values, refer to the appropriate oscillator section in the *"PIC24F Family Reference Manual"*.

39.3.5.1 RETURN FROM DOZE ON INTERRUPT

Doze mode can be configured to automatically return to full-speed CPU execution on an interrupt event. Enabling the automatic return to full-speed CPU operation on interrupts is enabled by setting the ROI bit (CLKDIV<15>). By default, the ROI bit is cleared and interrupt events have no effect on Doze mode operation. When an interrupt event occurs in Doze mode and ROI is set, the DOZEN bit is automatically cleared.

The return from Doze mode feature allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU executes at a much lower speed, waiting for an event to invoke an interrupt routine and resume processing.

39.4 SELECTIVE PERIPHERAL POWER CONTROL

Sleep, Idle and Doze modes allow users to substantially reduce power consumption by slowing or stopping the CPU clock. Even so, peripheral modules still remain clocked, and thus, consume some amount of power. There may be cases where the application needs what these modes do not provide: the ability to allocate limited power resources to the CPU while eliminating power consumption from the peripherals. PIC24F devices address this requirement by allowing peripheral modules to be selectively enabled or disabled, reducing or eliminating their power consumption.

39.4.1 Disabling Peripheral Modules

Most of the peripheral modules in the PIC24F family architecture can be selectively disabled, reducing or essentially eliminating their power consumption during all operating modes. Two different options are available to users, each with a slightly different effect.

39.4.1.1 MODULE ENABLE BIT (XXXEN)

Many peripheral modules have a Module Enable bit, generically named, “XXXEN”, usually located in bit position 15 of their control registers (or primary control registers for more complex modules). Here, “XXX” represents the mnemonic form for the module of the module name. For example, the enable bit for an SPI module is “SPIEN”, and so on. The bit is provided for all serial and parallel communications modules and the Real-Time Clock (RTC). Clearing this bit disables the module’s operation; however, it continues to receive clock signals and draw a minimal amount of current.

As with all earlier PIC® MCU devices, timers continue to be under selective operation and are controlled by their own TON bit, also located in position 15. The A/D Converter also has a legacy enable bit, ADON, that has the same function as the XXXEN bits. I/O ports and features associated with them, such as input change notification and input capture, do not have their own module enable bits, since their operation is secondary to other modules.

Disabling modules not required for a particular application in this manner allows for the selective and dynamic adjusting power consumption, under software control, as the application is running.

39.4.1.2 PERIPHERAL MODULE DISABLE BIT (XXMD)

All peripheral modules (except for I/O ports) also have a second control bit that can disable their functionality. These bits, known as the Peripheral Module Disable (PMD) bits, are generically named “XXMD” (using “XX” as the mnemonic version of the module’s name, as before). These bits are located in the PMDx SFRs. In contrast to the module enable bits, the XXMD bit must be set (= 1) to disable the module.

While the PMD and module enable bits both disable a peripheral’s functionality, the PMD bit completely shuts down the peripheral, effectively powering down all circuits and removing all clock sources. This has the additional effect of making any of the module’s control and buffer registers, mapped in the SFR space, unavailable for operations. In other words, when the PMD bit is used to disable a module, the peripheral ceases to exist until the PMD bit is cleared. This differs from using the module enable bit, which allows the peripheral to be reconfigured and buffer registers preloaded, even when the peripheral’s operations are disabled.

The PMD bit is most useful in highly power-sensitive applications, where even tiny savings in power consumption can determine the ability of an application to function. In these cases, the bits can be set before the main body of the application to remove those peripherals that will not be needed at all.

39.4.2 Selective Disabling of Modules in Idle Mode

To achieve additional power savings, peripheral modules can be selectively disabled whenever the device enters Idle mode. This is done with the Stop in Idle (SIDL) control bit, which is generally located in bit position 13 of the control register of most peripheral modules. The generic name format is “XXXSIDL” (using “XXX” as the mnemonic version of the module’s name, as before). The Stop in Idle feature allows further reduction of power consumption during Idle mode, enhancing power savings for extremely power-critical applications.

Almost all peripheral modules have a Stop in Idle bit, including modules that lack a module enable bit (e.g., input capture and output compare). The Real-Time Clock module is the exception, as it is assumed that an application involving a Real-Time Clock will need to keep the module running continuously.

Table 39-3: Power-Saving Features of Register Map

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	TRAPR	IOPUWR	SBOREN	—	—	DPSLP	—	VREGS/PMSLP	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	xxxx(1)
CLKDIV	ROI	DOZE2	DOZE1	DOZE0	DOZEN	RCDIV2	RCDIV1	RCDIV0	—	—	—	—	—	—	—	—	0300
PMDx	XXMD	XXMD	XXMD	XXMD	XXMD	XXMD	XXMD	XXMD	XXMD	XXMD	XXMD	XXMD	XXMD	XXMD	XXMD	XXMD	0000
DSCON	DSEN	—	—	—	—	—	—	—	—	—	—	—	—	—	DSBOR	RELEASE	xxxx
DSWAKE	—	—	—	—	—	—	—	DSINT0	DSFLT	—	—	DSWDT	DSRTC	DSMCLR	—	DSPOR	xxxx
DSGPR0	Deep Sleep Persistent General Purpose bits																xxxx
DSGPR1	Deep Sleep Persistent General Purpose bits																xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: The RCON register Reset values are dependent on the type of Reset.

39.5 DESIGN TIPS

Question 1: ***What should my software do before entering Sleep, Deep Sleep or Idle mode?***

Answer: Make sure that the sources intended to wake-up the device have their IE bits set. In addition, make sure that the particular source of interrupt has the ability to wake-up the device. Some sources do not function when the device is in Sleep mode.

If the device is to be placed in Idle mode, make sure that the 'Stop in Idle' control bit for each device peripheral is properly set. These control bits determine whether the peripheral will continue operation in Idle mode. See the individual peripheral sections of this manual for further details.

If entering Deep Sleep mode, remember that the SFRs, RAM and program counter will be lost. Be sure to store any relevant device state information in the DSGPRx registers. These are the only SFRs that will retain their value after the device wakes up. The stored data can be used to restore the state of the device.

Question 2: ***How do I tell which peripheral woke the device from Sleep, Deep Sleep or Idle mode?***

Answer: You can poll the IF bits for each enabled interrupt source to determine the source of wake-up. When waking up from Deep Sleep mode, poll the bits in the DSWAKE register and RCON register to determine the wake-up source.

39.6 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Power-Saving Features with Deep Sleep of PIC24F Devices are:

Title	Application Note #
Low-Power Design using PICmicro® Microcontrollers	AN606

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

39.7 REVISION HISTORY

Revision A (January 2009)

This is the initial released revision of this document.