

Computer Science

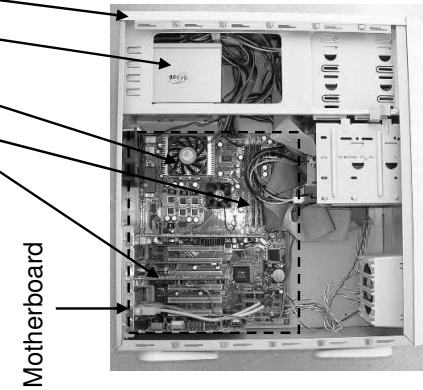
Personal Computer (PC) - Architecture

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Personal Computer - construction

- ◆ Case
- ◆ Power supply
- ◆ Processor
- ◆ Memory
- ◆ Extension cards
 - ◆ Graphic card
 - ◆ Sound card
 - ◆ Network card, etc.
- ◆ Mass storage
 - ◆ Hard drive
 - ◆ Floppy drive
 - ◆ CDROM

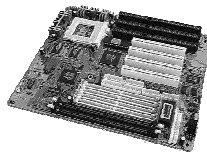


Motherboard, Mainboard

- Mechanical base for computer components such as memory, processor, etc.
- Multilayer (3-7 layers) Printed Circuit Board (PCB)
- Sockets for processor, memory modules, extension cards
- System and external buses
- Set of integrated circuits (*chipset*)
- Read-only memory (ROM) containing boot program (BIOS)
- Nonvolatile RAM memory where computer configuration is stored
- Real Time Clock (RTC)

Electromagnetic interference !

- very high operating frequency
- limitations for length and shape of interconnections
- board screening



Motherboard – evolution

Before ~1993-1995:

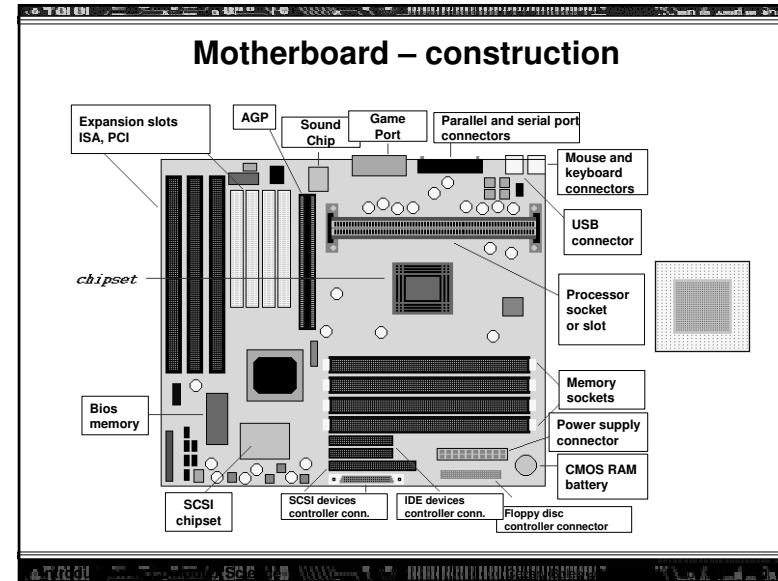
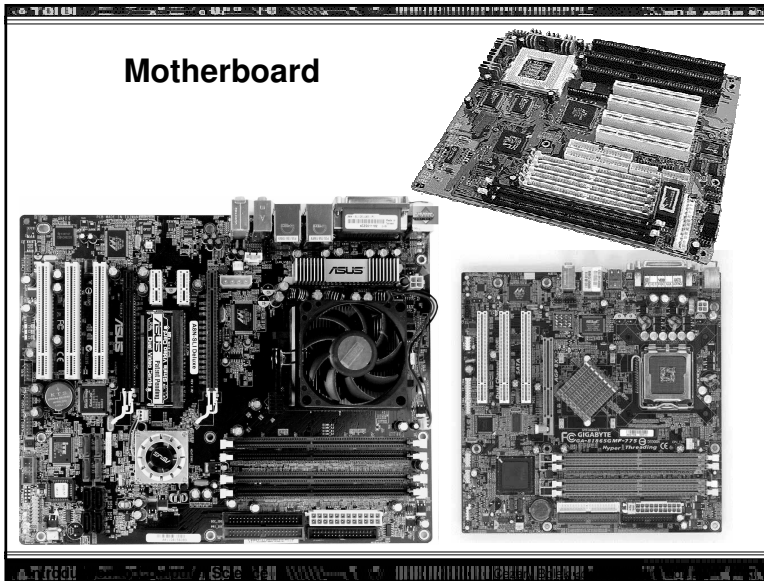
- ◆ only basic components of system (*chipset*+BIOS):
- ◆ *expansion slots* – according to ISA bus standard
- ◆ processor socket (no mechanical insertion support)
 - the oldest DIL (*Dual In Line*)
 - modern: PGA (*Pin Grid Array*)
- ◆ keyboard plug-in sockets
- ◆ memory modules sockets

After ~1993-1995:

- tendency to integrate additional computer components (controllers: in/out, drives, graphics, sound, network)
- new processor sockets: ZIP (*Zero Insertion Force*)
- variety of expansion slots (ISA, PCI, VLB, AGP)

Configuration standards: (*form factor*)

- AT, (babyAT), ATX (microATX max:244x244mm)



BIOS

*Basic Input-Output System
(PC Firmware)*

ROM memory containing startup program which is executed after computer power up.

- Hardware configuration checking (processor type, memory size, extension cards, storage media presence)
- Hardware testing for failure - POST (*Power-On Self Test* + audible diagnostic signals)
- Bootstrap – operating system loading from mass storage system. Data source – fixed in CMOS RAM (hard drive, CDROM, floppy, network)
- BIOS memory in general cannot be changed programmatically what ensures that system will always boot.
- But, usually BIOS is implemented in Flash Memory, what allows periodical changes by reprogramming (*bios upgrade*)

www.wimsbios.com

PnP BIOS

(Plug and Play)

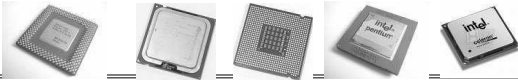
PnP – automatic configuration, selfconfiguration of expansion cards in PC system

- input/output address space fixing
- interrupt number
 - Input/output address space allows exchange data between external device and processor
 - Interrupts – mechanism which allows devices to notify the processor that they need immediate service

For older BIOS all external devices configuration must have been performed manually (card configuration) to avoid hardware conflicts.

Microprocessors

Type	Year	Processor clock	Memory clock	Multiplier	Cache L1	Cache L2 (built-in)	Memory space	Transistors number
8086	1978	4,77-8	4,77-8	-	-	-	1MB	29 tys.
8088	1980	4,77-8	4,77-8	-	-	-	1MB	29 tys.
80286	1982	6-20	6-20	-	-	-	16MB	134 tys.
80386DX	1985	16-33	16-33	-	-	-	4GB	275 tys.
80386SX	1988	16-33	16-33	-	-	-	16MB	275 tys.
80486DX	1989	25-50	25-50	-	8kB	-	4GB	1,2 mln
80486SX	1991	25-50	25-50	-	8kB	-	4GB	1,18 mln
80486DX2	1992	50-80	25-40	2	8kB	-	4GB	1,2 mln
80486DX4	1994	75-120	25-40	3	8KB+8KB	-	4GB	1,6 mln
Pentium	1993	60-200	60-66	1-3	8KB+8KB	-	4GB	3,1 mln
Pentium Pro	1995	166-200	60-66	2,5-3	8KB+8KB	256-512KB	64(4)GB	22 mln
Pentium MMX	1997	166-233	66	2,5-3,5	16KB+16KB	-	4GB	4,5 mln
Pentium II (Klamath)	1997	233-300	66	3,5-4,5	16KB+16KB	512KB (ext)	64(4)GB	7,5 mln
Pentium II (Deschutes)	1998	266-450	66-100	3,5-5	16KB+16KB	512KB (ext)	64(4) GB	7,5 mln
Celeron (Covington) (PII)	1998	266-300	66	4-4,5	16KB+16KB	-	64(4) GB	7,5 mln
Celeron (Mendocino) (PII)	1998	300-533	66	4,5-8	16KB+16KB	128KB	64(4) GB	19,2 mln



Microprocessors

Type	Year	Processor clock	Memory clock	Multiplier	Cache L1	Cache L2 (built in)	Memory space	Transistors number
Pentium III (Katmai)	1999	450-600	100-133	4-6	16KB+16KB	512KB (ext)	64GB	9,5 mln
Pentium III (Coppermine)	1999	500-1000	100-133	4-7,5	16KB+16KB	256KB	64GB	28,1 mln
Celeron II (Coppermine)	2000	533-1300	66-100	8-13	16KB+16KB	128KB	64GB	28,1 mln
Pentium III (Tualatin)	2001	1133-1400	133	8,5-10,5	16KB+16KB	256-512KB	64GB	28,1 mln
Celeron II (Tualatin)	2001	1G-1,4G	100	10-14	16KB+16KB	256KB	64GB	
Pentium M (Banias) (PIII)	2003	1G-1,7G	100 (400)		32K+ 32K	1MB	4GB	77 mln
Celeron M (Banias)	2003	1G-2,2G	100 (400)		32K+ 32K	512KB	4GB	
Pentium M (Dothan) (PIII)	2004	1G-2,2G	100 (400)		32K+ 32K	2MB	4GB	
Pentium M (Yonah) (Dual)	2006	2,13G	166 (667)		32K+ 32K	2MB	4GB	

Type	Core	Clock	FSB	Cache	Additional inf.
	Willamette	1.3-2.0 GHz	100 (400)	L1:8KB+12KB L2:256KB	
P4A	Northwood	1.6-3.0 GHz	100 (400)	L1:8KB+12KB L2:512KB	
P4B	Northwood	2.0-3.06 GHz	133 (533)	L1:8KB+12KB L2:512KB	Hyperthreading for 3.06+ GHz
P4C	Northwood	2.4-3.4 GHz	200 (800)	L1:8KB+12KB L2:512KB	Hyperthreading
P4E/Sx0 series	Prescott	2.8-3.8 GHz	200 (800)	L1:16KB+12 KB L2:1 MB	Hyperthreading, instrukcje SSE3
P4A	Prescott	2.4-2.93 GHz	133 (533)	L1:16KB+12 KB L2:1MB	bez Hyperthreading, instrukcje SSE3
Extreme Edition	Gallatin	3.2-3.4 GHz	200 (800)	L1: 8KB+12 L2:512KB L3:2MB	Hyperthreading, addition of on-die L3 cache
P4F/Sx1 series	Prescott	3.2-3.8 GHz	200 (800)	L1:16KB+12 KB L2:1MB	EM64T (64-bit extension)
6x0 series	Prescott 2MB	2.8-3.8 GHz	200 (800)	L1:16KB+12 KB L2:2MB	EM64T 64-bit extension)
Extreme Edition	Prescott 2MB	3.73 GHz	266 (1066)	L1:16KB+12 KB L2:2MB	
Pentium D	Smithfield	2.8-3.2 GHz	200 (800)	L1:16KB+12KB x2 L2:2MB	Dual Core Processor, EM64T

Microprocessors

- ◆ Pentium Dual Core
 - ◆ 2006
 - ◆ 2 cores, low budget
- ◆ Intel Core 2
 - ◆ 8th generation, 64-bit x86-64 architecture
 - ◆ 2006

Model	Cores no.	Clock	FSB	Multiplier	L2 Cache	QPB	Core
E4200	2	1600 MHz	200	8x	2 MB	800 MHz	Allendale
...							
E4700	2	2600 MHz	200	13x	2 MB	800 MHz	Allendale
E6300	2	1866 MHz	266	7x	2 MB	1066 MHz	Conroe
...							
E6850	2	3000 MHz	333	9x	4 MB	1333 MHz	Conroe
E7200	2	2530 MHz	266	9.5x	3 MB	1066 MHz	Wolfdale
...							
E7600	2	3060 MHz	266	11,5x	3 MB	1066 MHz	Wolfdale
E8190	2	2660 MHz	333	8x	6 MB	1333 MHz	Wolfdale
...							
E8600	2	3330 MHz	333	10x	6 MB	1333 MHz	Wolfdale

Microprocessors

Intel Core 2 Quad

Model	Cores no	Clock	FSB	Multiplier	L2 Cache	QPB	Core
Q6600	4	2394 MHz	266	9x	8 MB	1066 MHz	Kentsfield
Q6700	4	2660 MHz	266	10x	8 MB	1066 MHz	Kentsfield
Q6850	4	2926 MHz	266	11x	8 MB	1066 MHz	Kentsfield
Q7600	4	2700 MHz	200	13,5x	2 MB	1333 Mhz	Yorkfield
Q8200	4	2331 MHz	333	7x	4 MB	1333 Mhz	Yorkfield
Q8300	4	2497 MHz	333	7,5x	4 MB	1333 Mhz	Yorkfield
Q8400	4	2664 MHz	333	8x	4 MB	1333 Mhz	Yorkfield
Q9300	4	2497 MHz	333	7,5x	6 MB	1333 Mhz	Yorkfield
Q9400	4	2664 MHz	333	8x	6 MB	1333 Mhz	Yorkfield
Q9450	4	2664 MHz	333	8x	12 MB	1333 Mhz	Yorkfield
Q9550	4	2830 MHz	333	8,5x	12 MB	1333 Mhz	Yorkfield
Q9650	4	2997 MHz	333	9x	12 MB	1333 Mhz	Yorkfield

Intel Core 2 Extreme

Model	Cores no	Clock	FSB	Multiplier	L2 Cache	QPB	Core
X6800	2	2933 MHz	266	11x	4 MB	1066 MHz	Conroe
QX6700	4	2667 MHz	266	10x	8 MB	1066 MHz	Kentsfield
QX6800	4	2926 MHz	266	11x	8 MB	1066 MHz	Kentsfield
QX6850	4	3000 MHz	333	9x	8 MB	1333 MHz	Kentsfield
QX9650	4	3000 MHz	333	9x	12 MB	1333 MHz	Yorkfield
QX9770	4	3200 MHz	400	8x	12 MB	1600 MHz	Yorkfield
QX9775	4	3200 MHz	400	8x	12 MB	1600 MHz	Harpertown

Microprocessors

- ◆ Intel Core i3
 - ◆ 2010
 - ◆ built in GPU (Graphics Processing Unit), physically separated silicon structure
 - ◆ 2 cores
 - ◆ Direct Media Interface
 - ◆ low end, Core 2 continuation



Codename	Name	Cache L3	Socket	TDP	Multipl.	Clock	I/O Bus
Clarkdale	Core i3-560	4 MB	LGA 1156	73 W	22	3.33 GHz	Direct Media Interface Integrated GPU
	Core i3-550	4 MB	LGA 1156	73 W	22	3.20 GHz	
	Core i3-540	4 MB	LGA 1156	73 W	22	3.06 GHz	
	Core i3-530	4 MB	LGA 1156	73 W	22	2.93 GHz	
	Core i3-6xx	4 MB	LGA 1156	73 W	22	3.33 GHz	
Arrandale	Core i3-350M	3 MB	LGA 1156	35 W	17	2.26 GHz	
	Core i3-370M	3 MB	LGA 1156	35 W	?	2.40 GHz	
	Core i3-330UM	3 MB	LGA 1156	18 W	?	1.20 GHz	
	Core i3-330M	3 MB	LGA 1156	35 W	16	2.13 GHz	
	Core i3-330E	3 MB	LGA 1156	35 W	?	2.13 GHz	

Microprocessors

- ◆ Intel Core i5
 - ◆ 2009
 - ◆ Niektóre posiadają wbudowany układ graficzny
 - ◆ positioned between Core i3 and Core i7



Core i5 model	Cores no (threads)	Core clock (GHz)	Multiplier		Cache	Memory controller	DMI	TDP	Socket	IO Bus
			Min.	Max.						
750	4 (4)	2.66	9	20	32KB (instrukcje) + 32KB (dane) L1 / rdzeń 256KB L2 / rdzeń 8MB L3 dzielonej	2x DDR3-800/1066/1333	2.5GT/s (GigaTransfers)	95 W	LGA 1156	DMI
Seria 600	2 (4)	3.2 – 3.46 733 – 900 MHz	9	25	32KB L1-32KB L1/rdzeń 256KB L2/rdzeń 4MB L3 dzielonej			73 – 87 W		DMI, zintegrowane GPU

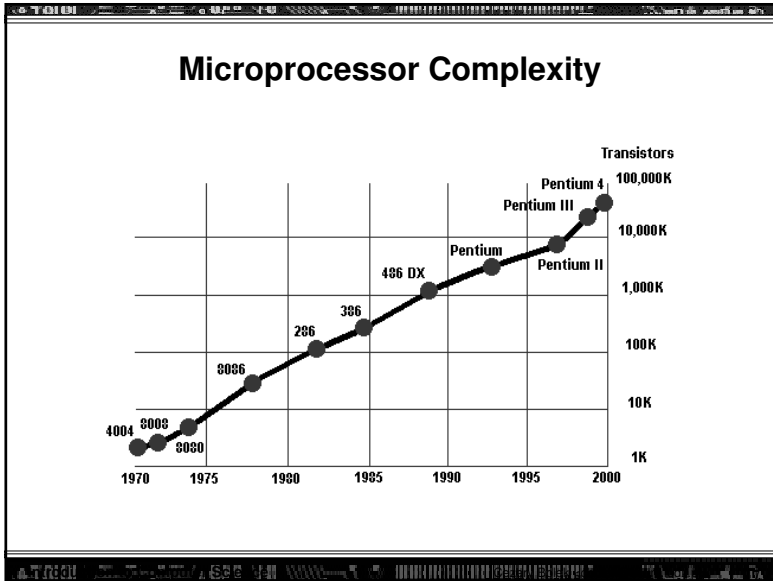
Microprocessors

- ◆ Intel Core i7
 - ◆ Cache
 - ◆ L1: 32KB for instructions L1 and 32KB for data per each core
 - ◆ L2: 256KB instructions/data shared per each core
 - ◆ L3: 8MB shared
 - ◆ Hyper-Threading technology
 - ◆ Built in memory controller DDR3, IMC (Integrated Memory Controller)
 - ◆ New system bus, QPI (QuickPath Interconnect)
 - ◆ DMI (Direct Media Interface)
 - ◆ New SSE4 instructions
 - ◆ Socket LGA 1366 or LGA 1156



Microprocessor - Trends

- Increase clock speed of processor and memory
- Increase width of data and address buses
- Evolution of instruction sets, main unit and Floating Point Unit (FPU) - coprocessor
- Low cost versions of existing processors (SX, Celeron, Duron, ...)
- Increase size of cache memory – internal (L1) and external (L2 & L3)
- Advanced architectures: superscalar, pipelining, chaining, multithreading, ...
- GPU, memory controller integration
- Specialized instruction sets: MMX, SSE, 3DNow, ...



Processor sockets

- Socket must conform processor terminals and packaging
- Efficient carrying of heat by radiator
- Passive cooling system: radiator + fan
- Radiator: base (copper, aluminum, ceramics) + ribbing
- Advanced, active cooling systems: water, electric (Peltier), cryogenic.

Processor Socket Evolution

	Socket 1	169-terminals	486 processors (supply voltage 5V and versions DX2, DX4, OverDrive)	
	Socket 2	238-terminals	Socket 1 modification for 486 processors	
	Socket 3	237-terminals	Last socket for 486, supply voltage 5V and 3.3V	
	Socket 4	273-terminals	Socket for first Pentium processors 60/66 MHz, 5V	
	Socket 5	320-terminals	Socket for Pentium 75/133 MHz, 3.3V	
	Socket 6	235-terminals	Socket 3 extension for 486, very rare	
	Socket 7	321-terminals	Very popular socket for Pentium MMX and clones, dual voltage	
	Socket 8	387-terminals	Socket for Pentium Pro only	
	Slot 1	242-terminals	For Pentium II, III and Celerons, L2 cache memory in processor cartridge	
	Slot 2	330-terminals	For Pentium II, III and Xeon with bigger cache memory	

Microprocessor Sockets Evolution

Slot A	242-terminals	Mechanically identical to Slot1 but electrically different, for AMD Athlon processors	
Socket 370	370-terminals	Slot 1 replacement for new Pentium II, III and Celeron	
Socket 423	423-terminals	For Pentium 4, better heat dissipation and more efficient cooling systems	
Socket A	462-terminals	For newer AMD Athlon, Athlon XP and Duron with bigger cache memory	
Socket 478	478-terminals	Smaller version of 423 for newer Pentium 4 processors	
Socket 603	603-terminals	For Pentium 4 Xeon with bigger cache memory, multiprocessor support	
Socket 754	754-terminals	Socket for new AMD Athlon 64 processors	
Socket 940,939	939-terminals	Improved socket for new Athlon 64 and Opteron processors	
Socket 775 (LGA775, T)	775-terminals	Socket for newest Pentium 4, P4EE, Celeron (Prescott i Smithfield core)	

Processor sockets

◆ LGA 775 (Socket T)

◆ Wolfdale codename:

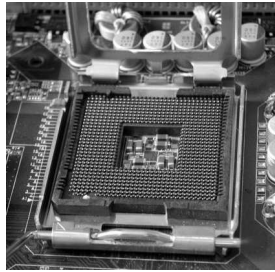
- ◆ Core 2 Duo (E7200, E7300, E7400, E7500, E7600, E8200, E8400, E8500, E8600, E8700)
- ◆ Intel Pentium Dual Core (E5200, E5300, E5400, E5500, E5700, E6300, E6500, E6500K, E6600, E6700, E6800)

◆ Conroe codename :

- ◆ Core 2 Duo (E4500, E6300, E6320, E6400, E6420, E6500, E6600, E6700, Extreme Edition)
- ◆ Pentium Dual Core (E2140, E2160, E2180, E2200)

◆ Kentsfield codename :

- ◆ Intel Core 2 Quad (QX6600)



Ewolucja gniazd procesora

◆ LGA 1156 (Socket H)

◆ Lynnfield codename

- ◆ Core i5 i5-7xx
- ◆ Core i7 i7-8xx, i7-2600
- ◆ Xeon L34xx, X34xx

◆ Clarkdale codename

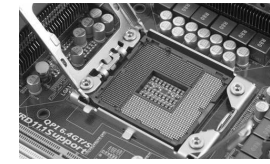
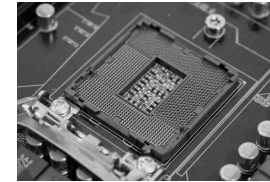
- ◆ Pentium G6xxx
- ◆ Core i3 i3-5xx, i3-6xx, i3-3xx
- ◆ Core i5 i5-6xx

◆ Arrandale codename

- ◆ Core i3 i3-350M, i3-370M, i3-330UM, i3-330M, i3-330E

◆ LGA 1366 (Socket B)

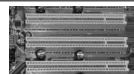
- ◆ Core i7 i7-9xx
- ◆ Xeon 5500 series



Input/Output Buses

- I/O buses are interfaces between computer system and devices located on expansion cards.
- Construction of motherboards, processors and memory chips changes fairly often, but I/O interfaces relatively rarely. This allows to use typical expansion cards in every PC computer.
- ISA (*Industry Standard Architecture* 1982) – the oldest, clock speed 4.77 i 8MHz, max. transfer speed 8MB/s (not enough for graphic cards, hard drives, network),

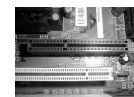
- PCI (*Peripheral Component Interconnect* 1993) – universal and efficient, clock speed 33,66MHz, max. data transfer speed 266MB/s, support for PnP,



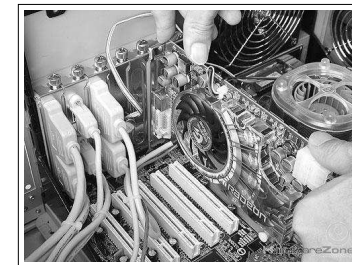
- PCI-Express (PCIe, PCI-E 2003) – universal, efficient serial bus, clock speed 2.5 GHz, max. transfer speed 250MB/s (per line)



- AGP (Accelerated Graphics Port) – efficient local bus optimized for graphic cards controllers, max. transfer speed up to GB/s, clock speed = 1x, 2x, 4x, 8x *frontside bus*,



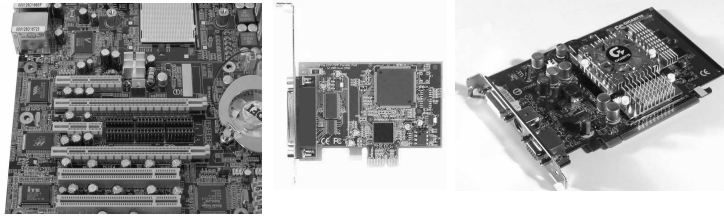
AGP Bus



AGB Bus controller is connected to System Bus, what offers high speed data transfer between:

- AGP graphic card and processor
- AGP graphic card and RAM memory

PCI Express Bus



- very high data transfer speed – serial architecture
- *point-to-point* connection
- possibility to plug/unplug cards during computer work (*hot plug/swap*)
- target – to eliminate other I/O buses
- introduced in 2003, first computers equipped with PCI Express: 2004

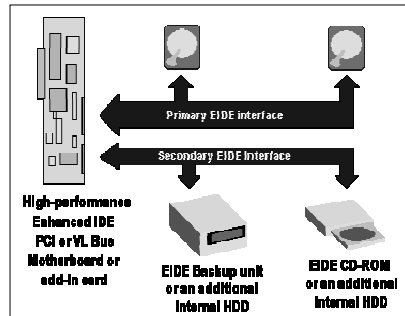
PCIe	Speed
x1 (2004)	250 MB/s
x2 (2004)	500 MB/s
x4 (2004)	1000 MB/s
x8 (2004)	2000 MB/s
x16 v. 1.0 (2004)	4 GB/s
x16 v. 2.0 (2007)	8 GB/s
x16 v. 3.0 (2011)	16 GB/s

Hard Disc Interfaces

- IDE (Integrated Drive Electronics) – hardware solution for data transfer to/from hard drive
- Data exchange protocol (interface) for IDE devices: ATA (AT Attachment)
- IDE device controllers with ATA interface are connected to I/O buses: ISA, VL-Bus or PCI (presently)
- IDE architecture allows to connect only 2 hard drives, maximum storage capacity 528MB per drive, data transfer speed 3MB/s – limitation, bottleneck for mass storage systems

EIDE Standard

Enhanced IDE



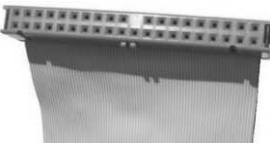
- 4 IDE devices:
- *two channels*
 - *master-slave*

- faster data transfer up to 16MB/s (ATA-2 1994)
- max. disc capacity 8.4GB and (1998) 137GB
- support for other devices (CD-ROM) – extension ATA to ATAPI
- support for Direct Memory Access (DMA)

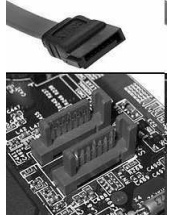
And faster... Ultra ATA

- ATA 3 (1996) – SMART (Self-Monitoring Analysis and Reporting Technology)
- ATA 4 (1997, Ultra ATA) – data transfer speed 33MB/s (ATA 33), support for error correction CRC (*Cyclical Redundancy Check*), ATAPI integration
- ATA 5 (1999) – data transfer speed 66MB/s (ATA 66), new 80-wire connecting tapes (so far 40-wire)
- ATA 6 (2000) – data transfer speed 100MB/s (ATA 100) (2001) – speed 133MB/s (ATA 133)

Serial ATA



Parallel ATA



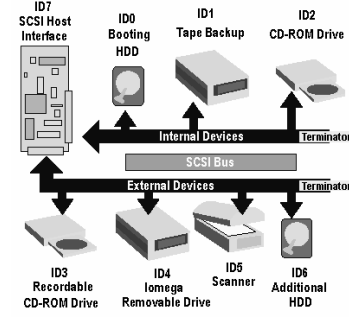
Serial ATA

- Lower signal voltage (0.5V)
- Longer connecting tapes (up to 1m), less wires per tape
- Efficient error correction
- Hot-plug
- Generations:
 - SATA revision 1.0 (SATA 1.5 Gbit/s) – transfer 150 MB/s (2002)
 - SATA revision 2.0 (SATA 3 Gbit/s) – transfer 300 MB/s
 - SATA revision 3.0 (SATA 6 Gbit/s) – transfer 600 MB/s (2009)

- eSATA – external SATA, for external mass storage systems, cable length up to 2m
- xSATA – longer cables, up to 8m, shielded cables
- mSATA – mini SATA (revision 2)

SCSI Interface

- Communication interface for external devices, developed for efficient, high-end computers (1986).
- 8 devices can be attached to single SCSI adapter. System can have many SCSI adapters.
- Long connection cable (up to 12m)
- Application: servers, efficient computer systems
- Many versions:
 - FastSCSI,
 - FastWideSCSI
 - UltraSCSI
 - UltraWideSCSI,
 - Ultra2
 - Ultra3
 - Ultra4 SCSI
 - Ultra 640 SCSI – transfer 640MB/s



The diagram illustrates a SCSI bus architecture. At the top left is the 'ID7 SCSI Host Interface'. A horizontal 'SCSI Bus' connects it to various devices. 'Internal Devices' include ID0 Booting HDD, ID1 Tape Backup, and ID2 CD-ROM Drive. 'External Devices' include ID3 Recordable CD-ROM Drive, ID4 Iomega Removable Drive, ID5 Scanner, and ID6 Additional HDD. Terminators are shown at both ends of the bus.

Parallel and Serial Ports

Legacy ports

Standard for over 20 years with no modifications !!!

Serial Port:

- data transfer speed 115Kb/s (~12kB/s) – sufficient only for very slow devices: modem, mouse
- simple data transmission protocol, long connection cables (few meters)
- necessity of using computer hardware resources (interruptions)

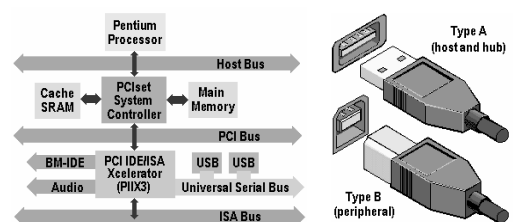
Parallel Port:

- data transfer speed ~60KB/s – not enough for most multimedia devices
- problems when connecting many devices do single port
- simple, dual direction data transmission protocol
- short connection cables (1.5 m)
- necessity of using computer hardware resources (interruptions)

USB Interface

Universal Serial Bus

- Universal communication standard for external I/O devices, full support for PnP, support for *hot-plug*
- Up to 127 devices can be connected at a time: serially or via hub
- USB connector has 5V power supply lines, that can be used for supplying external low power consumption devices (0.5A)
- Maximum data transfer speed 12Mbit/s (~1MB/s USB 1.1) and 480Mbit/s (USB 2.0)
- Speed:
 - USB 1.1 12Mbit/s (~1.5MB/s)
 - USB 2.0 (Hi-Speed) 480Mbit/s
 - USB 3.0 (SuperSpeed) 4.8Gbit/s
- Cable length 5m

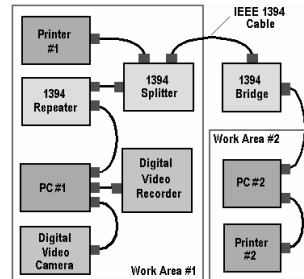
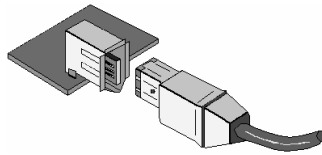


The diagram shows a system architecture with a 'Pentium Processor' connected to 'Cache SRAM', 'PCISet System Controller', and 'Main Memory'. Below the processor, various buses are shown: 'Host Bus', 'PCI Bus', 'Audio', 'BM-IDE', 'PCI IDE/ISA Xcelerator (PIIX3)', 'USB', and 'ISA Bus'. To the right, two USB connectors are shown: 'Type A (host and hub)' and 'Type B (peripheral)'.

IEEE1394 Interface

FireWire - Apple

- Interface dedicated to high speed multimedia equipment, sound and video, philosophy similar to USB
- Cable length up to 4.5m, for bigger length *repeater is needed*
- 63 devices can be connected at a time, serially
- High data transfer speed 400Mbit/s (~50MB/s)
- Flexible configuration
- *Hot-Plug* support



Memory Systems in PC

Memory Efficiency Progress

- Processor efficiency doubles: every 18 month
- Memory efficiency doubles: every 7 years

Memory efficiency is understood as:

- speed
- capacity

Memory speed, two parameters:

- **Memory access time:** transfer time of basic portion of data between memory and processor
- **Memory cycle time:** minimal time between read/write operations from/to same memory cell

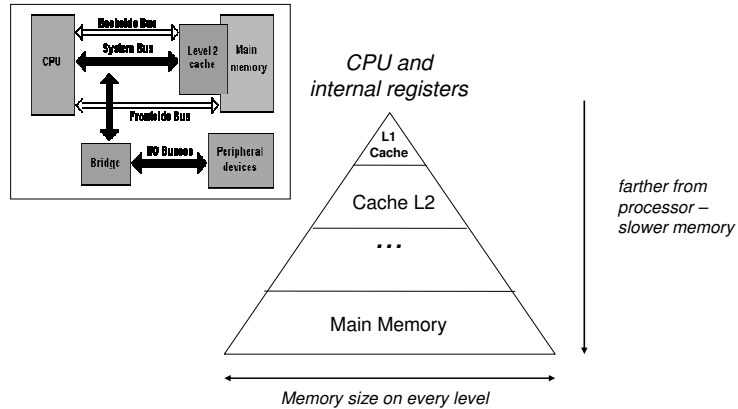
Memory – Computer System Bottleneck

How to solve the problem of slow memory subsystem ?

- using very fast StaticRAM memory modules –very expensive solution, high power consumption. Only for high-end, expensive computer systems;
- using slow DRAM memory modules improving methods of data transfer: wide buses, block transfers;
- using the combination of slow and cheap DRAM memory (main memory) and fast StaticRAM (support memory). Such memory subsystem should be organized the way to optimize data transfer that mostly takes place between processor and fast, support memory – Cache Memory.

Modern, efficient memory system must have hierarchical organization!

Hierarchical Memory Organization



Main Memory

- Always *Dynamic* RAM, communication with processor via system bus or *frontside bus*
- All Pentium processors (after 1993) have data bus width = 64bits (8 bytes)

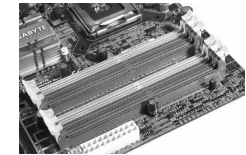
DRAM	– 4.77-40MHz
Fast Page Mode DRAM	– FPM DRAM (16-66MHz)
Extended Data Out DRAM	– EDO DRAM (33-75MHz)
Burst Extended Data Out DRAM	– BEDO DRAM (60-100MHz)
Synchronous DRAM	– SDRAM (100,133MHz)
Double Data Rate DRAM	– DDR DRAM (200, 266, 333MHz, ...)
DDR2	
DDR3	

DDR1-3 SDRAM

	Standard name	Memory clock	Cycle time	I/O Bus clock	Data transfers per second	JEDEC standard VDDQ voltage	Module name	Peak transfer rate
DDR1	DDR-200	100 MHz	10 ns ^[1]	100 MHz	200 Million	2.5v +/- 0.2v	PC-1600	1600MB/s
	DDR-266	133 MHz	7.5 ns	133 MHz	266 Million	2.5v +/- 0.2v	PC-2100	2100 MB/s
	DDR-300	150 MHz	6.67 ns	150 MHz	300 Million	Not a JEDEC standard	PC-2400	2400 MB/s
	DDR-333	166 MHz	6 ns	166 MHz	333 Million	2.5v +/- 0.2v	PC-2700	2700 MB/s
	DDR-400	200 MHz	5 ns	200 MHz	400 Million	2.6v +/- 0.1v	PC-3200	3200 MB/s
	Standard name	Memory clock	Cycle time	I/O Bus clock	Data transfers per second	Module name	Peak transfer rate	
DDR2	DDR2-400	100 MHz	10 ns	200 MHz	400 Million		PC2-3200	3200 MB/s
	DDR2-533	133 MHz	7.5 ns	266 MHz	533 Million		PC2-4200 PC2-4300 ¹	4266 MB/s
	DDR2-667	166 MHz	6 ns	333 MHz	667 Million		PC2-5300 PC2-5400 ¹	5333 MB/s
	DDR2-800	200 MHz	5 ns	400 MHz	800 Million		PC2-6400	6400 MB/s
	DDR2-1066	266 MHz	3.75 ns	533 MHz	1066 Million		PC2-8500 PC2-8600 ¹	8533 MB/s
	Standard name	Memory clock	Cycle time	I/O Bus clock	Data transfers per second	Module name	Peak transfer rate	
DDR3	DDR3-800	100 MHz	10 ns	400 MHz	800 Million		PC3-6400	6400 MB/s
	DDR3-1066	133 MHz	7.5 ns	533 MHz	1066 Million		PC3-8500	8533 MB/s
	DDR3-1333	166 MHz	6 ns	667 MHz	1333 Million		PC3-10600	10667 MB/s ^[1]
	DDR3-1600	200 MHz	5 ns	800 MHz	1600 Million		PC3-12800	12800 MB/s

Memory Modules

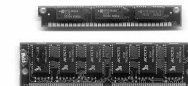
(the most popular)



- DIP (*dual inline package*) – DRAM, oldest type of modules, computers with processors 8086, 80286



- SIMM (single inline memory module) – FPM, EDO for processors 386 (30 terminals modules, 16 bit), 486 (72 terminals modules, 32 bit), Pentium (72 terminals modules, 32 bit, used in pairs)



- DIMM (dual inline memory module) – for computers with Pentium II and MMX (100 terminals modules, FPM, EDO) and newer (168 terminals modules, 64 bit, SDRAM, DDR RAM)



- SO-DIMM (Small Outline DIMM) – for laptop computers, 72 or 144 terminals (32 or 64 bit)

Flash Memory

- Nonvolatile semiconductor memory (EEPROM technology)
- Compromise between ROM and RAM memory, perfect for portable computers: Palmtop, DigiCam, etc...
- Significantly slower than typical computer memory systems, (write cycles), not suitable (for now) as main computer memory
- Limited number of write cycles (hundreds of thousand)
- Application: BIOS memory in PC, configuration memory for extension cards, external storage systems (PenDrive, SmartMedia, CompactFlash,...)

Moore's Law

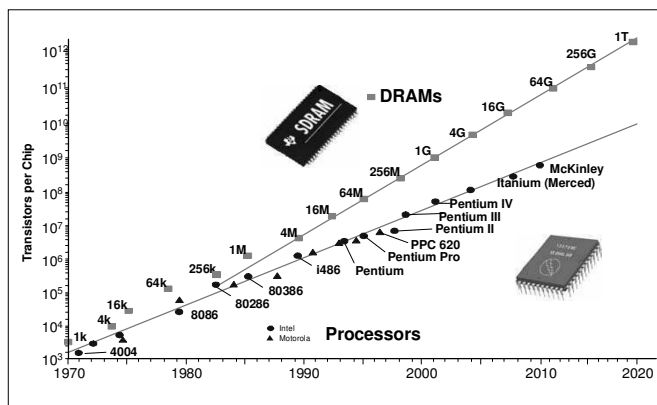
Gordon E. Moore, 1965. "Cramming more components onto integrated circuits," *Electronics*, v.38, no 8 (19 April),

- ◆ Exponential increase in the number of components on a chip
- ◆ Doubling of number of transistors on a chip every 18 months (1980s)
- ◆ Doubling of microprocessor power every 18 months (1990s)
- ◆ Computing power at fixed cost is doubling every 18 months (1990s)

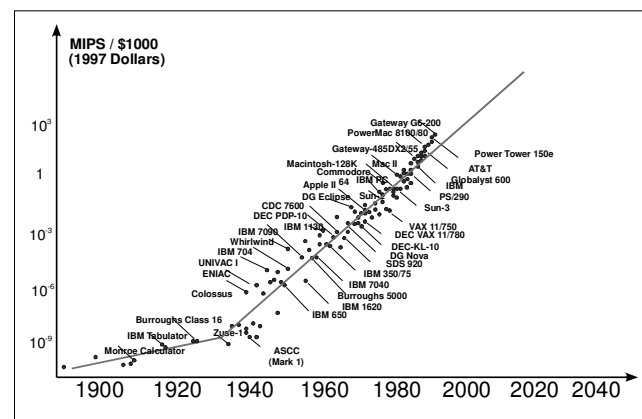
Throughput of integrated circuits, in MIPS, will be doubled every 18 months with cost of decrease by 50%, and this regularity will remain correct for several decades.

(MIPS -millions of instructions per second)

Memory and Processor Complexity Progress



Evolution of Computer Power/Cost



Memory Cost

