Mid Sweden University
The Department of Information Technology and Media (ITM)
Author: Anil Kumar Makineni
E-mail address:anma1003@student.miun.se
Study programme: Masters programme in Electronics design,120 points
Examiner: Docent Goran Thungstrom, goran.thungstrom@miun.se
Tutors: Hussain Mazhar, mazhar.hussain@miun.se
Scope: 6921 words inclusive of appendices
Date: 2012-09-18

M.Sc. Thesis project report
within Electrical Engineering, EL007A, 30 points

Construction and realisation of measurement system in a radiation field of 10 standard suns

Anil Kumar Makineni

Abstract

A measurement system is to be presented, which is used to obtain the *I-V* characteristics of a solar cell and to track its temperature during irradiation before mounting it into a complete array/module. This project presents both the design and implementation of an Electronic load for testing the solar cell under field conditions of 10000 W/m^2, which is able to provide current versus voltage and power versus voltage characteristics of a solar cell using a software based model developed in LabVIEW. An efficient water cooling method which includes a heat pipe array system is also suggested. This thesis presents the maximum power tracking of a solar cell and the corresponding voltage and current values. In addition, the design of the clamp system provides an easy means of replacing the solar cell during testing.

Keywords: Solar cell, Metal Oxide Semiconductor Field Effect Transistor (MOSFET), *I-V* characteristics, cooling system, solar cell clamp system, LabVIEW, Graphical User Interface (GUI).

Acknowledgement/foreword

Special thank goes to my helpful supervisors, Goran Thungstrom and Hussain Mazhar for their guidance in this research and also for providing me with the opportunity to pursue my Masters studies at Mid Sweden University, Sundsvall,Sweden.

I would also like to thank my parents, Indian students, Sundsvall SAI community, Mid Sweden University ITM staff for their kind support and motivation during my studies.

Table of Contents

1 Introduction

Today an important scientific means of taking advantage of solar energy involves the use of the photovoltaic technology. Fossil fuels are non-renewable energy sources which are limited in supply and will soon become depleted. In coming years, renewable energy sources will play a vital role for the generation of electric power. In relation to near loads such as street lights and household purposes solar energy is used as Distributed Resources (DR). Photo Voltaic systems are suitable as *DR* [1]. A clean, quiet and reliable means of generating electricity is possible by using Photo voltaic systems yet they have limitations in relation to generating electric power due to varying field conditions. Thus, a measurement system must be developed and constructed which optimizes the maximum power available from the solar panels. During this operation several parameters are considered including solar radiation, operating conditions in the field, Maximum Power Point Tracking (MPPT) etc. Operating under certain conditions in the field involving either one standard sun or 10 standard suns for solar panels produces Current versus Voltage *(I-V)* characteristics. It is difficult to track the characteristics of PhotoVoltaic (PV) cell in either individually or in group because of rapid and randomly varying field conditions. To overcome such a constraint, placing a variable load and testing the whole system in a short period of time from the open circuit *(Voc)* to short circuit *(Isc)* is possible using a linear MOSFET as an electronic load. The main advantage of using a linear MOSFET as an electronic load for testing PV cell is based on its rapid variation of the equivalent load resistance [2]. Under certain field conditions one has to keep on tracking temperature during irradiation as it will affect the maximum power of the PV cell [7]. In this regard, the suggestion is to use a cooling system, which is a type of heat pipe array with a good contact with the solar panel, uniform temperature distribution and moreover with high heat transfer efficiency. Under different illumination conditions a solar cell displays complex behaviour with regards to the relation between solar irradiation, temperature and total resistance [15]. This leads to a non linear output efficiency which must be investigated before installation of complete module or array.

1.1 Background and problem motivation

This project supports research in relation to the characterization of solar cells used for the production of energy in concentrated solar receivers. To achieve sufficient voltage in the production of electrical energy the solar cells are connected in series. When solar cells are connected in series and additionally if one of the solar cells has reduced its sensitivity, sufficient voltage will not be produced for the production of electrical energy. Therefore the effect on the entire cell system would be a limit of the maximum current and in that case the solar cell must be tested before mounting it in a complete module/ array.

1.2 Overall aim / High-level problem statement

A measurement system should be designed and implemented to observe *I-V, P-V* characteristics and temperature during the irradiation of a solar cell. The monitoring of the voltage, current and temperature in addition to controlling the load of a solar cell using LabVIEW is to be implemented.

2 Theory

2.1 Introduction to PhotoVoltaics

A clean, quiet and reliable method to generate electricity is possible by using Photo voltaic systems. The Photo voltaic effect is defined as generation of electric power by the conversion of solar radiation into direct electric current with the assistance of semiconductors. Photo voltaic cells are often called as solar cells as because the Sun is the source of light and where the photo means light and voltaic means producing electricity. Power generation by the photovoltaic effect is performed by solar panels which consist of a number of solar cells that contains photo voltaic material. PhotoVoltaics are widely used for low power applications [3]. There are many types of PhotoVoltaic systems depending on the applications. Stand-alone PV systems are used in remote areas which are independent of AC grid systems and for low power applications such as a battery bank and street lights. Hybrid PV systems consist of PV array system and other types of energy source including water or wind. These hybrid PV systems are used over long periods of time and are providing the average energy requirements from the PV array system and battery bank. When the weather conditions are sufficiently poor,an auxiliary power supply is used. Another type involves a grid connected power systems which consist of PV arrays that are generally connected to an inverter and a power grid. In this case the PV array DC flows to the inverter which then flows to the power grid [7]. Using PV cells the main advantages are involved in the designing and installing of a new system over a short period of time, noise free, highly mobile and high power capacity per unit weight [22].

2.2 Physical characteristics

Figure (1) shows the basic construction of PhotoVoltaic cell made from a P-type material (boron-doped silicon) and an N type material (phosphorous –doped silicon) both of which are semiconductor materials. When light penetrates through the solar cell, absorption of photons from the light occurs by means of the semiconductor atoms in which the free electrons from the N-type layer flow back to the P-type layer through an external circuit producing the electric current [3]. Figure (2) shows the solar cell made from a mono crystalline silicon wafer. Interconnection of individual photovoltaic cells increases the generation of electric power and where the cells are sealed with a weather proof package called a module. Depending on the desired mode of operation and regardless of the amount of electric power the modules are connected in series and parallel which can be called a PV array as shown in figure (3).

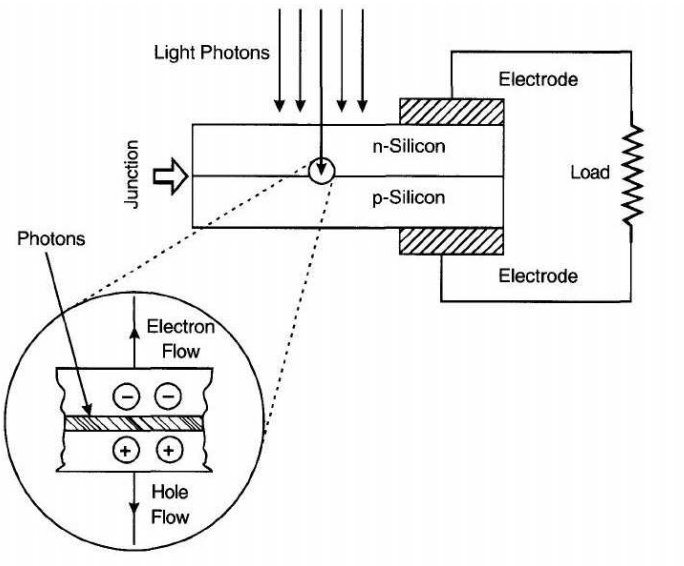


Figure 1: Basic Solar cell construction [7].

Figure 2: Solar cell made from mono crystalline silicon [20]

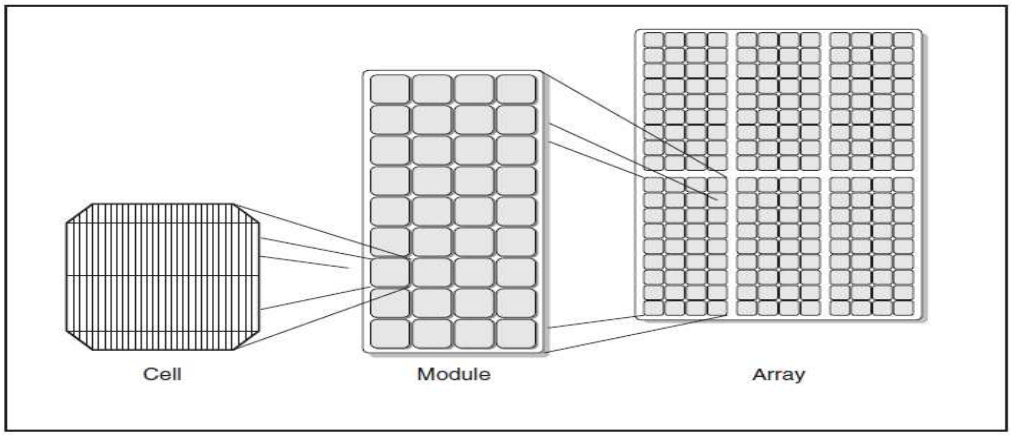


Figure 3: Building of photovoltaic cells, modules and arrays depending on application [3][4].

At the present time, the majority of the PV cells are silicon based and are made of semiconductor materials. Many PhotoVoltaic materials are available in the market with the major ones being crystalline and thin film materials. These differ from each other in relation to light absorption efficiency, energy conversion efficiency, manufacturing technology and cost of production [4]. Single crystal silicon, poly crystal silicon and Gallium Arsenide (GaAs) coms under the crystalline type of materials. Amorphous Silicon (a-Si), Cadmium Telluride (CdTe), Copper Indium Diselinide (CulnSe2, or CIS) comes under the thin film materials. This is important when considering the conversion efficiency of the materials, as for a given area of exposure to the sunlight the more the conversion efficiency the more electricity is generated. Due to the material cost and manufacturing benefits of Amorphous Silicon (a-Si) and because it has a high light absorptivity which is 40 times greater than that for crystalline materials, Amorphous Silicon (a-Si) is widely used from an industrial point of view. However there are other factors to be considered when using a-Si in relation to its conversion efficiency of about 9% and its reliability is also be considered as the system efficiency degrades by 10-15% after several months of exposure to sunlight [4].

2.3 Electrical characteristics

A p-n junction solar cell principle of operation is illustrated as shown in Figure 4. When the incident light falls on the device, the light photons of certain wavelengths are absorbed by the semiconducting material and as a result charge carriers, electrons and holes are generated. A strong electric field exists when these carriers penetrate through to the junction. An electric current in the external circuit is produced when holes and electrons are separated by the electric field. This electric current, which is also called a photocurrent depends on the incident photon intensity and the nature of the semiconductors that form the junction device [7].

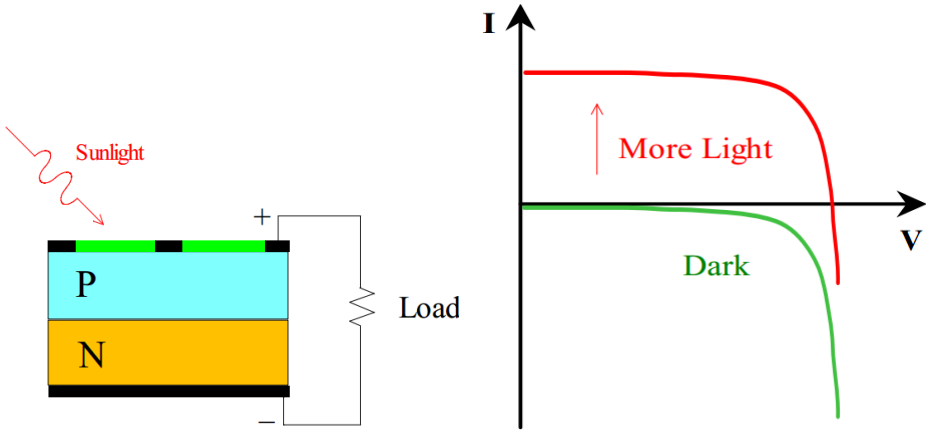


Figure 4: Electrical diagram of a PV cell and associated *I-V* curve [21][5].

Figure 4 shows an Electrical diagram of a solar cell and its *I-V* behaviour with no incident light. When under illumination, an electric current flow as a reverse diode current that linearly depends on the intensity of incident the light [22]. As the diode saturation current varies with changes in temperature, this must also be taken into account. No electric current flows through the diode without illumination unless an external potential is applied. As observed in the *I-V* graph with incident light, this indicates that there is an electric current flowing from solar cell to load [21].

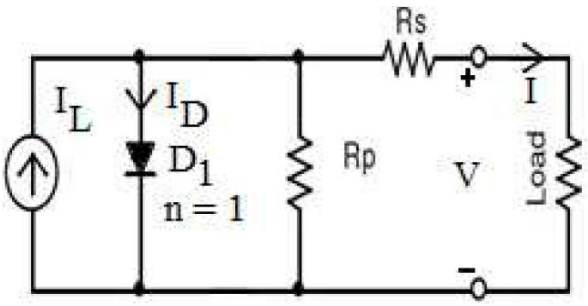


Figure 5: Equivalent circuit model for photovoltaic cell [7].

Figure 5 represents the equivalent circuit of a photo electric cell. *IL* represents the generated photo electric current. The diode and resistance *Rs* comes under the internal electrical losses [22].
The current *I* produced is calculated by applying Kirchoff's law to the node of the circuit as shown in figure 5 which is written as equation (1).
*I= IL-ID*_____ *(1).*
By using the Shockley equation the diode current ID is given as equation (2).

$$ID = Io[\exp(\frac{q(V + IRs)}{\mathrm{KTc}}) - 1] \text{ \_\_\_\_\_(2)}$$

IL is the photo electric current and *ID* is the diode current. *V* represents the output voltage [V] and I0 represents the saturation diode current [A]. In this case, the Rs is the series resistance of the cell [Ω]. *Q* is the electric charge (1.602*10-19C). *K* is the Boltzmann's constant (1.381*10-23K). *Tc* is the cell temperature [K].

By substituting equation (2) above into equation (1), the resulting equation (3) represents the *I-V* cell characteristics under generic radiation and temperature conditions [22].

$$I = IL - Io[\exp(\frac{q(V + IRs)}{\mathrm{KTc}}) - 1] \text{\_\_\_\_\_(3)}$$

The power output becomes zero when the terminals of the junction are shorted. For maximum power *Pmax* is observed with an optimum value by adjusting the Load [7]. The conversion efficiency under specified conditions is given by

$$\eta = \left(\frac{\text{output at optimum operating point)}}{\text{(Energy input to junction)}} * 100 \right) \_\_\_\_\_ (4)$$

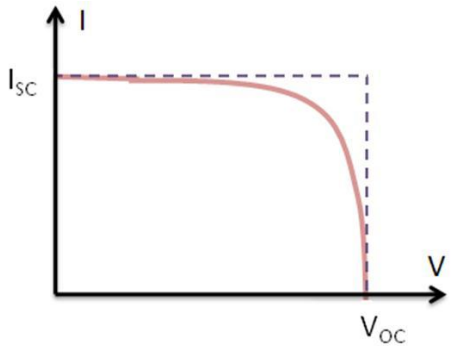


Figure 6: *I-V* curve of a PV cell [5].

Figure 6 shows the *I-V* curve of an illuminated Photovoltaic cell in which the voltage from zero to *Voc* is swept across the load.

Isc= Short circuit current at zero voltage
at low impedance.
Voc=Open circuit Voltage at no current

The *I-V* curve shows two important parameters, which are the short circuit (Isc) and open circuit voltage (Voc). When the voltage across the solar cell is zero, the current through the solar cell is the short circuit current *Isc* which depends on which side of the junction, the light is incident. Open circuit voltage *Voc* results when the load is an open circuit, and the corresponding *Vout* is *Voc*. The short circuit current *Isc* is proportional to the photon flux and is also a function of the cell design. At the optimum operating point *Pmax*, *Isc* and *Voc* are related to the output power [7].

*Pmax= Isc*Voc*FF*_____ *(5)*, where FF is the fill factor.

Fill factor is defined as the Voltage *Vm* and Current *Im* at the optimum operating point to *Voc* and *Isc* and is written as equation (6).

$$FF=\frac{Vm*\mathrm{Im}}{Voc*Isc} \quad \text{(6)}.$$

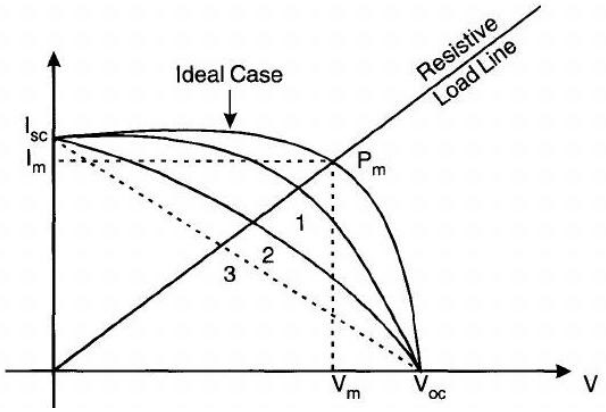


Figure 6: *I-V* curves, 1, 2, 3 *Rs* increasing [7].

The resistive mechanisms and shunt paths plays a significant role for the actual operation of the p-n junction solar cell. The Fill factor and *Pmax* will be decreased with decrease in *Rsh* and an *increase* in *Rs.* A drop of *Voc* is generally more with a significant reduction in *Rsh* and an increase in *Rs* and this causes the *Isc* to drop more as shown in figure 6 [7]. Therefore this results in a current voltage characteristic which departs from the ideal.

The efficiency of a solar cell is given as $\eta=\frac{Voc*Isc*FF}{Incidentsolarpower}$ *(7)*

The conversion efficiency of a solar cell in practice is calculated under Standard Test Conditions (STC). The irradiance of the incident light in W/m^2 or the suns irradiance 1000 W/m^2 is multiplied by the surface area of solar in m^2. The temperature of solar cell during measurement is 25^{o}C [7].

The efficiency of the PV cell also depends on internal resistance of the circuit, *Rsh* and *Rs*. The effect of the internal resistances on the *I-V* curve is shown in figure 8 and 9.

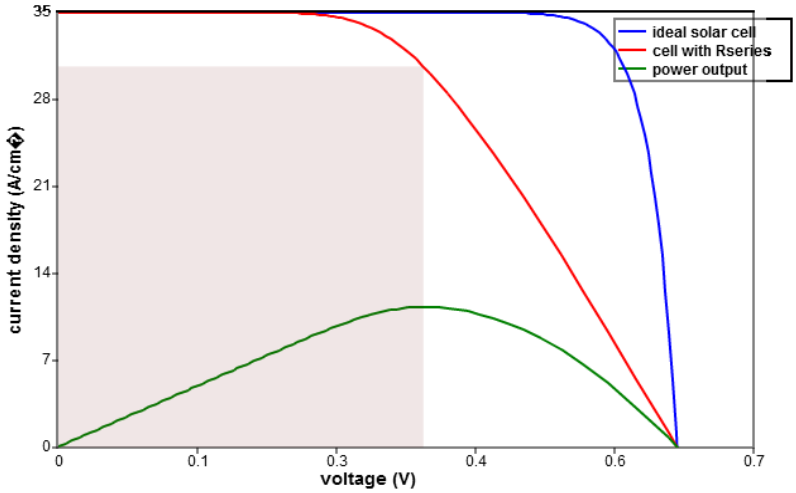


Figure 8: Variation of *I-V* curve with effect of *Rs* from an ideal *I-V* curve [24].

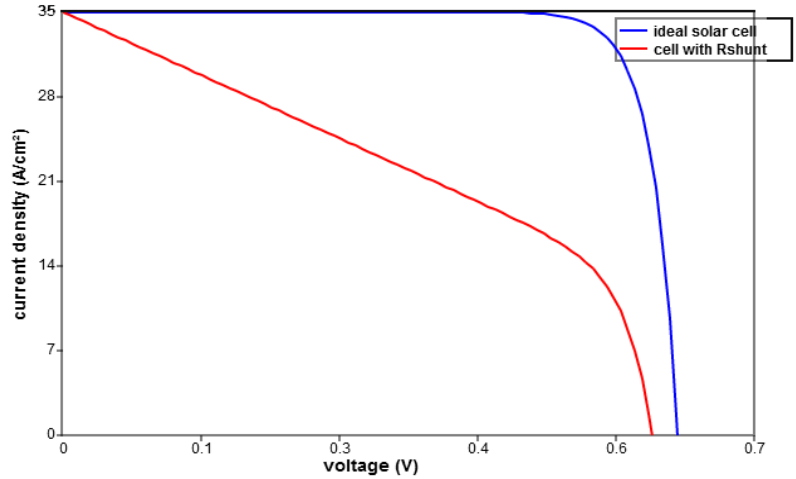


Figure 9: Variation of *I-V* curve with effect of *Rsh* from an ideal *I-V* curve [25].

The red curve represents the ideal *I-V* curve whereas the blue color represents the change in the *I-V* curve with respect to changes in *Rs* and *Rsh*. The causes of series resistance in a solar cell are the current movement through the emitter and base of the solar cell, the contact resistance between the metal contact and the Silicon and most importantly, the front and rear metal contacts. With series resistance the *I-V* curve of a solar cell is strongly effected which is shown in figure 8. At the open circuit voltage the series resistance has no effect on the solar cell. How-

ever at a point near the open circuit voltage the series resistance has a huge impact on the *I-V* curve [24]. At a point near to the short circuit current the impact of the shunt resistance is strongly affected on the *I-V* curve which results in a power loss of a solar cell with a low shunt resistance which in turn reduces the amount of current flowing through the cell and simultaneously reduces the voltage from the solar cell as shown in figure 9[25].

Exposure to higher temperatures results in an increase in *Isc* and decrease in *Voc* shown in figure 10 and for which outcome there is a decrease in the maximum efficiency of the photovoltaic cell. PhotoVoltaic cells are constructed of crystals which are sensitive to temperature in a manner which is more similar to that of semiconductors [26].

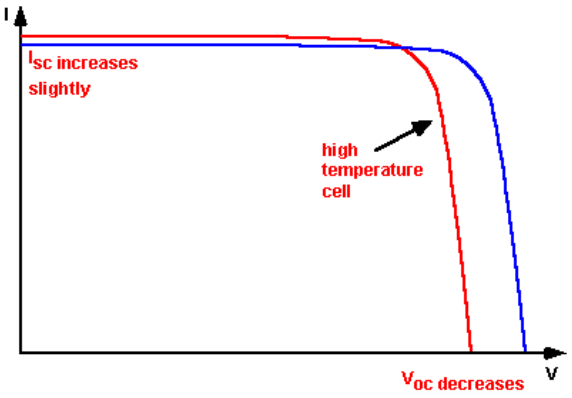


Figure 10: Effect on the *I-V* curve with variation in temperature [26].

3 Methodology / Model

In order to develop a measurement system for tracing the solar *I-V* characteristics, components must be selected whose outcome will produce a low minimal voltage drop when dealing with a low power application. In this section, the selection of suitable components for the current measurement with its corresponding voltage, selection of load in order to drive the measurement system, design selection of cooling system and clamp system are all discussed.

3.1 Hardware

3.1.1 Selection of current transducer

Figure 13 shows the current transducer FHS 40-P/SP600 based on the Hall Effect principle and which is manufactured by the Minisens Company. In relation to the hall effect principle, when the current (*I*) flows in to an electric conductor which is perpendicular to the magnetic field (*B*) exerting a transverse force *Fm* on the charge carriers and which has the tendency *Fe* to move apart to one side of the conductor where it produces a difference voltage between both sides of the conductor. This is shown in figure 11 [12].

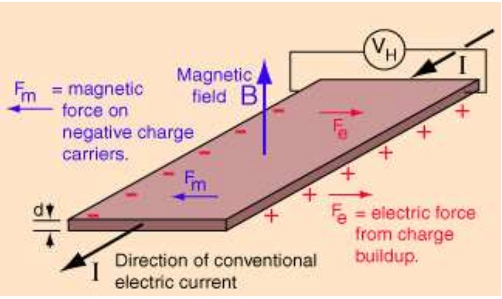


Figure 11: Behaviour of electrical conductor by Hall Effect [12].

Depending on the current rating the LEM Minisens has different kits. As, in this case, a high current of 10A tracking is being dealt with, kit 4 is selected as shown in figure 13. The track width of kit 4 should be noted as it has more width, more sensitivity and also depends on the distance. The figure below shows the complete relation of sensitivity, distance and width.

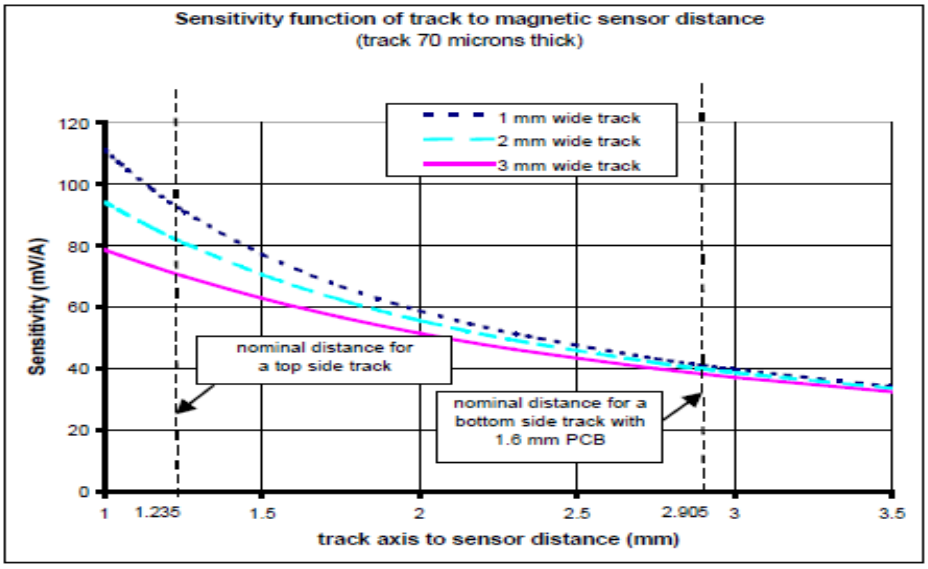


Figure 12 :Sensitivity function of track to magnetic sensor distance[17].

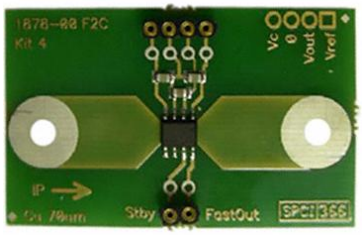


Figure 13: FHS 40-P kit4 [18]

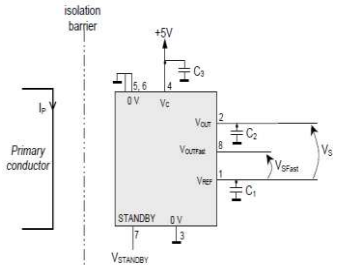
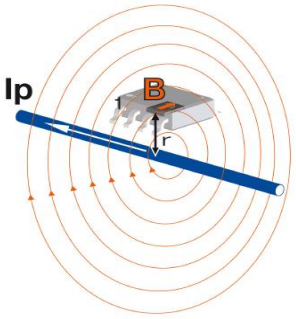


Figure 14: Pin configuration of current Transducer [17].



The Minisens kit 4 works on the Hall Effect principle. When the current flows through the track, the transducer produces difference voltage that senses the magnetic field. Equation 8 shows the generation of the flux density when current flows through the conductor and this is given by [17].

Figure 15: Magnetic field generated by a conductor along a conductor [17]

$B = (\mu/2\Pi)\ (Ip/r)\ T$ _____ *(8)*

Ip= Current to be measured (A), *r* = distance from the centre of the wire (m), $\mu 0$ permeability of vacuum $\mu 0$=4.Π.10^-7 H/m.

Equation 9 shows the voltage and current in relation to the current transducer as follows with figure 14, in which the output voltage is proportional to the current *Vout= Vref +Gi*Ip*. _____ *(9)*
where *Gi* is the sensitivity of value 67.2 mV/A (maximum rating) and *Ip* is the primary current, *Vc* is the positive supply of range 4.75-5.25 V, 0 as *GND, Vref* as reference input/ output voltage [17].

3.1.2 Selection of transistor

To test the solar cell, a linear Metal Oxide Semiconductor Field Effect Transistor (MOSFET) can be used as an electronic load as stated previously commercial systems are available in market such as the Agilent N3300 electronic load for testing solar panels under field conditions however these are expensive. The best and cheapest method is to have a MOSFET that can be operated to obtain current versus voltage and power versus voltage of a solar cell because its rapid variation of the equivalent load resistance [2]. The following theory provides a clear understanding of the MOSFET as a load to drive the test as shown in figure 16. As is already known, there are two types of MOSFETs N-channel and P-channel MOSFETs and because of its high mobility of electrons the N-channel MOSFET is selected. The basic power circuit for testing a solar cell is shown in figure 16. *VGS* is the gate-source voltage, *VDS* is the drain-source voltage and *ID* is the drain current of the MOSFET. *Vpv* is the output voltage of the PV cell and *Voc* is the open circuit voltage. *Isc* is the short circuit current and *Ipv* is the output current of the PV cell.

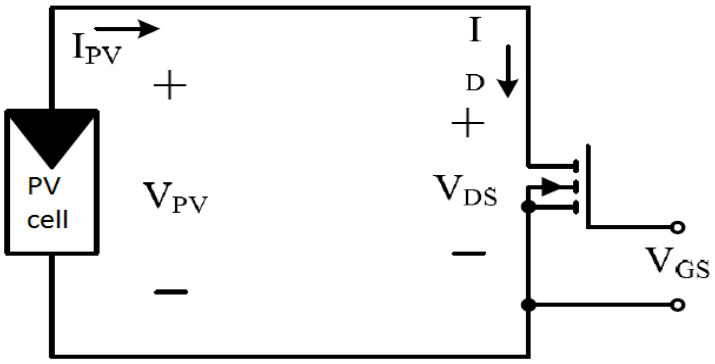


Figure 16: Basic power circuit for testing solar cell [23][2].

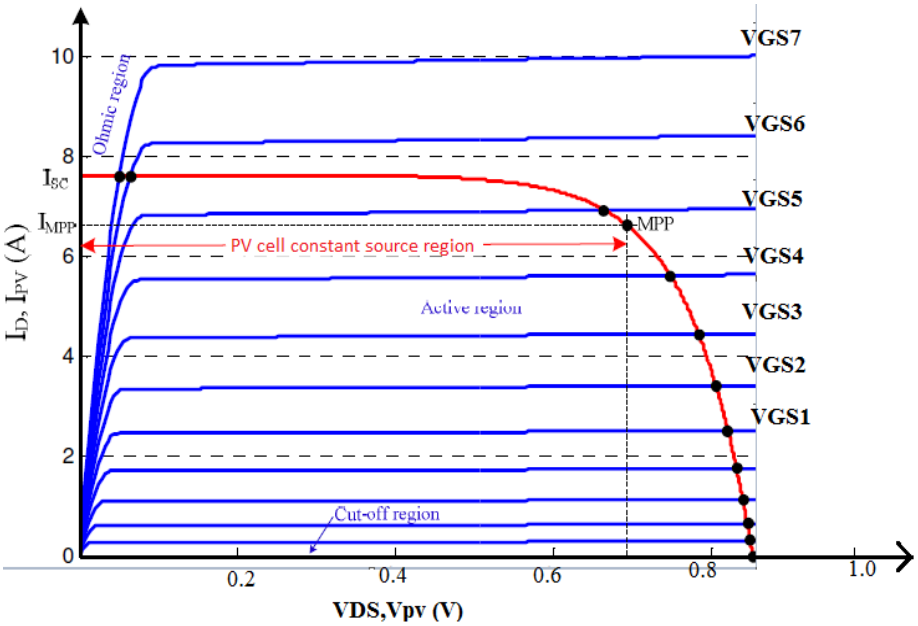


Figure 17: MOSFET characteristics and load curves[23].

The *Ipv-Vpv* characteristics of a PV cell under STC conditions and characteristics of the MOSFET are shown in figure 17 where for a given value of *VGS* each curve *ID-VDS* (blue curves) is plotted [23].

The operating point is given by eqaulising the curent *ID* of the MOSFET, where *ID* and *IPV* are the same which are given by equations 6 and 7

*ID= K(2(VGS-Vth)VDS-VDS^2)= 2K(VGS-Vth)*_____*(6).*

ID= K(VGS-Vth)^2(1+γVDS)*_____ *(7).*

The current of PV cell is given by equation 8

*Ipv=IL-Idiode*_____*(8).*

*Idiode= I0(e^(Vpv/nVt)-1)*_____ *(9).*

Equations 6 and 7 fall under the ohmic region which is also referred to as the linear or triode region and in this case *VDS<VGS-Vth*. In active region, *VDS> VGS-Vth* is also called the saturation region. *IL* is the light generated current *(Isc),Vth* is the threshold gate voltage, n is the diode ideality factor, *Vt* is the thermal volatge,*K* and *γ* are the device parameters. *ID* is given by equation 9 and where *I0* is the dark saturation current [23].

Thus, the operating point of the MOSFET is set when the characteristics of the MOSEFT and the PV cell characteristic are given and these are provided by the value of *VGS*. To draw the *I-V* characteristic curve of a solar cell, sweeping the *VGS* in a range such that the operating point of the MOSFET can easily be changed and thus the operating point of the solar cell can drive along its *I-V* characteristic curve. The MOSFET will be in the OFF state until the *VGS* is above the threshold voltage while sweeping from 0V. Above the threshold, the MOSFET operates in a constant current region as shown in figure 17 [2].

Consideration should be given to the selection of MOSFET for low power applications with a high current and low voltage that the value with the *Rds* ON should be as low as possible so as, for the closed circuit the current with low resistance is required.

3.1.3 Clamp model design

In order to replace the solar cells during testing, a lever arc mechanism is used. This lever arch mechanism is mainly used for filing the papers, folders etc as shown in figure 18.

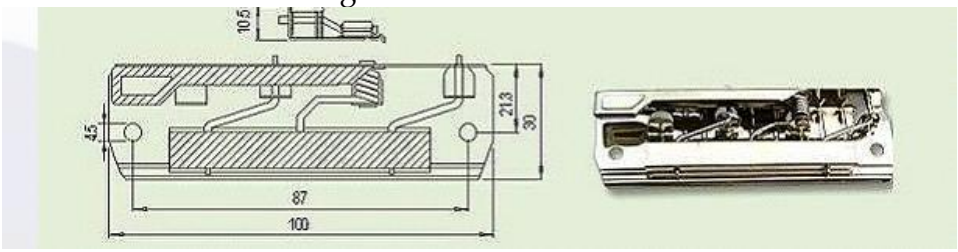


Figure 18 : Lever arch file clip[13]

For easy replacement of solar cells and to hold them during testing, lever file clip mechanism is designed. The lever file clip is designed according to solar cell of area 0.0035m^2 with length 12cm and breadth 3cm as shown in figure 19.

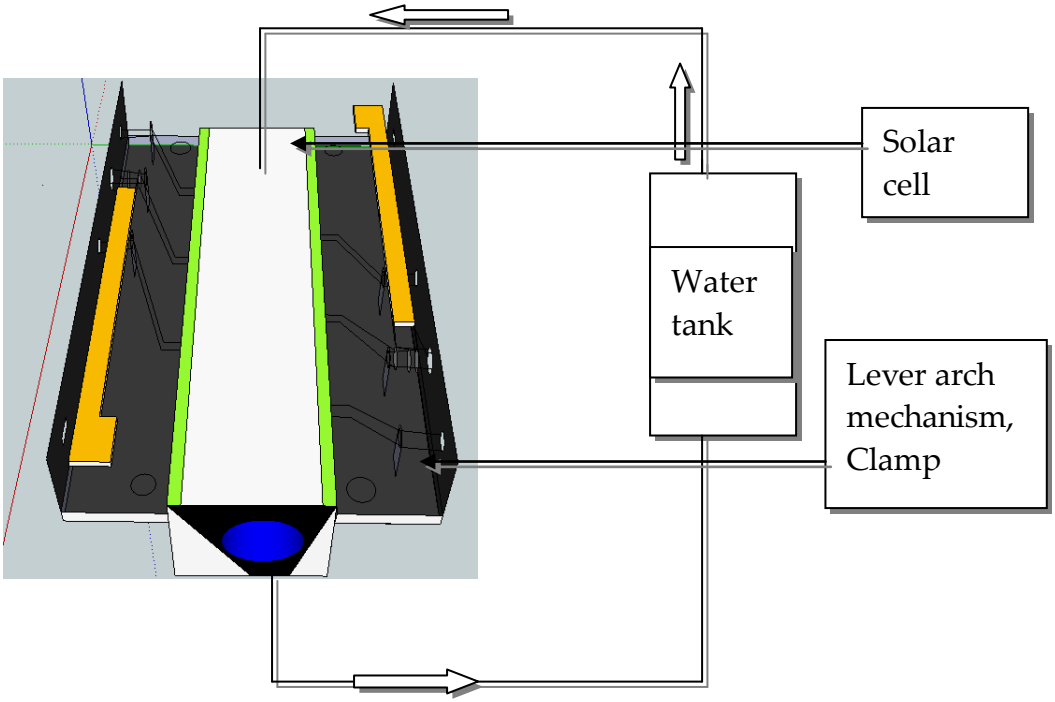
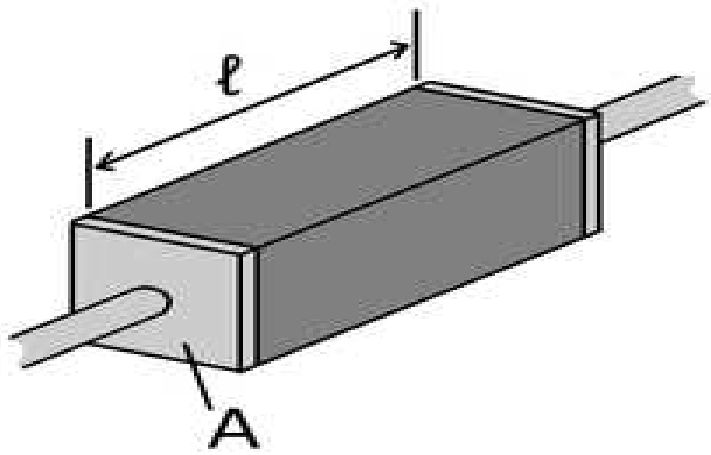


Figure 19: complete model with cooling system and clamp system

3.1.4 Printed Circuit Borad design

The circuit used in this project is designed in Cad soft Eagle layout editor (6.1.0). When dealing with a low power application which arrives at a high current and at low voltage, consideration must be given to the necessity of having a wide track to allow for continuous current with no break point and a low volatge drop. In addition, a careful design must be made regarding the path distance between the components when following equation 10.



$R=\rho\ (l/A)$ _____ *(10)*

Figure 20: A piece of resistive material **Error! Reference source not found.**

Where l is the length of the material in meters
A is the cross sectional area of the specimen in m^2
R is the electrical resistance of a uniform specimen of the material in Ω.
ρ is the resistivtiy of the material conductivity Ω-m.

Figure 21 shows the layout of the board and in which the components are placed with more width and a shorter distance. The circuit is designed in a single layer. It is recommended to consider the resistance while using a single layer board [9]. A careful design has been conducted for the return path for the inputs and the load. Because of the high amount of current flowing through the circuit, a ground plane is designed as shown in figure 22. It is also recommended to account for the resistance of the power leads of the device. In a single layer, the board will be significantly affected by radiated noise if many jump wires are used [9]. In this project, because of the low complexity of the design as it consists of a single layer, the focus is on the return path. In order to design the board in CadSoft eagle version 6.1.0 the following steps are involved. For some hardware components in CadSoft eagle, there are combinations of inbuilt symbols and packages, called a device, that are included in the library. However, if it is necessary to add symbols and to create package with particular dimensions for a device then it is possible to add this to the library. In this case, in the Printed Circuit Board component design, the temperature sensor SOT23 device and the phoenix connetors are in the library thus there was no requirement to create a symbol and package[11]. After creating components the layout is viewed in board layout from schematic a shown in figure 22.

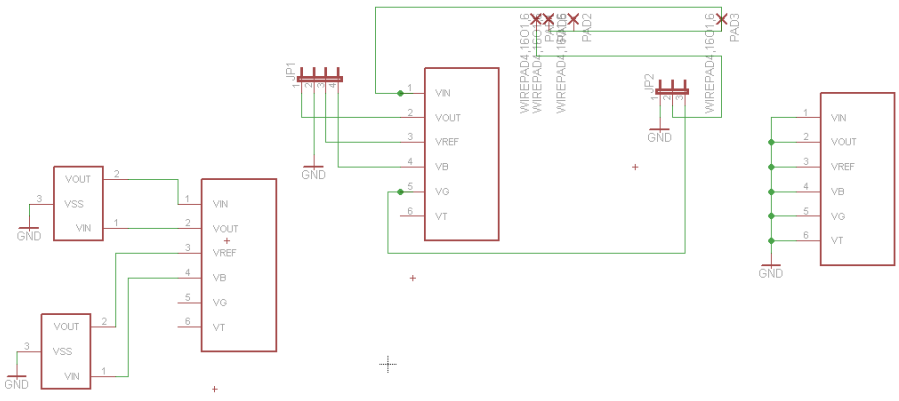


Figure 21: Schematic for current transducer, phoenix connectors, temperature sensor and MOSFET

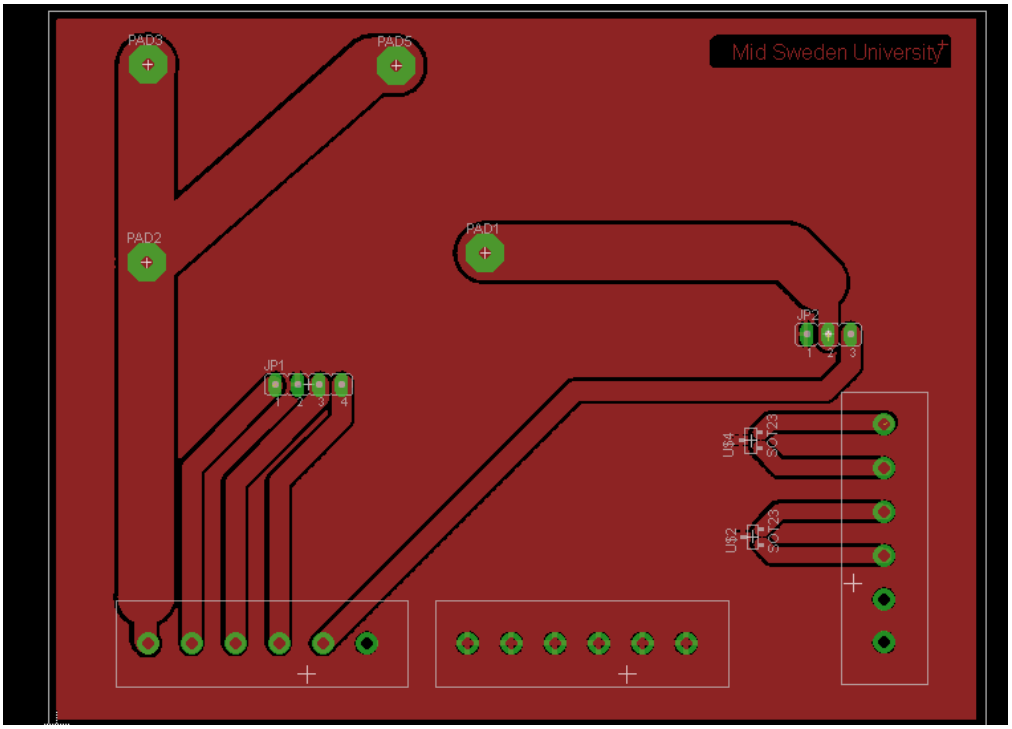


Figure 22: Board layout for current transducer, MOSFET, temperature sensors, Phoenix connectors

When both the analog and digital ground planes are connected together, the circuit is more susceptible to digital noise in the analog circuitry due to a capacitance disturbance between the overlapping of the analog and digital portions. This should be dealt with in a similar manner to placing the analog power coincident with the analog ground and, on the other hand, placing the digital power coincident with the digital ground [9]. In this project, this was dealt with by means of the analog power circuitry and not with the digital power circuitry. The analog power was placed coincidentwith the analog ground.

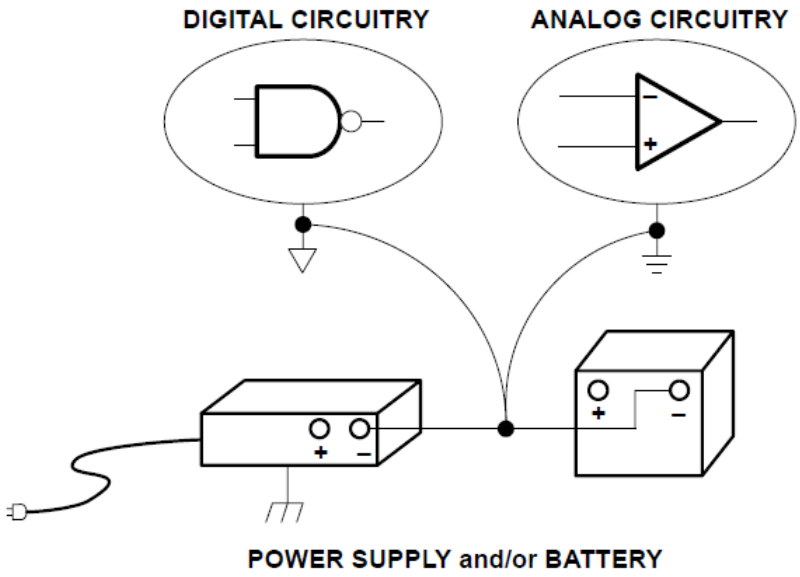


Figure 23: Common ground for analog and digital planes on PCB [9].

No confusion should occur as the system will have only one ground for the analog and digital portion of the circuitry, which should meet at the common point, the preference for which is a single point with low impedance. A good design of a PCB board should avoid ground loops for which the ground is not a return point [9]. In relation to this peoject, an analog ground plane was used for the electronic load circuit. Groundloops were avoided and the *I/O* connections for the board were made to be as close as possible.

A good design not only has a ground plane but other factors such as creepage clearance and trace reflections are considered as shown in figure 24. In relation to trace reflections, as shown in figure 25, not all the PCB traces are straight as in some cases they must turn at corners. For a 90 degrees turn, at the apex of the corner, the trace width is 1.414 times its width which results in a reflection, for which the transmission line characteristics are upset due to a disturbed capacitance and a self inductance change [9]]. Moreover, the majority of CAD systems do not possess a constant width at the corners. Figure 24 shows the method of rounding the cornersin order to avoid reflections.

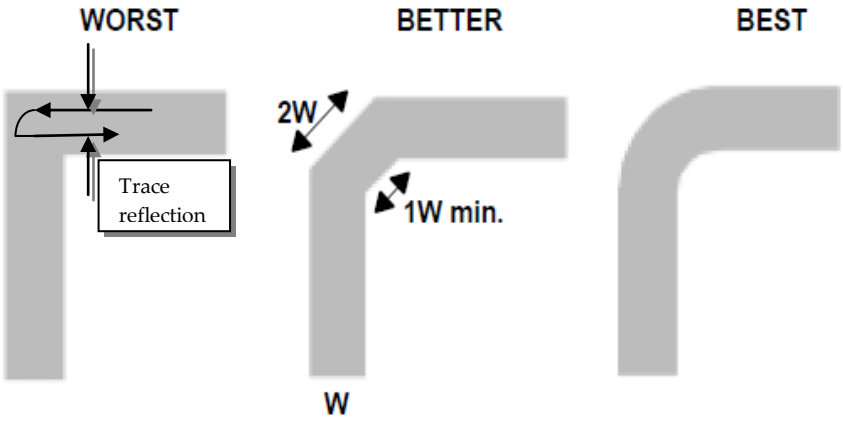


Figure 24: PCB trace corners [9].

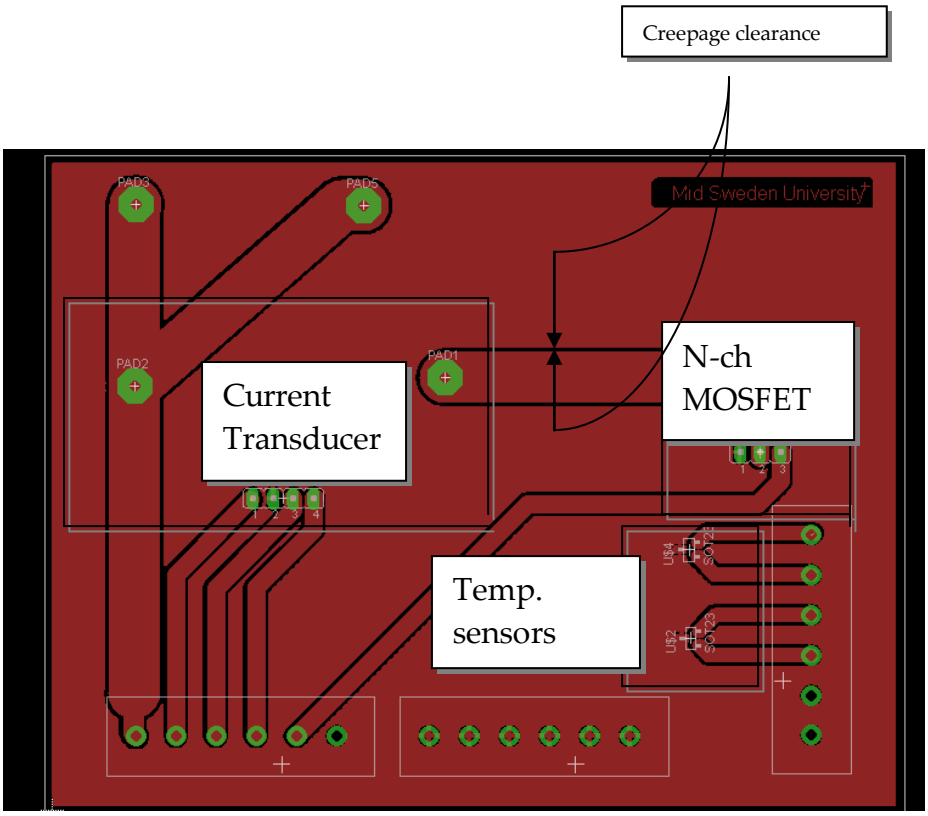


Figure 25: Printed Circuit Board (PCB) design in Cad Soft eagle version (6.1.0)

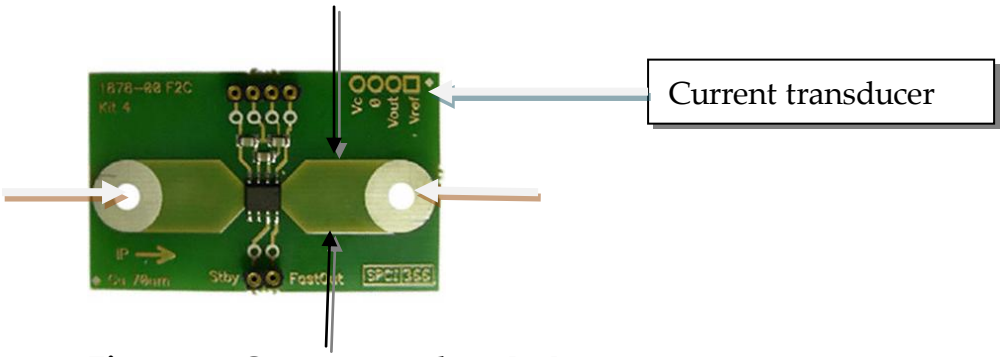


Figure 26: Current transducer[17]

The track, highlighted by black, on the current transducer should be maintained along the PCB so as to enable the current to flow with no break point. If this is not the case, then, the voltage drop drop across that path, which is then connected to the drain of the MOSFET would increase as shown in figure 26. The current transducer contacts, highlighted in orange, must be maintained to have as much contact as possible with the M3 screws and with the washers on both the front and back so that the input current with continuous flow provides a low voltage drop. These two steps are to be considered while connecting the current transducer to the PCB board.

3.2 Software model

3.2.1 Introduction to LabVIEW

National Instruments developed a platform for visual programming language, which is called Lab VIEW (Laboratory Virtual Instrumentation Engineering Workbench). For engineers and scientists LabVIEW is a system design software that provides the tools to create and deploy measurement and control systems for hardware integration which is either unknown or which has not been previously experienced. In relation to the user end, instrumentation solutions such as those for controlling and measuring can be developed with VI ,which is a combination of hardware and software and which consists of a block diagram, front panel, and icon/connector. For this, National Instruments introduced several plugs in the hardware and driver software such as data acquisition (DAQ), serial communications, etc. This project used NI USB-6008 data acquisition (DAQ). It is a low cost and simple multifunction *I/O* and control device with 8 analog inputs (12-bit, 10 KS/s), 2 analog outputs (12-bit, 150 S/s), 12 digital *I/O* with no extra supply and which is compatible with LabVIEW including the NI-DAQmx driver software.

3.2.2 Features of DAQmx

Analog input represented as (AI) has 8 inputs that can be of single ended signals or with 4 inputs that are differential signals. Voltage ranges that are easily configured are of ±10V, ±5V, ±4V, ±2.5V, ±2V, ±1.25V, ±1V. The maximum sampling rate is 10kS/s (10000 samples per second) with a 12 bits AD converter. The analog output is represented as (AO) and has 2 outputs with a voltage range of 0 - 5V (fixed) at an output rate of 150Hz (samples/second) with a 12 bits DA converter.
Digital input (DI) and digital output (DO) possesses 12 channels which are organized in ports, with Port 0 and Port 1 having lines 0, .., 7 of port 0 and lines 0, .., 3 of port1. Input low is based on a range of -0.3V and +0.8V and Input high is for a range of 2.0V and +5.8V. Output low uses 0.8V and output high is above 2V. 2.5V and 5.0V voltage sources are available at individual terminals with counter 32 bits that are on the falling edge.
.

Documentation
The documentation for the NI USB-6008 DAQ device is as follows:
NI USB-6008 Data Sheet
NI USB-6008 User Guide
NI-DAQ mx for USB Devices
These documents are available from www.ni.com.

NI-USB 6008 Configuration:

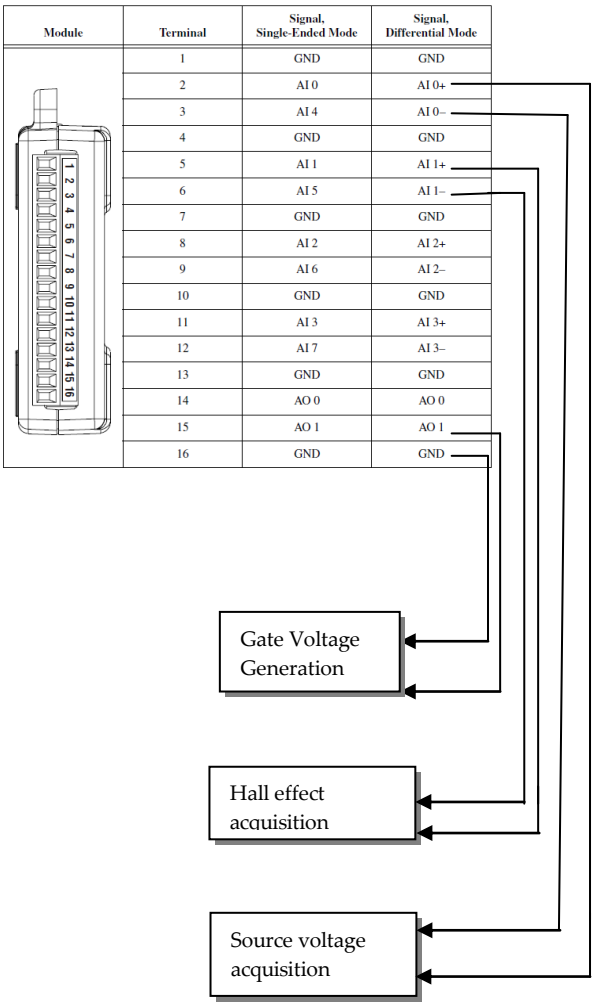
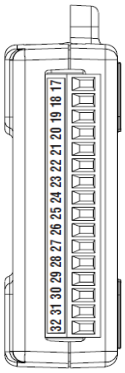


Table 1: Analog terminal assignments [14]

Module	Terminal	Signal
	17	P0.0
	18	P0.1
	19	P0.2
	20	P0.3
	21	P0.4
	22	P0.5
	23	P0 6
	24	P0.7
	25	P1.0
	26	P1.1
	27	P1.2
	28	P1.3
	29	PFI 0
	30	+2.5 V
	31	+5 V
	32	GND

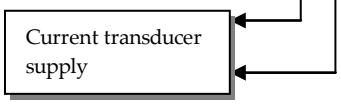


Table 2: Digital terminal assignments [14]

Signal Name	Reference	Direction	Description
GND	—	—	**Ground**—The reference point for the single-ended AI measurements, bias current return point for differential mode measurements, AO voltages, digital signals at the I/O connector, +5 VDC supply, and the +2.5 VDC reference.
AI <0..7>	Varies	Input	**Analog Input Channels 0 to 7**—For single-ended measurements, each signal is an analog input voltage channel. For differential measurements, AI 0 and AI 4 are the positive and negative inputs of differential analog input channel 0. The following signal pairs also form differential input channels: <AI 1, AI 5>, <AI 2, AI 6>, and <AI 3, AI 7>.
AO 0	GND	Output	**Analog Channel 0 Output**—Supplies the voltage output of AO channel 0.
AO 1	GND	Output	**Analog Channel 1 Output**—Supplies the voltage output of AO channel 1.
P1.<0..3> P0.<0..7>	GND	Input or Output	**Digital I/O Signals**—You can individually configure each signal as an input or output.
+2.5 V	GND	Output	**+2.5 V External Reference**—Provides a reference for wrap-back testing.
+5 V	GND	Output	**+5 V Power Source**—Provides +5 V power up to 200 mA.
PFI 0	GND	Input	**PFI 0**—This pin is configurable as either a digital trigger or an event counter input.

Table 3: Signal Descriptions of NI USB-6008 DAQ [14]

There are two types of analog input modes as shown in the table which is represented as AI, single ended and differential ended. Differential mode is preferred when the signal is of a floating type, which can be easily stated as positive and negative differences between the analog inputs that are to be measured [16]. For the measurement of the voltage and temperature, a differential mode was used in this case as the voltage signals are not connected to an absolute reference. When the input, with respect to common ground, is used then a single ended mode is acceptable for which the converter expects a positive input and , in this case, the voltage signals are referenced to a system ground. At the same time the single ended measurement cannot be stated as being negative, USB -6008 has a resistor network that can scale the range -10V to +10V to 0V to +10V ref.

3.2.3 LabVIEW functions

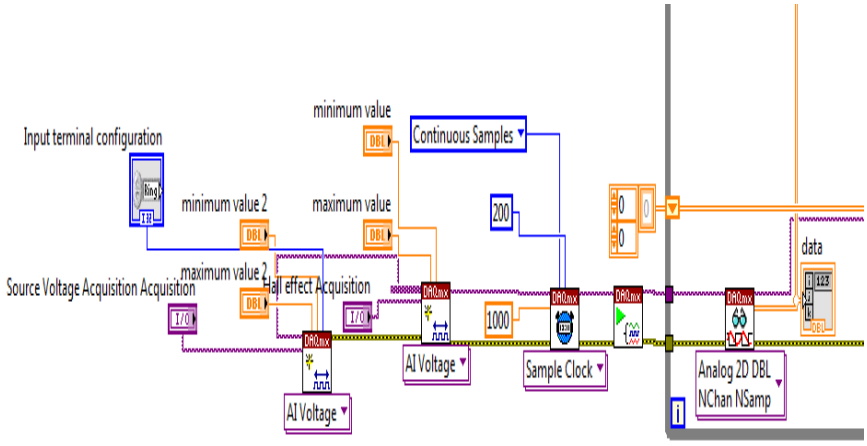


Figure 27:Develeped LabVIEW code for solar *I-V* characteristics(acquisition part)

DAQmx create Virtual Channel (VI):
Virtual channel is created and adds them to a task. For analog input, digital output or counter output the polymorphic VI corresponds to the *I/O* type of channel; performs the temperature measurement, voltage generation.

AI voltage:
Creates a channel used for the measurement of voltage. As shown in figure 27, the named source voltage acquisition is the physical channel used to measure the voltage of a solar cell and the named Hall Effect acquisition is the physical channel used to measure the voltage difference of the current transducer, which corresponds to a measurement of the current. The maximum and minimum value is set to +5 and -5. The input terminal configuration is set to differential mode for both source voltage and Hall Effect acquisition.

DAQmx Timing (VI):
The DAQmx timing VI configures the number of samples to be acquired or generated.
Sample mode is set to continuous mode to acquire the samples until the DAQmx stop task VI runs. For a better representation of the original input signal, the sampling rate is set to 1 kHz specifying 200 samples for each channel. Poor representation of the analog signal occurs when sampling is too slow. In a given time, more points are acquired thus setting a fast sampling rate. With a 1 kHz sampling rate and 200 samples per channel, this proves to be more than sufficient for the representation of signal. With the specified samples and sampling rate, the current and voltage values are plotted perfectly at the region of interest that is from *Voc* to *Isc*.

DAQmx start task (VI):
The DAQmx start task changes the status of the task from running state to beginning the measurement or generation.

DAQmx Read (VI):
The DAQmx read VI is used for reading the samples from the virtual channels, named as the source voltage acquisition and Hall Effect acquisition. The DAQmx read VI is able to read multiple samples or a single sample. In this project, multiple samples are read simultaneously from multiple channels as shown in figure 27. Data named in figure 27 is a 2D array of samples in which each row corresponds to a channel in the task. On the other side, a column corresponds to a sample from each channel.

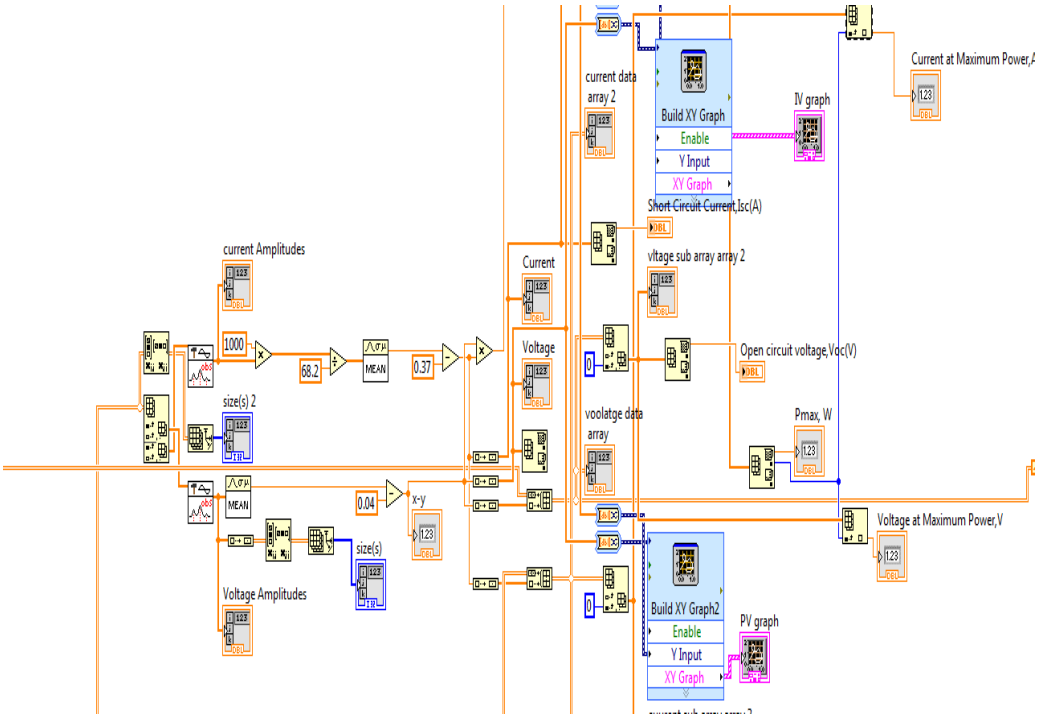


Figure 28: Developed LabVIEW code for solar *I-V* characteristics (data manipulation part).

After acquiring the input data from the source voltage and Hall Effect acquisition channels, the data is extracted separately to the source voltage and Hall Effect difference voltage. In this case DC is being dealt with, the input signal is of a floating type in which the peak detector is used to find the amplitude of the peaks in the input signal and then averaged with the mean block that corresponds to the DC values. The Hall Effect difference voltage values are manipulated to the current as in section 3.1.1.The whole task is implemented until the loop for the continuous run reaches the Gate voltage of the MOSFET condition of 5V.

3.3 Overview of system design

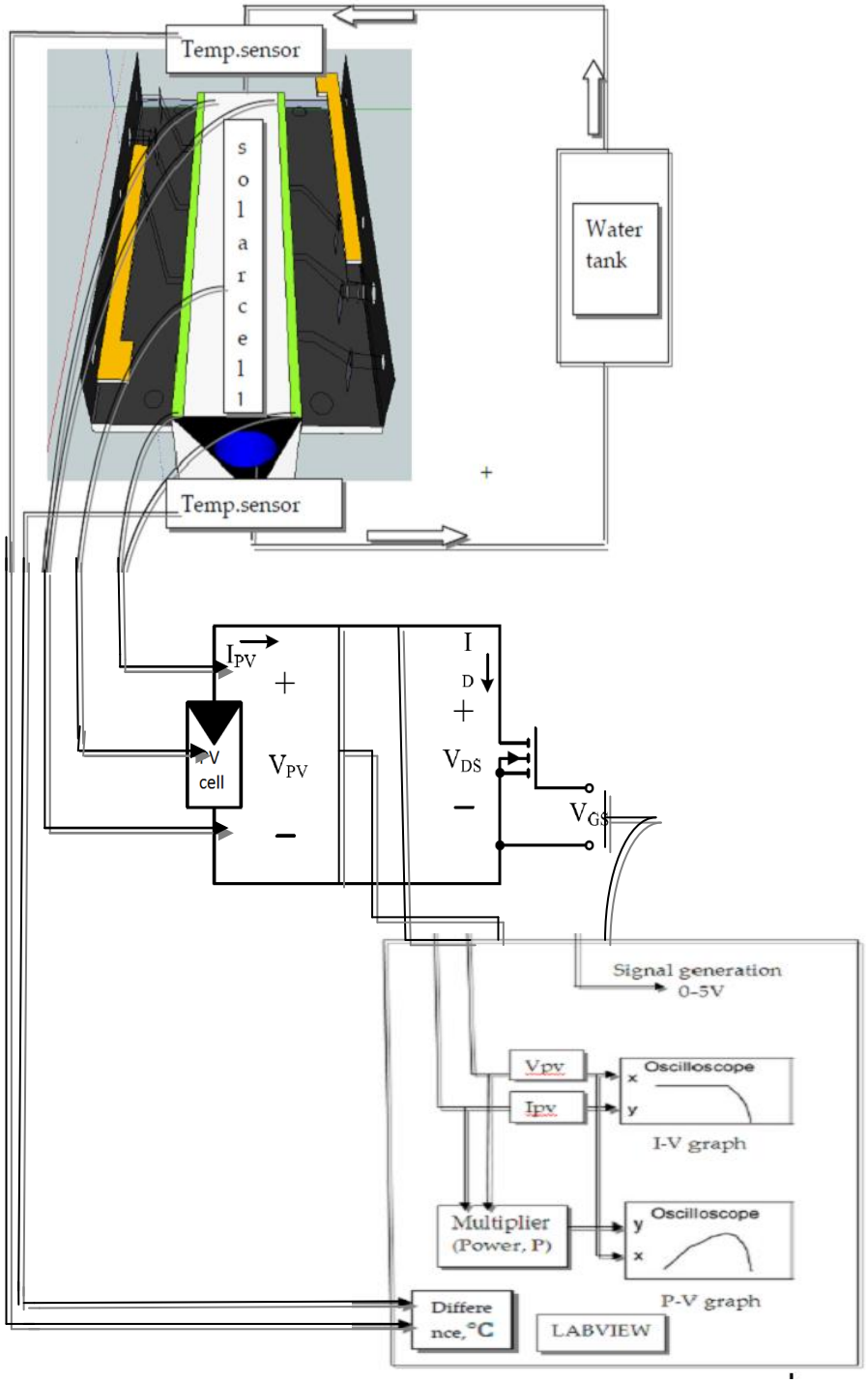


Figure 29:Overview of system model

The above figure 29 shows the overview of system model to track *I-V, P-V* characteristics. Driving the load circuit with a 0-5V gate signal drives the circuit from *Voc* to *Isc,* which are then measured in LabVIEW at the maximum values of *Vpv* and *Ipv*. The difference in temperature readings through the sensors in and out flow of the heat pipe array provides an approximate value of the solar cell temperature. As the cooling system has not been implemented during the period of this thesis work, the tracking of the temperature is has not been conducted. In order to have an overview of the system model provided, a sketch of the tracking temperature is shown in figure 29.

4 Experimental setup

In order to trace the *I-V* characteristics of a solar cell under field conditions of 10000W/m^2 an efficient cooling system should underlay the solar cell. As the cooling system was not constructed during this thesis period, the measurement system was tested with a power supply rating of 0.7V and 10A in which a solar cell in a real case has the same rating.
The load cell developed in this thesis work is connected to a power supply of (0-30) V and 20A. Driving from the open circuit 0.7 Voc to the short-circuit 10A, the Isc of the power supply with the MOSFET provides I-*V* characteristics of a similar nature to the solar cell characteristics.

Before testing the load cell with a power supply of (0-30) V and 20A, the load cell is tested with a power supply (0-30) V and 10A.

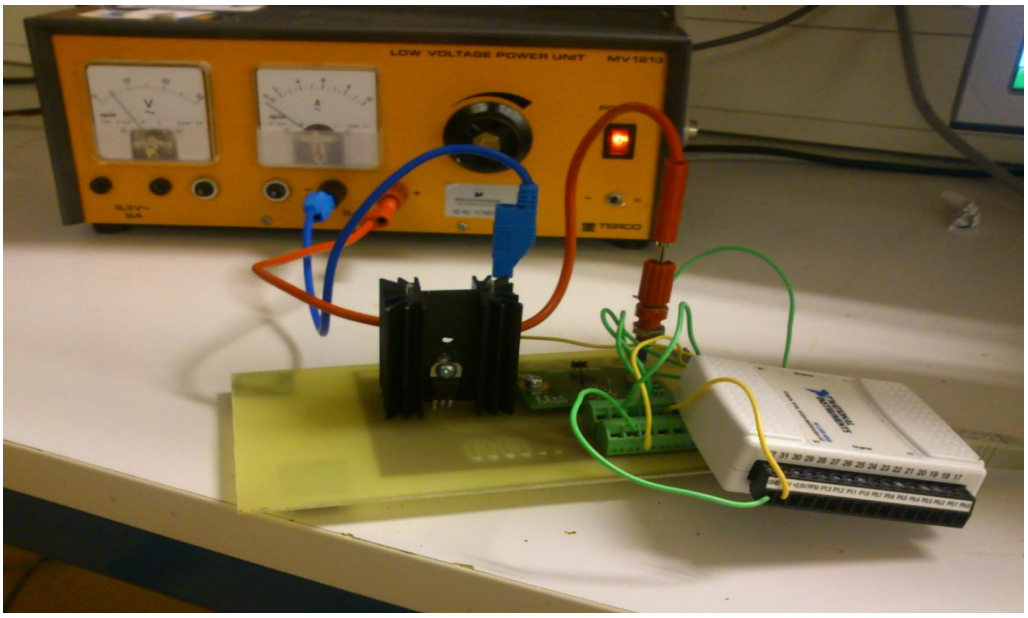


Figure 30: Load cell connection with power supply (0-30) V 10A

Varying the load resistance from 0 Ohm to infinity with the MOSFET provides the *I-V* characteristics of solar cell. The data acquisition system acquires data for the current and voltage in applying the Gate voltage from (0-5) V which is equivalent to varying the load resistance. Across each value of the load resistance, in steps of 0.05, current with the corresponding voltage values is acquired. The collected data is able to plot the graph from the open circuit *Voc* to the short circuit *Isc*. The data in which LabVIEW is able to plot the *I-V* graph provides the maximum power rating and also the Power –Voltage graph. Through the plotted graphs, *I-V* and *P-V*, it becomes possible to draw the parameters for the Fill factor and efficiency. The project presents an *I-V* graph so as to be able to see the voltage existence at the maximum current.

5 Results

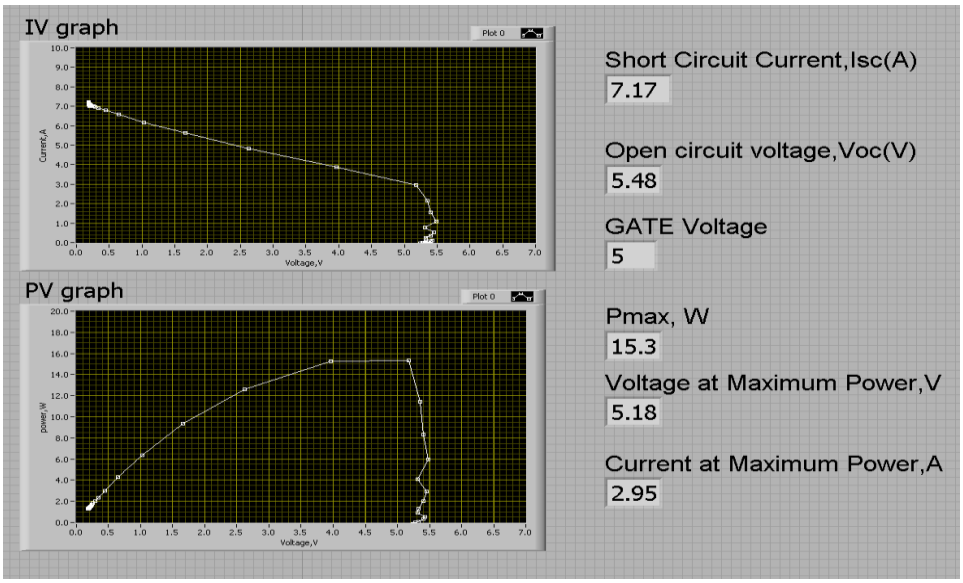


Figure 31: Experimental results of load cell at 5V and 8A.

Before testing the load cell in a realistic case of 0.7V and 10A, the load cell is tested with a power supply of 5V and 8A. As observed in figure 31 the load cell has a series resistance of 6.25 mΩ where the slope of the *I-V* curve states that the load cell is suitable for testing a solar cell. The following figure shows the load cell tested in a realistic case of 0.7V and 10A.

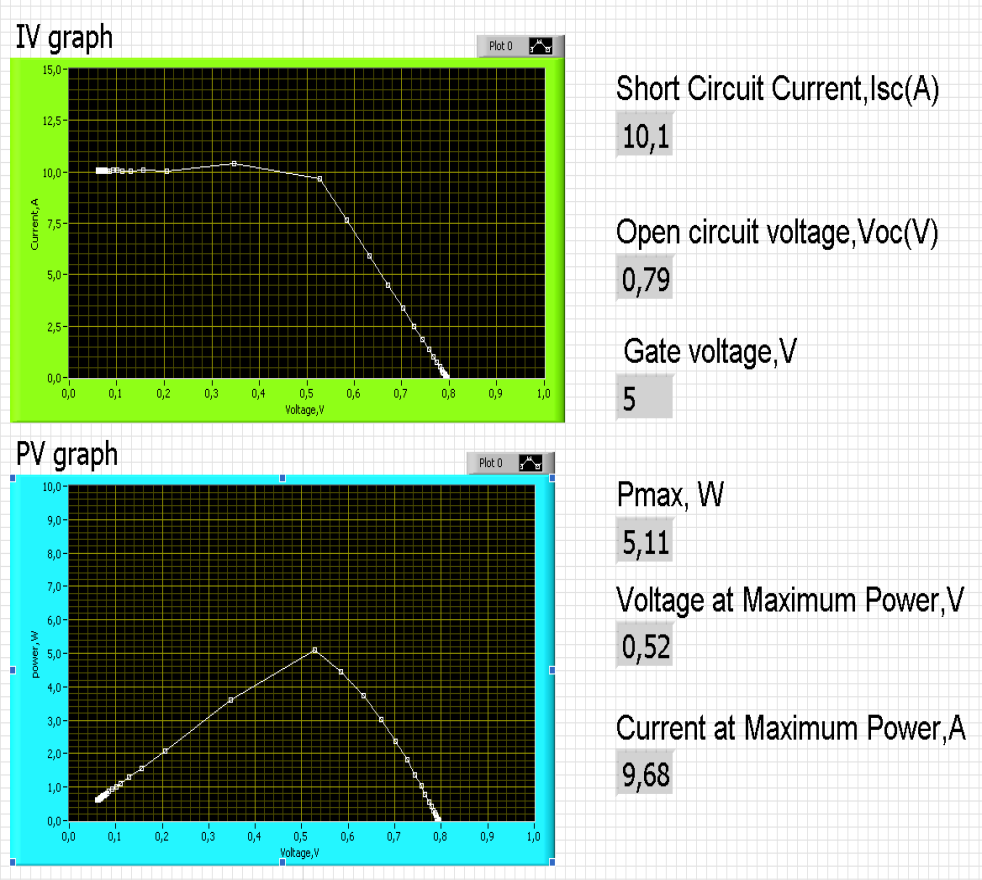


Figure 32: Experimental result of load cell at 0.8V and 10A.

By observing figure 32 above, the load cell is suitable for testing a solar cell where it draws the *I-V* and *P-V* characteristics which have a low series resistance of 7.9 mΩ at a full rated current with a voltage drop of 79mV. The voltage drop is due to the MOSFET where it has 35mΩ *Rds* ON at a full rated current of 10 A with 35mV. In addition, for the current transducer with a voltage drop of 42mV this is due to the current transducer track contacts (M3 screws) with the PCB. This was the main intention of the thesis to reduce the series resistance of a load cell such that the solar cell can be tested in order to determine the voltage drop at the maximum rated current.

6 Conclusion

The load cell for testing a solar cell has been designed, implemented and tested with a power supply rating of 0.7V and 10A. The developed load cell is suitable for testing a solar cell after observing the results. A method for a cooling system has also been suggested, which has the maximum efficiency of a solar cell during irradiation and which is able to observe the temperature of a solar cell. The design provided for the clamp system in order to enable an easy replacement of solar cells during testing has also been accomplished. The tested results indicate that the load cell is suitable for testing a solar cell where it has low voltage drop of 79mV.

Future Work

The development of a clamp system and the implementation of water cooling system for tracking of temperature are to be made in order to have a complete measurement system for testing the solar cell under 10 standard suns.

7 References

[1] Francisco M. González-Longatt "Model of Photovoltaic Module in Matlab", 2DO CONGRESO IBEROAMERICANO DEESTUDIANTES DE INGENIERÍA ELÉCTRICA, ELECTRÓNICA Y COMPUTACIÓN (II CIBELEC 2005)

[2] Yinying Kuai,S.Yuvarajan" An electronic load for testing photovoltaic panels", North Dakota State University, June 25.

[3] Introduction of Photovoltaic systems SECO Fact sheet no.11http://www.infinitepower.org/pdf/FactSheet-11.pdf, Page no; 2.

[4] National Solar Power Research Institute, fundamentals of photovoltaic Materials, 12/21/98.

[5] Part II-Photovoltaic cell I-V characterization Theory and LabVIEW Analysis code http://www.ni.com/white-paper/7230/en Page no; 1.

[6] Solar cell junction temperature measurement of PV module, National Taiwan University, Photovoltaic Technology Center, Industrial Technology Research Institute, Taiwan. 18, December 2010.

[7] Reddy, P. Jayarama, Science Technology of Photovoltaics, second edition,2010 Page no 11,17 ,18,19,20

[8] Xiao Tang, Zhenhua Quan, Yaohua Zhao, Experimental Investigation of Solar Panel Cooling by a Novel Micro Heat Pipe Array, *Beijing* University of Technology, Beijing, China, June 29, 2010.

[9] Texas Instruments, Circuit board layout techniques, *Chapter 17*, Literature Number SLOA089.

[10] Chapter 12 Printed Circuit Board design issues. section 12.3. http://www.analog.com/library/analogdialogue/archives/43-09/EDch%2012%20pc%20issues.pdf

[11] Schematic-layout-Autorouter, Page no 15 http://www.cadsoft.de/wp-content/uploads/2011/05/tutorial-eng.pdf.

[12] Hyper physics, Hall Effect http://hyperphysics.phy-astr.gsu.edu/hbase/magnetic/hall.html page no; 1.

[13] http://www.alibaba.com/trade/search?SearchText=lever+arch+file+mechanism&IndexArea=product_en&fsb=y

[14] National Instruments USER GUIDE AND SPECIFICATIONS USB6008/6009 Page no 7, 8, and 9.

[15] Maximum Peak Power Tracker:A Solar Application, Daniel F.Butay Michael T.Miller, April 24th 2008,Page no 12.

[16] ME experimental methods, Data Acquisition,BJ Furman 30SEP02,Page no 4,5.

[17] Current transducer FHS 40-P/SP600,Minisens http://www.lem.com/docs/products/fhs%2040-p%20sp600.pdf page no 7,9,11.

[18] User guide for FHS 40-P current transducer FHS 40-P kit 4 http://www.lem.com/docs/manuals/KIT%204%20FHS%2040-P.pdf page no 1, 4.

[19] TC1047/TC1047A,Precision temperature to voltage converter

[20] Hebe corporation, http://www.hebesolar.com/monocrystalline-silicon-solar-cells.html

[21] Solar cell Voltage-Current characterization, California Scientific research http://www.californiascientific.com/resource/Solar%20Cell.pdf

[22] A. Durgadevi, S. Arulselvi and S.P.Natarajan, Photovoltaic Modeling and Its Characteristics, page no 469,470.

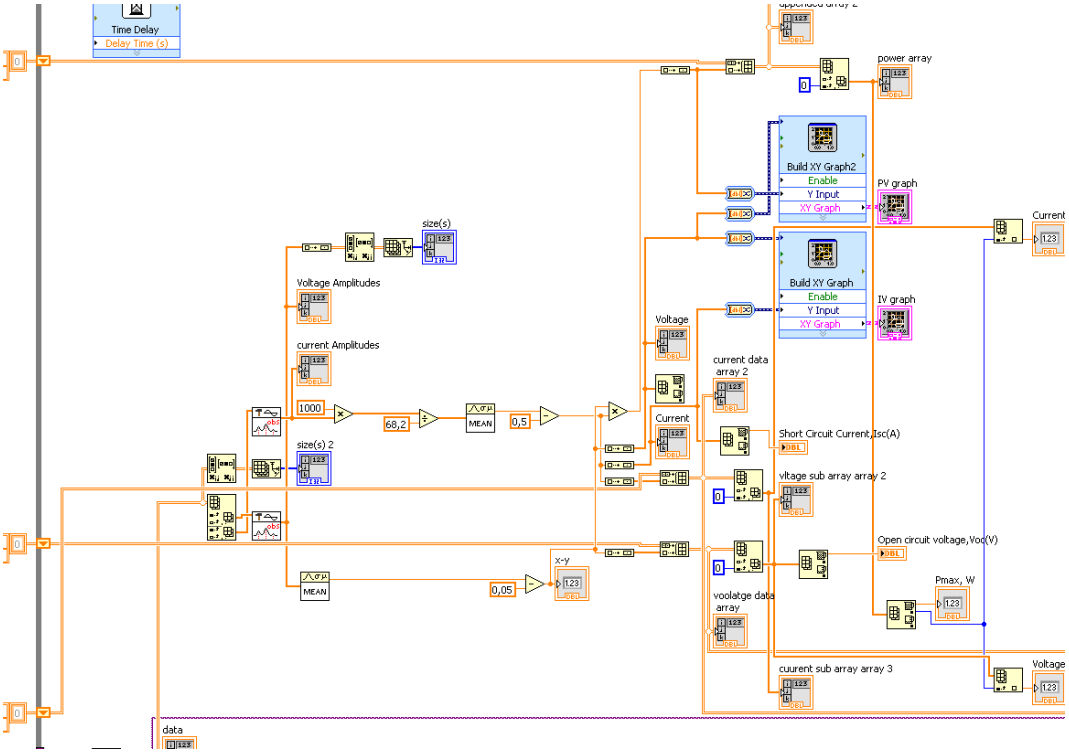
[23] Vicente Leite and Faustino Chenlo, An Improved Electronic Circuit for Tracing the I-V Characteristics of Photovoltaic Modules and Strings, Page no 2.

[24] Christiana Honsberg and Stuart Bowden, PVeducation.org. http://www.pveducation.org/pvcdrom/solar-cell-operation/series-resistance

[25] Christiana Honsberg and Stuart Bowden, PVeducation.org. http://www.pveducation.org/pvcdrom/solar-cell-operation/shunt-resistance

[26] Christiana Honsberg and Stuart Bowden,PVeducation.org http://www.pveducation.org/pvcdrom/solar-cell-operation/effect- of-temperature

Appendix A: Documentation of own developed program code



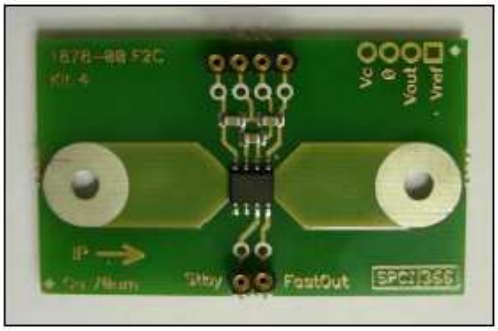
Appendix B: User manual

LEM

User guide for FHS 40-P Current Transducer

FHS 40-P Kit 4 (G2.00.23.103.0)

Evaluation PCB



Connectors Pin-OUT

The board has two single row connectors J1 and J2.

- The four pin one (J1) makes possible to supply the board and access to the output voltage easily. It has the following pin-out:

Pin #	Name	Description J1 connector
1	V_{REF}	Reference voltage input/output
2	V_{OUT}	Output voltage is proportional to current in the PCB track, $V_{OUT} = V_{REF} + G_I * I_P$ Note that the output voltage is positive when the current flows inside the tracks according to the direction marked "I_P→" on the PCB
3	0	0 V
4	V_C	Positive supply voltage 4.75-5.25 V; typical consumption 15 mA

- The two pin one (J2) makes possible to access to the fast output voltage and standby input easily. It has the following pin-out:

Pin #	Name	Description J2 connector
1	$V_{OUTFAST}$	$V_{OUTFAST}$, fast output signal; note that this output is opposite to V_{OUT} (see datasheet for connection)
2	Standby	Standby, Set operating or Standby modes (see datasheet for connection)

Manufacturer and reference for J1, J2: PRECI-DIP, 310-13-120-41-001001.

Thermal Capability

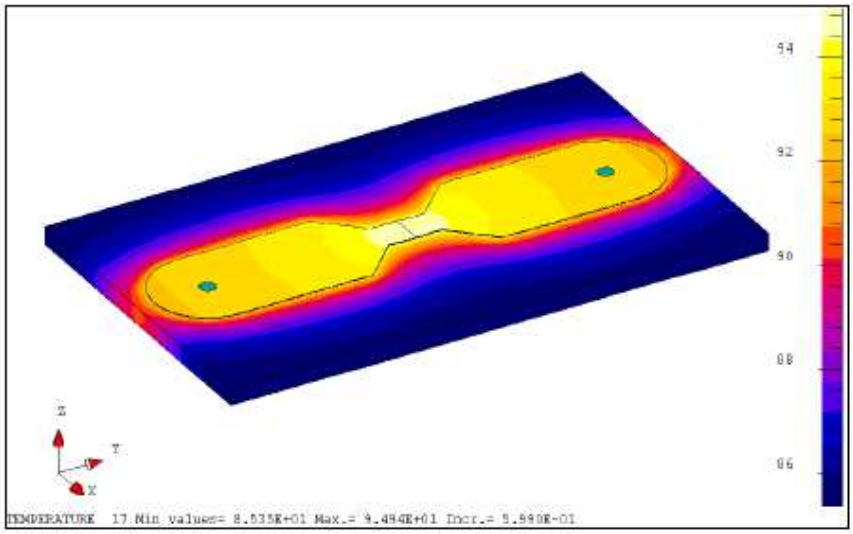
The enclosed evaluation PCB has tracks with thickness of 70 µm.

The dimensions of the tracks drawn on the evaluation PCB lead to some limitations on the maximum continuous current which can go through the PCB track.

Remark: under normal operating conditions, temperature of some parts of this product might exceed 70°C.

Thermal simulation Cu 70 µm:

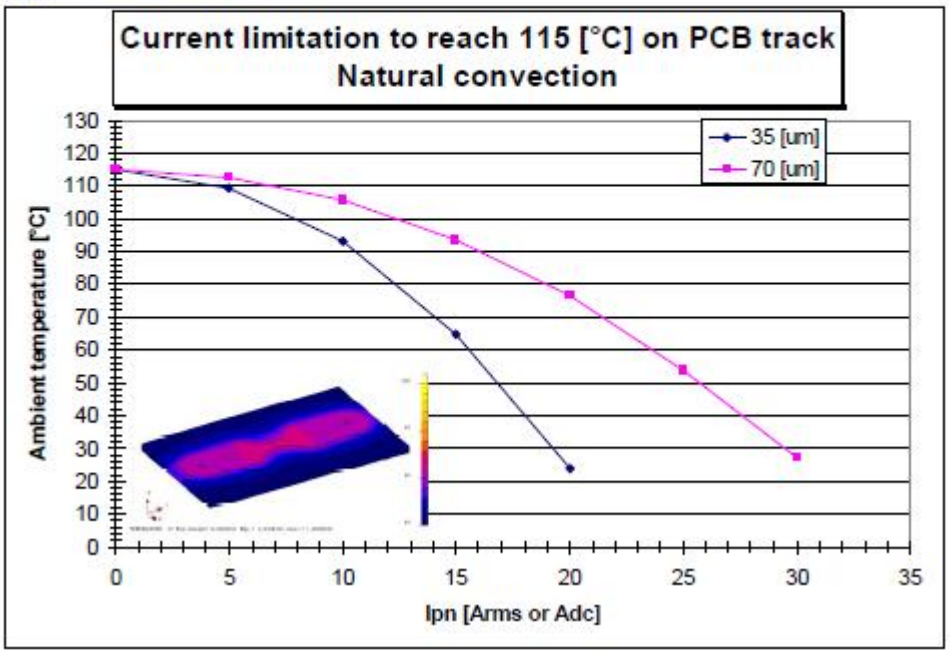
Track thickness 70 µm, PCB thickness 1.6 mm, T_A = 85°C, natural convection, I_{PN} = 10 A rms or A DC.

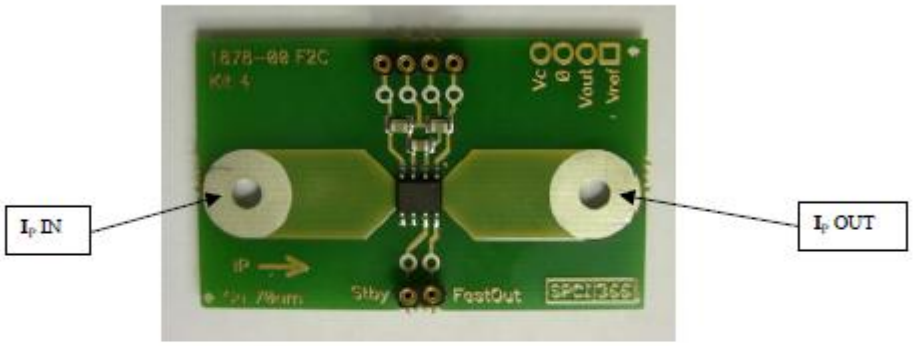


The following figures should be taken into account to avoid overheating:

(T primary track = 115 °C)

Maxi rms current I_{PN} [A]	Cu 35 µm		Cu 70 µm	
	T_A [°C]	ΔT [°C]	T_A [°C]	ΔT [°C]
0	115	0	115	0
5	109.5	5.5	112.5	2.5
10	93	22	105.5	9.5
15	65	50	93.5	21.5
20	24	91	76.5	38.5
25	NA	NA	54	61
30	NA	NA	27	88





Connect then the primary between pins I_P IN and I_P OUT.

Features

Magnetic field sensitivity	Typical 600	mV/mT
Current sensitivity	Typical 67.2 mini (typical-3σ): 66.1 maxi (typical+3σ): 68.2	mV/A
Measuring range	typical ± 30 Unless maxi rms current reached, see Thermal Capability.	A
Frequency range	DC – 100k	Hz