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Parabilis: Speeding up Single-Threaded Applications by Extracting Fine-Grained Threads for Multi-Core Execution

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Parabilis: Speeding up Single-Threaded Applications by Extracting Fine-Grained Threads for Multi-Core Execution

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Abstract

The trend in architectural designs has been towards using simple cores for building multicore chips, instead of a single complex out-of-order (OOO) cores, due to the increased complexity and energy requirements of out of order processors. Multicore chips provide better performance when compared with OOO cores while executing parallel applications. However, they are not able to exploit the parallelism inherent in single threaded applications. To this end, this paper presents a compiler optimization methodology coupled with minimal hardware extensions to extract simple fine-grained threads from a single-threaded application, for execution on multiple cores of a chip multiprocessor (CMP). These fine-grained threads are independent and eliminate the need for communication between cores, reducing costly communication latencies. This approach, which we call Parabilis is scalable for up to eight cores, and does not require complex hardware additions to simple multicore systems. Our evaluation shows that Parabilis yields an average speedup of 1.51 on an 8-core CMP architecture.

1. Introduction and Motivation

Powerful out-of-order (OOO) and superscalar processors have dominated the traditional computing space until recently. The complexity of these out-of-order designs significantly increases the transistor count. As the number of transistors on the processor chips increases and moves past beyond the billion mark, some inherent concerns are exposed; including power dissipation, memory capacity limitations and delays due to global wire communication across elements on the processing chip. The complexity of hardware structures needed to extract implicit parallelism in out-of-order (OOO) processors increases power dissipation and the overall complexity of processor design. Therefore, the trend of increasing single processor frequency and complexity of processing elements present in an OOO processor is seen as a not viable option. But there is still a need to provide solutions which address improving the performance of single-threaded applications. Current research efforts are focused on building chip multiprocessors. These multicore chips consist of several simpler cores, with less complex hardware structures. The inherent nature and configurations of CMPs naturally lend themselves to improved performance for multi-threaded and parallel applications. In addition, there has been a large increase in multithreaded and parallel programming to take advantage of the multiple data stream processing power of CMPs. However, a majority of applications available are single-threaded, and single-threaded execution performance is not explicitly addressed by multicore designs. While some compiler techniques exist for extracting parallelism in program loops, the level of parallelization available in some applications is limited. In order to fully extract parallelism from these applications, significant time and effort by programmers would be required. More recently there have been several efforts [1, 2] to improve, adapt or modify CMP hardware for single-threaded performance improvement. Most of these schemes show limited improved performance compared to single core OOO execution, and often require significant extensions to hardware structure in CMPs (thus defeating the purpose of using simple cores).

In this research we take an approach that relies heavily on compilers to extract fine-grained parallelism from single-threaded applications, and executing these threads on several simple cores. This approach requires minimal extensions to the hardware. We call our system

Parabilis. Parabilis extracts fine-grained threads through the use of compiler optimization algorithms that statically schedules independent instructions on different cores in a CMP configuration. However the problem of data dependency limits the number of threads that can be extracted. This can either be overcome by inter-thread communication or instruction replication. We choose to replicate instructions to avoid the overhead of inter-thread communication. We believe that exploiting parallelism at the basic block level results in improved performance for "single-threaded" applications. Parabilis is implemented with minimal hardware modification of a conventional CMP configuration. We add a cross-register communication network, based on idea of the operand network seen in [3], and new state bit to registers to track data dependence and assure program correctness for replicated instructions executed on different cores. We show that Parabilis significantly improves the speed of "single-threaded" applications running on a CMP, and approaches the performance of OOO processors.

The rest of this paper is organized as follows: Section 2 surveys related research in this area. The algorithm and additional hardware modifications needed for Parabilis are discussed in Section 3. Section 4 presents the simulation methodology and experimentation results of our scheme. The results and analysis are presented in Section 5. In Section 6, we highlight factors on the limitations of this work and detail future work needed to overcome these limitations. Finally, Section 7 concludes this paper.

2. Prior Related Research

The prohibitive power consumption and increasing hardware complexity, coupled with the increasing difficulty in improving instruction level parallelism has led to renewed interest in research for alternative solutions. The adoption of CMPs over SMT processors by industry supports this notion. The limitations of CMPs for sequential or single thread based applications have continued to drive the need to adapt CMPs for such applications. The native configuration of CMPs naturally lends itself to improved performances for parallel applications. However, OOO processors still provide better performance than CMPs when executing single-threaded applications. To this end, there has been a significant amount of research on what configuration is best to adopt.

One approach utilized by several proposals employs primarily hardware modifications to explore single-thread performance improvement. In [1], a dual configuration architecture is proposed, in which groups of independent CMPs can be dynamically fused into a more powerful single core. This approach aims to accommodate software diversity by using independent CMPs for parallel applications and fused cores for sequential applications. Similar configurations are also explored in [2, 3]. These approaches tend to ease the constraint of power consumption and simplify the design of complex cores by using multiple simpler in-order cores. While fusing cores does yield performance approaching single OOO processor performance, fusing of cores introduces several additional hardware complexities.

There has also been published research which utilizes the approach of thread decomposition. The single stream of instructions present in a single-threaded applications can be split into smaller threads at varying levels of granularity. In [4], a scheme is proposed where a sequential application is speculatively decomposed into fine-grained threads for execution on CMPs. Since the threads are speculatively decomposed at compile time, threads incur data dependencies, which may be addressed by inter-thread communication or instruction replication. Parabilis is largely inspired by this scheme, however we seek to present an approach to extract finer-grained threads which we claim achieve more thread level parallelism in sequential applications. In addition, [5] presents a work very similar to our paper. Their simulation results are similar to our work, and serve as further justification of the ideas presented. The work in [6] utilizes execution profiling to select candidates from potential mini-threads which have been extracted from single-threaded applications, which may subsequently be compiled into the application itself. In general, this approach introduces the challenges of thread scheduling in addition to load balancing across the cores. Managing data dependencies across threads is another key issue, which is further complicated by the cost of inter-core communication to handle data dependencies across the threads. The research in [7] presents a scheme to address data dependencies across threads by utilizing compiler and hardware support to deduce and insert synchronization instructions into threads created from a single-threaded application.

Loop iterations present another prospective target for thread partitioning, however optimal thread extraction still presents some challenges for loops with loop-carried data dependencies. In addition, pointer references may prevent a compiler from statically extracting loop-level parallelism inherent in an application. The work in [8] is a related scheme in which loops are partitioned into fine-grained threads for execution on multiple cores, while using speculation to handle dependences. Loops which are resistant to compiler optimization due dynamic references can be decomposed into component threads, akin to a producer-consumer model. Using appropriate synchronization, these component threads can be set to execute on different cores. In [9], an algorithm that overcomes the problems of load balancing and inter-core communication is presented. For each loop iteration, [10] speculative threads are spawned, which are squashed if they are dependent on previous iterations. The research in [11, 12] present a Java-based run-time system consisting of a hardware profiler to dynamically profile loops to determine optimal iteration candidates for parallelization. In [11], a dynamic compiler is also used to re-compile selected speculative thread loops for parallel execution.

Instruction replication can be used to further exploit parallelism, which may be employed in concert with thread decomposition to reduce or eliminate inter-core communication and data dependencies. In [13], the authors present an approach utilizing modulo scheduling and instruction replication for loops on clustered micro-architectures while [14] presents an approach that optimizes instruction replication to minimize the overheard of inter-core communication. This approach speculatively decomposes single-threaded applications and employs a balanced min-cut approach that minimize load imbalances while keeping communication overheard low. In [15], a technique for duplicating instructions for execution in VLIW architectures is presented. The work in [9] presents a scheme to selectively replicate instructions in multi-clustered architectures. The clusters are connected through an interconnect to support inter-cluster communication. Both of these techniques primarily utilize compiler support, but additional hardware is needed to enforce instruction dependencies. Speculative CMPs [16, 17], provide hardware structures for this purpose, in addition to temporary storage for, and the ability to roll back speculative execution.

Our work explores finer-grained threads than [4] and we use recursive thread decomposition. In addition, we attempt to minimize load imbalances by examining latency costs while selecting candidate threads, at the same time eliminating inter-thread dependencies by replicating instructions.

3. Parabilis:Algorithm and Hardware Support

Our proposed scheme is called Parabilis, which utilizes compiler support in combination with minimal hardware modifications. The following subsections detail the methodology and hardware modifications necessary for implementing Parabilis.

3.1. Compiler Algorithm Optimizations

The static compile time algorithm extracts fine grain threads through the use of graph traversals. The instructions and data dependencies in a basic block can be represented as a directed acyclic graph (DAG) [18] (an example is shown in figure 1).

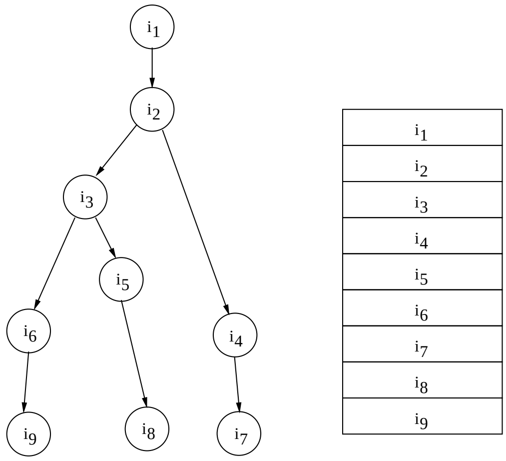


Figure 1. Example of Basic Block and Schedule

Paths from the root node(s) to the leaf nodes represent potential fine-grained threads for parallel execution. The number of leaf nodes dictates the maximum number of parallel threads that can be extracted from a basic block. The figure 2 shows a possible thread extraction of the basic block in figure 1.

The set of vertices and edges representing a path is an incomplete representation of a fine-grained thread. The goal is to obtain a set of edges and vertices such that no edges cross the sub-graph boundary. Therefore, the vertices representing additional instructions are incorporated into the set (i.e., replicated) until this goal is accomplished, which forms a complete thread subgraph. These subgraphs, represented as fine-grained threads, can be scheduled to execute concurrently on different cores. Instructions may appear in multiple subgraphs. The replication of instruction in multiple threads eliminates data dependencies among the threads.

Using replicated instructions, the need to exchange data in registers (corresponding to dependent variables) is eliminated - the each thread will compute its own register values for the dependent variables. However, the replication of instructions may lead to load-imbalance (some threads may have more more instructions to execute), and the need to merge the computed values in registers. We analyze the load imbalances and merging of registers in scheduling fine-grained threads on available cores. Our thread generation algorithm is detailed below 1.

Algorithm 1 Algorithm that implements Parabilis

```
1:  Parse the assembly code.
2:  Extract the basic block.
3:  Find dependencies within instructions within each
    basic block
4:  Each thread starts from each leaf nodes including all
    dependent instructions
5:  Keep the longest thread and combine the short
    threads that give the most repetition to fit under the
    longest limit
6:  for do
7:      If too many threads force merge with smallest
        cost
8:      Longest_Thread + Comm_Overhead =
        BB_Latency
9:  end for
10: while Basic Block not finished do
11:     Move to the next basic block.
12: end while
```

The algorithm starts by identifying and then extracting basic blocks from the code generated by a compiler. After the basic blocks have been extracted, dependent instructions are found. All basic fine-grained threads are extracted by exploring all dependent paths from the leaf nodes to the root. The initial number of fine-grained threads extracted is only limited by the available leaf nodes and not based on the number of cores, creating more fine-grained threads than the number of cores available. We then combine the fine-grained threads in such way that the execution time (or execution latency) of the larger thread does not adversely increase the parallel execution of the fine-grained threads. Note that the execution time of the basic block is limited by the fine-grained thread with maximum number of instructions. We also considered using the number of replicated instruction as criteria for merging threads.

If the number of threads remaining is still more than the available cores, we employ a cost minimizing technique to determine which threads to combine. We exhaustively search for pair-wise thread combinations that yield the best overall execution times (or execution latencies). We repeat this process of pair-wise merging of threads until the number of threads is equal to the number of cores. Figure 3 shows an example using the threads generated in figure 2 with 2 cores. An exhaustive search for merging T_1, T_2, T_3 is done to find which thread combinations yield the best latencies. There are three possible combinations for these three threads, [(T_{12}, T_3), (T_{13}, T_2), (T_{23}, T_1)]. The best combination is(T_{13}, T_2). This example shows that although T_1 and T_2 have more common instructions, but their merger does not yield the best savings. This cost defined in lines 7 and 8 of Algorithm 1 favors greater latency savings, which is our main goal.

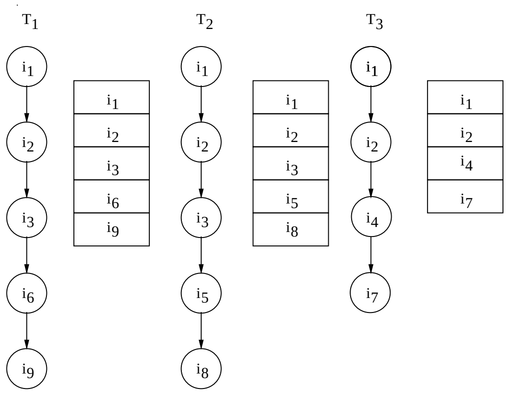


Figure 2. Example of threads extracted from a Basic Block

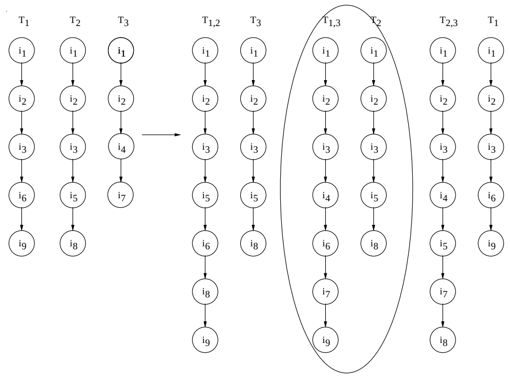
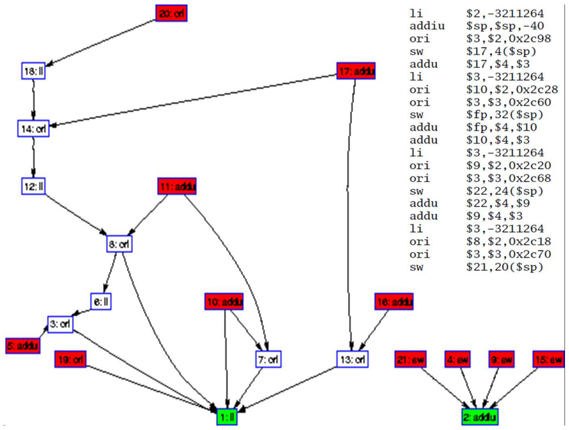


Figure 3. Example of Force Merging

Optimal scheduling is an N-P complete problem and our scheduling algorithm does not always provide the optimal solution. The figure 4 displays an example of a basic block from an actual code in MIPS assembly language and the resulting threads.

The number of thread which can execute concurrently is constrained by the number of available cores. The overall execution time of the basic block would be bound by the execution time of the longest fine-grained thread. At the end of a basic block execution, register values need to be communicated across the cores. To this end, we propose some basic hardware modifications to facilitate this process. These modifications are detailed in the next subsection.



```
li      $2,-3211264
addiu   $sp,$sp,-40
ori     $3,$2,0x2c98
sw      $17,4($sp)
addu    $17,$4,$3
li      $3,-3211264
ori     $10,$2,0x2c28
ori     $3,$3,0x2c60
sw      $fp,32($sp)
addu    $fp,$4,$10
addu    $10,$4,$3
li      $3,-3211264
ori     $9,$2,0x2c20
ori     $3,$3,0x2c68
sw      $22,24($sp)
addu    $22,$4,$9
addu    $9,$4,$3
li      $3,-3211264
ori     $8,$2,0x2c18
ori     $3,$3,0x2c70
sw      $21,20($sp)
```

Figure 4. Basic Block:Thread Extraction and Scheduling

3.2. Hardware

Parabilis extends the basic architecture found in CMPs with additional register metadata and a cross-core register communication network bus. The special cross-core register communication bus is based on the technique used in [3]. A diagram of a multicore Parabilis architecture is shown in figure 5. The figure shows how conventional CMPs cores can be connected with the cross-core register communication network bus. Each core has private L1 (instruction and data) and L2 caches. An expanded view of a single core is also shown in figure 5. It shows how the cross-core register data is communicated to each core through the help of a communication functional unit (Comm FU).

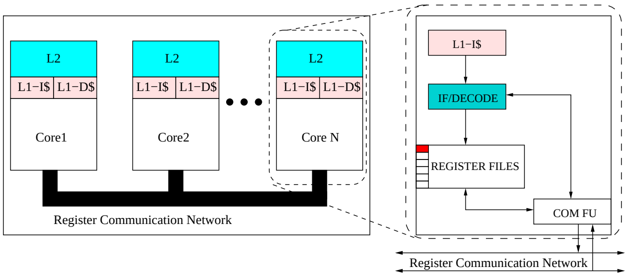


Figure 5. Conceptual Parabilis Architecture

An extra register bit is added to the register metadata to indicate if that register has been modified by that core during the basic block execution. A '1' signifies that the register has been modified and the updated value needs to be communicated to other cores (for use in computations in future basic blocks) at the end of the basic block execution. A '0' signals that the register has not been modified and the current values are valid. After the execution of the basic blocks, all registers with a modified value are broadcast to other cores on the register communication bus. The fast cross-core communication bus is able to communicate a register value in 3 cycles. Our estimates differ from the one in [3] by a cycle. The estimates for communication in [3] add an extra cycle per hop between cores. Our configuration allows for direct communication between all cores. Further details are discussed in the performance evaluation section.

4. Performance Evaluation and Simulation Setup

In evaluating Parabilis, we compare the speedup achieved by Parabilis to that of conventional CMPs and OOO for selected SPEC2006 Benchmarks. We evaluate speed up by comparing the reduction in total cycles needed for execution. In the following subsections, the configuration and simulation setups are discussed.

4.1. Configuration

For Parabilis, we assume simple in-order cores and each core has one functional unit of each type; floating point (FP), Integer (Int), Multiplier (Mult). For the OOO simulation, we assume 2-wide instruction issue architecture with one functional unit of each type: floating point (FP), Integer (Int), Multiplier (Mult). We run simulation tests for up to 64 cores of a CMP.

4.2. Simulation

Our thread generation algorithm is applied to thee MIPS code generated by the GCC compiler for the selected SPEC-2006 benchmarks. We use estimated latencies for each MIPS instruction to compute the execution cycle-times for the benchmark programs. The instruction latencies used in our study are taken from [19]. For register communication after completing a basic block, we assume 3 cycle delay: one cycle to push updated values to the register network, one cycle to propagate values across the network, and one cycle to update the registers. In addition, we model a perfect network with a 0 cycle communication latency to establish an ideal maximum bound for performance.

5. Results and Analysis

Table 1 and Fig. 6 show the results offer simulations, normalized to the execution time of a single in-order

CMP core. We achieved the best performance gains for mcf, even beating the performance of OOO core, when 16 simple cores are used. In addition, milc approaches the performance of an OOO core when using 64 cores The general trend across all benchmarks achieve only small gains beyond the 8 cores. The average speedups are 1.30, 1.44, 1.50, and 1.51 for 2, 4, 8 and 16 cores, respectively.

Table 1. Simulation Results With Communication Overhead

Config	2	4	8	16	32	64	OOO
bzip2	1.119	1.140	1.145	1.145	1.147	1.147	1.682
gcc	1.267	1.359	1.387	1.393	1.398	1.400	1.512
hmmer	1.357	1.556	1.632	1.648	1.661	1.667	1.995
lbm	1.494	1.930	2.160	2.185	2.232	2.244	3.272
mcf	1.320	1.448	1.491	1.498	1.505	1.507	1.487
milc	1.412	1.677	1.793	1.833	1.849	1.855	1.859
sjeng	1.272	1.378	1.408	1.47	1.425	1.427	1.738
specrand	1.099	1.176	1.195	1.195	1.210	1.210	1.557
sphinx3	1.367	1.527	1.579	1.591	1.599	1.602	1.673
Geometric mean	1.293	1.444	1.502	1.513	1.525	1.528	1.809

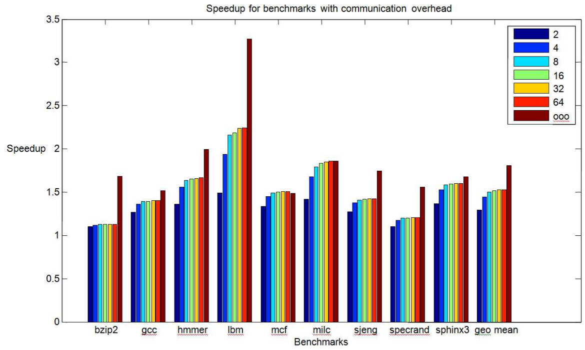


Figure 6. Speedup for Benchmarks with Communication

Table 2 and Fig. 7 shows our results when the communication overhead is set to zero. The results are similar to those obtained with a 3 cycle communication overhead. The average speedup is slightly better at 1.33, 1.49, 1.55 and 1.56 for the 2, 4, 8 and 16 cores respectively. This indicated that even with a perfect bus mechanism the scheme does not exceed the performance of an OOO core.

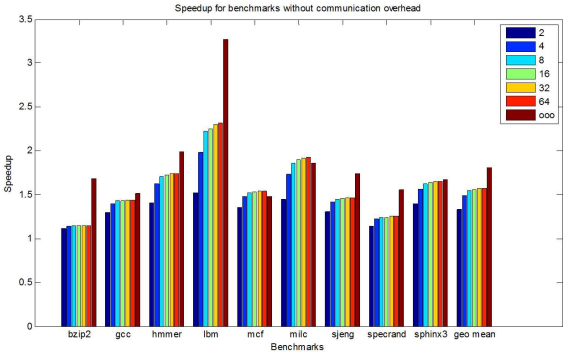


Figure 7. Speedup for Benchmarks without Communication

5.1. Analysis

From the simulation results, we see an improved speedup for applications using simple in-order cores. However, on average the performance is still less than that of a OOO core. For the milc and mcf benchmarks we equal or outperform OOO cores. Even though we do not outperform OOO, we obtain an average speedup of 1.5 using 8 in-order cores, when compared to using a single in-order core. We can further improve the performance achieved by our system using simple compiler techniques like loop unrolling, software pipelining, instruction reordering and variable (register) renaming. We believe that the primary reason for the OOO core performance is their use of register naming (with a large number of renaming registers). This renaming eliminates many data dependencies and permits concurrent execution of instructions (in out of order). We hope to explore register renaming for CMPs in our future work.

6. Future Work and Limitations

6.1. Limitations

Our implemented model as it stands, contains some limitations. The execution stream is a simple traversal of the assembly code produced, and does not account for the factors introduced by control flow changes, particularly the multiple jumps associated with loops. In addition, this scheme does not account for latencies introduced by load or store misses. The variable latencies imposed by network traffic and the memory hierarchy will have a significant impact on the performance gains. Another limitation is the nature of the static scheduling, which forces a the application to conform to a set CMP configuration.

6.2. Future Work

In the future we will explore extensions to our architecture by exploiting register renaming. Register renaming will reduce the number of anti and output dependencies, allowing for the extraction of more finer-grained threads. In particular, the length of the longest thread, based on the number of instructions in the thread, can be shorted since some data dependencies are eliminated with register renaming, and eliminate the need for replicated instructions. In addition, using liveness analysis, the number of registers that need to be updated by the fine-grained threads across basic blocks can be reduced (only the live registers need to be updated). As previously mentioned, accounting for the variable latencies of memory operations is another important factor to investigate.

Another potential factor is the use of selective decomposition of a basic block for execution on multiple cores. If the achieved performance is small, we may execute the code of a basic block on a single core. One other area we can examine is the potential of exchanging register values during the execution of threads of a basic block (and not wait until the end of the basic block). This allows cores to proceed to execute threads from different basic blocks, without waiting for all computations of a basic block to complete. The addition of a priority bit to each register will allow the communication of prioritized values during basic block execution, reducing the need for replication instructions. We also wish to address the limitations imposed by the use of compile time thread generation. An application may be compiled for individual CMP configurations, but hardware resources available to the application may be variable, and adapting the scheduling to account for this variability can improve the scalability and performance. [20] presents a potential basis for work in this area.

Table 2. Simulation Results Without Communication Overhead

Config	2	4	8	16	32	64	OOO
bzip2	1.118	1.140	1.145	1.145	1.146	1.146	1.683
gcc	1.303	1.401	1.430	1.437	1.441	1.444	1.512
hmmer	1.407	1.623	1.705	1.723	1.737	1.744	1.995
lbm	1.525	1.982	2.226	2.253	2.303	2.315	3.272
mcf	1.359	1.482	1.527	1.534	1.542	1.544	1.487
milc	1.453	1.735	1.860	1.903	1.920	1.927	1.859
sjeng	1.306	1.417	1.449	1.458	1.467	1.469	1.738
specrand	1.139	1.220	1.241	1.241	1.258	1.258	1.557
sphinx3	1.401	1.570	1.626	1.638	1.646	1.649	1.673
Geometric Mean	1.328	1.488	1.550	1.562	1.574	1.577	1.809

7. Conclusion

We have presented Parabilis as an alternative approach to the task of increasing the performance of CMPs for executing single-threaded applications. Parabilis addresses this by utilizing compile time analysis to extract fine-grained threads from a single thread and selectively replicating instructions, so that threads can be executed on multiple cores. Parabilis accomplishes this with minimal hardware extensions. The results of our simulations show a 50% speedup over a base simple in-order CMP core. We use this measure since, without OOO, single threaded applications can only run on one simple core. Parabilis achieved up to 83% of the performance of 2-issue Out of Order core. Our study can be improved by accounting for cache misses, and the performance of Parabilis can be improved using (register) renaming, selective replication of instructions, and other compiler techniques such as unrolling loops, software pipelining, instruction reordering.

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